

A WIDE DYNAMIC RANGE LINEAR-AND-LOG ACTIVE PIXEL

FIELD OF THE INVENTION

[0001] The present invention relates to a pixel circuit which operates in both linear and logarithmic regions, to obtain an improved dynamic range.

BACKGROUND OF THE INVENTION

[0002] Imaging systems often need to have pixels capable of handling a wide dynamic range to accommodate varying brightness levels of an imaged scene. Several different pixel circuit architectures have been developed for this purpose. However, they generally increase pixel circuit complexity and present difficulties such as increased pixel size, non-linear response characteristics, and pixel-to-pixel signal deviations, among others.

BRIEF SUMMARY OF THE INVENTION

[0003] The present invention discloses a simple pixel architecture which achieves increased dynamic range by having both a linear and a logarithmic response characteristic. A method of operating the pixel is also provided.

[0004] In one aspect, the invention discloses a pixel circuit having an integration node; a conversion transistor having a source/drain connected to the integration node and a drain/source connected to a reset line; a feed-through pulse capacitor having one leg connected to a feed-through pulse signal line and the other leg connected to the integration node; a photodiode having one leg connected to the integration node; and an output transistor having a gate connected to the integration node. The pixel circuit operates in a linear mode when the integrated charge at the node is at a lower level which causes the conversion transistor to operate in an shut-off mode and operate in a logarithmic mode when the integrated charge is at a higher level which causes the conversion transistor operates in a sub-threshold mode.

[0005] In yet another aspect the invention provides a method of operating the pixel circuit. The method includes operating the reset and feed through pulse signal lines to provide a maximum reset voltage at a pixel integration node, providing the reset voltage as a reset output signal through an output transistor, accumulating charge at the node with the photodiode during an accumulation period in which the conversion transistor operates first in an shut-off range and, if needed, then, in a sub-threshold range to produce an image signal at the node, and providing the image signal as a pixel output signal through the output transistor.

[0006] These and other features and advantages of the invention will be more clearly seen from the following detailed description of the invention which is provided in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Fig. 1 is a block diagram of an imaging device of the present invention;

[0008] Fig. 2 is a schematic diagram of the active pixel circuit of the present invention;

[0009] Fig. 3 is a timing diagram depicting operation of the pixel circuit of Fig. 2;

[0010] Fig. 4 is a graph of the raw linear and logarithmic response regions of the Fig. 2 pixel;

[0011] Fig. 5 is a graph of the standardized linear and logarithmic response regions of the Fig. 2 pixel; and

[0012] Fig. 6 is a flowchart depicting the process of separating, processing, and recombining the color and brightness signals outputted from the pixel circuit of Fig. 2.

DETAILED DESCRIPTION OF THE INVENTION

[0013] The present invention is employed in a CMOS imaging device generally illustrated in Fig. 1 by numeral 10. The imaging device includes an array of pixels arranged in rows and columns with each pixel having a pixel circuit 100. The pixel circuit 100 provides a reset signal V_{RST} and a pixel image signal V_{SIG} as outputs during a reset and integration period which are captured by the sample and hold circuit 200 respectively in response to sampling signals SHS (for the image signal) and SHR (for the reset signal). A sample and hold circuit 200 is provided for each column of pixels. Since the pixels are selected in a row by row fashion each pixel column will have a column line to which all pixels of that column are connected. The sample and hold circuit 200 provides the reset signal V_{RST} and image signal V_{SIG} of a pixel circuit 100 to an amplifier 40 which in turn provides a signal representing the difference between the reset signal and pixel image signal ($V_{RST} - V_{SIG}$) as an output. This difference signal is provided to an analog to digital converter 60 and from there to an image processor 80 which receives digitized pixel signals from all pixel circuits 100 of the pixel array and provides an image output.

[0014] The active pixel circuit 100 in accordance with the invention is shown in more detail in Fig. 2. It includes a conversion transistor 116, an output transistor 120, a row select transistor 124, a photodiode 108, and a feed-through capacitor 117. Also provided are a row select signal line 131 receiving a row select signal RD, a reset signal line 121 receiving a reset signal RST and a feed through pulse line 119 receiving a feed through pulse signal FTP. A voltage supply line 123 is also provided which supplies a voltage V_{AAPIX} to the pixel circuit 100. The conversion transistor 116 has a gate threshold voltage of V_t and is operated either in a shut-off voltage operating mode or a sub-threshold voltage operating mode, as described in greater detail below. The feed through capacitor 117 is located between the horizontal feed through pulse (FTP) signal line 119 and a signal

integration node 104. One source/drain region of the transistor 116 is connected to the row reset (RST) signal line 121, while the gate of transistor 116 is connected to the power supply line VAAPIX 123, and the other source/drain region of transistor 116 is connected to integration node 104. The photodiode 108 is connected to the integration node 104 and ground. One source/drain region of an output transistor 120 is connected to the supply line VAAPIX 123 while the gate of transistor 120 is connected to the integration node 104. The gate of row select transistor 124 is connected to the row select signal line which receives the row select signal RD, while the source/drain regions of the transistor 124 are respectively coupled to output transistor 120 and column line 126.

[0015] When connected to the column line 126 through the row select transistor 124, the output transistor 120 operates as a source follower transistor and provides a gain to the charge signal received from node 104.

[0016] As noted, transistor 116 has two operating modes. One operating mode is a shut-off operating mode in which the transistor 116 imparts a linear output to an accumulated pixel image signal V_{SIG} at node 104 during a charge integration period, while the other operating mode is a sub-threshold operating mode which imparts a logarithmic output to the pixel image signal V_{SIG} accumulated at node 104.

[0017] The operation of the pixel circuit 100 will now be explained with reference to the timing diagram of Fig. 3, which shows a typical frame cycle during operation of the pixel circuit 100. At the time t_0 , the sample and hold signal (SHS) pulse which causes pixel image signal sampling is applied to a sample and hold circuit which causes the pixel image signal V_{SIG} to be sampled and held. The read out signal RD is also high, signifying that charge accumulated at a node 104 is being read out. This charge was accumulated at node 104 prior to the time t_0 . At the time t_1 , the SHS pulse goes low thus completing the sampling of the image signal V_{SIG} voltage level. At the time t_2 , the RST

line and the feed-through pulse line (FTP) go low. This causes VPIX, the voltage at node 104, to be set to the RST line 121 low voltage. At time t3, the RST line 121 goes high beginning the process of resetting the pixel. This causes VPIX, the voltage at node 104, to begin increasing toward VAAPIX-Vt(116). At time t4, the FTP line goes high which causes VPIX to reach the level shown in equation (2) below:

$$VPIX = VAAPIX - Vt(116) + CFTP/CPIX \times \Delta FTP \quad (2)$$

[0018] where CFTP is the capacitance of the capacitor 117, CPIX is the total capacitance at the node 104, and ΔFTP represents the difference between the high and low state of the FTP line 119, as shown in Fig. 3.

[0019] At the time t5, the SHR pulse goes high, thus sampling the reset voltage level by the sample and hold circuit 200. The pixel circuit reset voltage V_{RST} is produced by the output transistor 120 and is applied through the select transistor to the column line 126. At time t6, the SHR pulse goes low, ending the sampling of the reset voltage VRST. At time t7, the RD line goes low ending the first readout process, and beginning a charge accumulation (integration) period. During the period from t7 to t8, the conversion transistor 116 operates in an shut-off mode and a linear accumulated charge signal is processed at the node 104. At the time t8, the conversion transistor 116 switches to a subthreshold operating mode as the accumulated signal at node 104 forces the transistor 116 into a sub-threshold operation region. At the point t8 the pixel voltage VPIX at node 104 transitions from a linear to a logarithmic output signal, as shown in shown in equation (3) below.

$$VPIX = VAAPIX - Vt(116) + CFTP/CPIX \times [\Delta FTP - \Delta ft] \quad (3)$$

[0020] In the equation (3) the symbol Δft is used, which as shown in Fig. 3 represents the instantaneous drop in VPIX at time t7 which occurs when the circuit 100 begins operating in a linear integration mode.

[0021] At the time t_9 , the RD and SHS lines go high, the charge accumulation (integration) period ends and the accumulated pixel voltage V_{PIX} is read out by the transistors 120, 124 as the pixel image signal V_{SIG} , and a new frame cycle begins.

[0022] The SHS and SHR pulses correspond to when the signal and reset voltages, respectively, are sampled. As with the control lines FTP, RD, and RST, the SHR and SHS pulses are produced by the signal controller 70 (Fig. 1).

[0023] The sampled signal V_{SIG} and reset V_{RST} voltages are then subtracted by amplifier 40 to obtain valid pixel image data. In equation (2) the symbol ΔFTP is used, which as shown in Fig. 3 symbolizes the difference between the high and low states of the FTP line. The voltage on the FTP line enables the circuit to achieve both linear and logarithmic responses, depending on the level of accumulated charge on the node 104. This is because when signal charge accumulates at the node 104 (Fig. 1) is small, they can all be integrated at the node 104. However, as the amount of signal charge increases to the point where some overflows to the transistor 116 (at time t_8 in Fig. 3), the photo response of the entire circuit becomes logarithmic. Thus, the FTP signal line provides a way to achieve linear response under low illumination conditions, yet preserve the circuit's logarithmic capability for higher illumination conditions. As shown in Fig. 3, the cross-over between the linear and logarithmic regions occurs at a pixel node 104 voltage of $V_{AAPIX} - V_T(116)$.

[0024] During the time the circuit 100 is operating in linear mode (time period t_7 through t_8), the photo conversion signal PCS can be expressed as follows.

$$PCS = GAIN_{SF} \times (t_{ac} \times I_p / C_{PIX}) \quad (4)$$

[0025] where $GAIN_{SF}$ is the source follower 112 gain, t_{ac} is the integration (accumulation) time as shown in Fig. 3, I_p is the photodiode current, and C_{PIX} is the total capacitance at the node 104.

[0026] However, when the circuit 100 transitions to operating in logarithmic mode (time period t8 through t9), the photo conversion signal PCS can be expressed as follows.

$$PCS = GAIN_{sf} \times [CFTP/CPIX \times [\Delta FTP - \Delta ft] \times [(1/\beta) \times \log(I_p)]] \quad (5)$$

[0027] where CFTP is the capacitance of the capacitor 117, and the symbol β represents an exponential coefficient of the subthreshold current of the transistor 116. Variations in threshold voltage V_t are one of the most well known causes of instability in MOS transistors. However, variations in the threshold voltage V_t do not affect photoconversion characteristics of the circuit 100. Because threshold voltage changes within the conversion transistor 116 cause the same level shift for both the reset and the transition levels expressed by the equations (2) and (3) above, $V_t(116)$ does not contribute to the range of linear operation of VPIX. Additionally, by subtracting V_{RST} from V_{SIG} , variations in $V_t(120)$ are also suppressed. Consequently, V_t components are not contained in the output 126 of the circuit 100.

[0028] Meanwhile, the conversion gain in both the linear and logarithmic operating regions are determined by the feed through capacitor CFTP, pixel overall capacitance CPIX, and β , as shown in the equation (5) above. Fortunately, variations in these parameters are much smaller than the threshold voltage V_t . Thus, improved uniformity and stability of the circuit 100 is achieved, and problems with fixed pattern noise (FPN) are reduced.

[0029] In equation (5) above, the total capacitance of the pixel node 104 is represented as CPIX. CPIX consists, of course, of CFTP but also includes the capacitance of the photodiode 108 and the sum of parasitic capacitances of the circuit 100 such as the gate capacitance of the transistor 120, and the junction capacitance of the source node of the transistor 116. Prior to a reset operation, a substantial amount of charge is injected into the pixel capacitor CFTP and its potential is then pinned at the 'low' level of the RST line as shown between the time period t2-t3 of Fig. 3. Because of this pinning action, the primary integrated signal is fully discharged from CPIX, so that the reset operation

completely resets the circuit 100, and excess charge from previous imaging cycles of the circuit 100 does not 'lag' into following imaging cycles.

[0030] While the transistor 116 is operating in sub-threshold mode during the time period t_8 - t_9 , any excess charge (overflow) present on the pixel node 104 is drained through the transistor 116. Another contribution to more effective resetting of the circuit 100 is that, during the reset time period t_2 - t_3 , the current through the transistor 116 is much larger than the photocurrent I_p . Therefore, temporal photocurrent during the reset time period does not affect the reset operation, so that a stable reset level for the photodiode 108 can be obtained for the subsequent accumulation period, which thereby reduces image lag.

[0031] When incoming light detected by the photodiode 108 is exceptionally strong, the accumulated (integrated) charge on the capacitor CFTP becomes large. However, any excess signal component (excess charge) becomes compressed because the circuit 100 begins operating in a logarithmic mode. In this way, the circuit 100 can achieve a higher dynamic range more closely resembling the image sensing properties of the human eye. However, special color processing functions (standardization) are still needed for situations where exceptionally bright light is incoming onto the photodiode 108. Fig. 4 shows the raw, non-standardized pixel output voltage of the circuit 100 without any processing by the image processor 80. Fig. 5 shows the standardized pixel output voltage of the circuit 100 after processing by the image processor 80.

[0032] When the circuit 100 is operating in the linear mode (Figs. 3-5), the color enhancement gain G_c is at unity, i.e. equal to 1. When the circuit 100 is operating in the logarithmic mode, the output range is divided into regions 1 and 2, as shown in Fig. 5, where the dividing line between the two regions is an arbitrary, predetermined amount of incident light on the photodiode 108. Fig. 5 shows that a pixel's color may be shifted to white or to some other color by the image processor 80 (Fig. 1), depending on the brightness level of that signal. In region 1 of Fig. 5, the color enhancement gain G_c ranges between 0 and 1 and is not affected by the image processor 80. However, when a pixel

signal is within the logarithmic region 2, the color signal is either eliminated ($G_c = 0$) or set to a predetermined minimum value ($G_c = G_{cmin}$) by the image processor 80.

[0033] Fig. 6 details the standardization process employed by the image processor 80 (Fig. 1) in breaking down logarithmic pixel signals into separate color and brightness components. The digitized pixel output originating from the analog to digital converter 60 is divided into three separate signal branches 504, 508, and 512 by the image processor 80. Branch 504 is for brightness signal extraction, branch 508 is for color signal extraction, and branch 512 is for color gain extraction. In the branch 508, the pixel output is reconverted from a logarithmic to a linear response, then transferred to a color processing circuit to extract its color component. In branch 512, a color gain factor is calculated from the pixel output level as shown in Fig. 5. The color component is then multiplied by the factor of the color gain at processing step 516. From both the gained color signal and brightness signal obtained in the processing branch 504, a final color video signal is constructed at the processing step 520. The brightness component extracted in processing branch 504 requires no additional processing (thus remains "raw"), but it is necessary to process (standardize) the color component 508, 512 prior to applying the gain at processing step 516. Because the photo signal is compressed logarithmically in the pixel output, calculation error increases in reconvertng data to the linear response with increasing brightness, which unfortunately increases color noise in high illumination portions of the images. However, by decreasing color gain in the high illumination conditions at the processing step 516, the color noise can be suppressed thereby yielding a more natural looking low-noise color image.

[0034] While the invention has been described and illustrated with reference to specific exemplary embodiments, it should be understood that many modifications and substitutions can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be considered as limited by the foregoing description but is only limited by the scope of the appended claims.

CLAIMS

1. A pixel circuit, comprising:
 - a photoconversion device for accumulating charge during a charge integration period;
 - a first transistor, having one of a source and drain terminal connected to an integration node;
 - said first transistor operating during said charge integration period in a first mode to provide a linear accumulation of charge by said photoconversion device up to a predetermined charge level, and in a second mode to provide a logarithmic accumulation of charge by said photoconversion device after said predetermined charge level is reached; and
 - a capacitor, having one leg connected to a capacitor signal line, and the other leg connected to said integration node.
2. The pixel circuit of claim 1, further comprising:
 - an output circuit, connected to said integration node, for reading out a signal at said integration node.
3. The pixel circuit of claim 2, wherein said output circuit further comprises an output transistor operating as a source follower readout transistor.
4. The pixel circuit of claim 1, wherein said first mode is a shut-off mode and said second mode is a sub-threshold mode.
5. The pixel circuit of claims 4, further comprising:
 - wherein said first transistor switches from said first mode to said second mode when a voltage at said integration node exceeds a voltage applied to a gate of said first transistor minus a threshold voltage.

6. The pixel circuit of claim 1, wherein said photoconversion device is a photodiode.

7. The pixel circuit of claim 6, wherein the other of the source and drain terminal of said first transistor is connected to a reset signal line and a gate of the first transistor is connected to a supply voltage.

8. The pixel circuit of claim 29, wherein said reset line and said capacitor signal line are operable to apply a reset voltage to said integration node.

9. The pixel circuit of claim 8, further comprising:
an output circuit and a pixel select line for operating said output circuit to read out said reset voltage to an output line.

10. The pixel circuit of claim 9 wherein said pixel select line is operable to begin a charge integration period.

11. A CMOS imaging device, comprising:
at least one pixel circuit;
a sample and hold circuit for storing a reset signal and an image signal produced by said pixel circuit;
an amplifier for subtracting the reset signal and image signal;
a digitizer for receiving an output of said amplifier; and
an image processor for receiving an output of said digitizer;
wherein said pixel circuit further comprises:
a photoconversion device for accumulating charge during a charge integration period;
a first transistor, having one of a source and drain terminal connected to an integration node;
said first transistor operating during said charge integration period in a first mode to provide a linear accumulation of charge by said photoconversion device up to a predetermined charge level, and in a second mode to provide a logarithmic

accumulation of charge by said photoconversion device after said predetermined charge level is reached; and

a capacitor, having one leg connected to a capacitor signal line, and the other leg connected to said integration node.

12. The imaging device of claim 11, further comprising:

an output circuit, connected to said integration node, for reading out a signal at said integration node.

13. The imaging device of claim 12, wherein said output circuit further comprises an output transistor operating as a source follower readout transistor.

14. The image device of claim 11, wherein said first mode is a shut-off mode and said second mode is a sub-threshold mode.

15. The imaging device of claim 14, further comprising:

wherein said first transistor switches from said first mode to said second mode when a voltage at said integration node exceeds a voltage applied to a gate of said first transistor minus a threshold voltage.

16. The imaging device of claim 11, wherein said photoconversion device is a photodiode.

17. The imaging device of claim 16, wherein the other of said source and drain terminal of said first transistor is connected to a reset signal line and a gate of the first transistor is connected to a supply voltage.

18. The imaging device of claim 30, wherein said reset signal line and said capacitor signal line are operable to apply a reset voltage to said integration node.

19. The imaging device of claim 18, further comprising:

an output circuit and a pixel select line for operating said output circuit to read out said reset voltage to an output line.

20. The imaging device of claim 19, wherein said pixel select line is operable to begin a charge integration period.

21. A method of operating a pixel circuit, comprising:

collecting photogenerated charge at an integration node in response to a pixel signal during a charge integration period;

operating a first transistor in a shut-off mode during said integration period when the amount of said collected charge is below a threshold value to cause charge to be linearly collected at said node;

operating said first transistor in a sub-threshold mode during said integration period when said collected charge is above said threshold to cause charge to be logarithmically collected at said integration node; and

prior to a reset operation, injecting charge into a pixel capacitor coupled to said integration node.

22. The method of claim 21, further comprising:

during the time said first transistor is operating in a sub-threshold mode, draining excess charge from said integration node through the first transistor.

23. The method of claim 22, further comprising:

separating said collected charge into color and brightness components;

processing said color component; and

recombining said brightness and color components.

24. The method of claim 23, further comprising:

during the time said collected charge is collected logarithmically, dividing said logarithmic charge-accumulation phase into first and second logarithmic phases corresponding to lower and higher saturation levels respectively; and

during exposure of said circuit to high saturation levels, standardizing the output voltage of said circuit.

25. The method of claim 24, further comprising:

during said second logarithmic phase, eliminating a color signal from an output of said pixel.

26. The method of claim 24, further comprising:

during said second logarithmic phase, setting a color signal from an output of said pixel to a predetermined minimum value.

27. A pixel circuit comprising:

a photoconversion device;

an integration node, connected to said photoconversion device;

a first transistor, for accumulating charge from said photoconversion device onto said integration node;

a signal controller, connected to said pixel circuit, for controlling resetting, signal accumulation, and reading out of said circuit;

a selection transistor, responsive to said signal controller, for selecting when said integration node is to be read out;

a readout circuit, responsive to said signal controller, for reading out said integration node;

an integration capacitor, for accumulating charge at said integration node;

a feed through pulse line, connected to said signal controller and said integration capacitor;

a reset line, connected to said signal controller and said conversion transistor;

a read line, connected to said signal controller and said readout circuit; and

a voltage supply line, connected to said first transistor and also said readout circuit.

28. The pixel circuit of claim 27, further comprising:

said photoconversion device being a photodiode.

29. The pixel circuit of claim 1, wherein the other of the drain and source terminal is connected to a reset line.

30. The imaging device of claim 11, wherein the other of a drain and source terminal is connected to a reset line.

31. The method of claim 21, wherein said step of injecting charge comprises, prior to a reset operation, applying a low signal to one of a source and drain terminal of said first transistor and a terminal of a pixel capacitor thereby injecting charge into the pixel capacitor and pinning said pixel capacitor at a low level of a reset line.

32. The method of claim 31, further comprising the acts of:
subsequent to said step of applying a low signal, applying a high signal to said one of the source and drain terminal of said first transistor while maintaining said low signal on said terminal of said pixel capacitor, and subsequent to said step of applying a high signal to the source/drain terminal of said first transistor, applying a high signal to said terminal of said capacitor.

33. A method of operating a pixel circuit comprising:
collecting photogenerated charge at an integration node in response to a pixel signal during a charge integration period;
operating a first transistor in a sub-threshold mode during said integration period when said collected charge is above a threshold voltage of said first transistor to cause charge to be logarithmically collected at said integration node;
during the time said collected charge is collected logarithmically, dividing said logarithmic charge-collection phase into first and second logarithmic phases corresponding to lower and higher saturation levels respectively; and
processing a signal representing said charge collected during said second logarithmic phase by setting a color signal to a predetermined minimum value.

34. The method of claim 33, wherein the act of processing comprises setting said color signal value to zero.