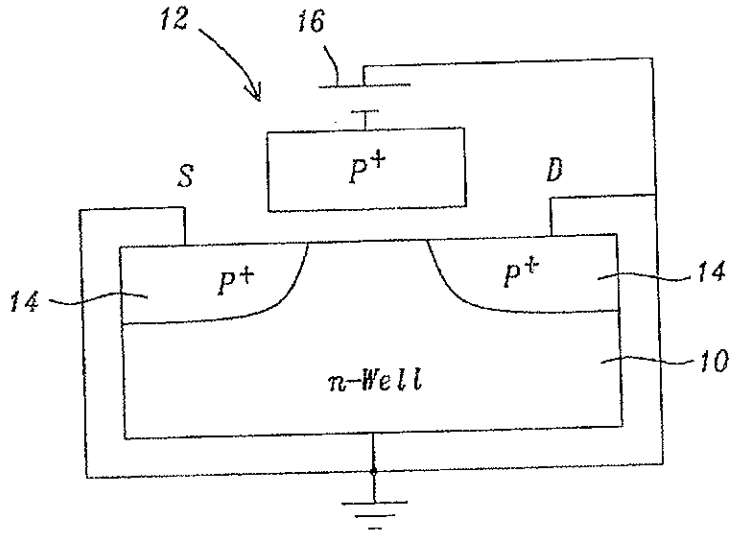


FIG. 1 – Prior Art

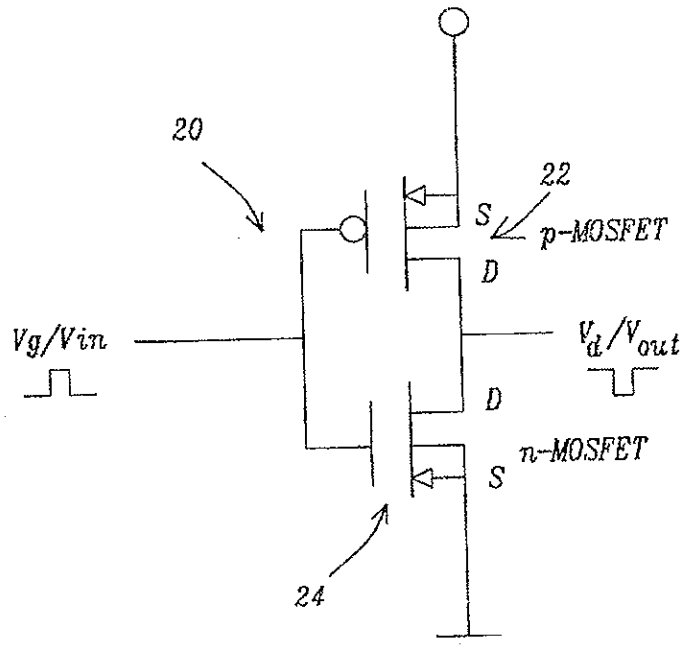


FIG. 2A – Prior Art

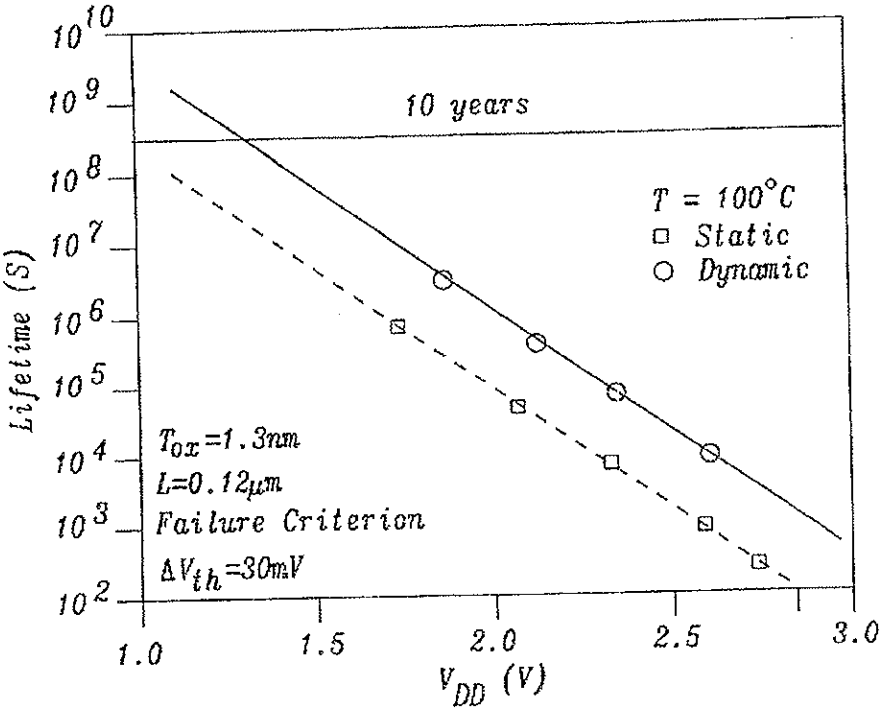


FIG. 2B – Prior Art

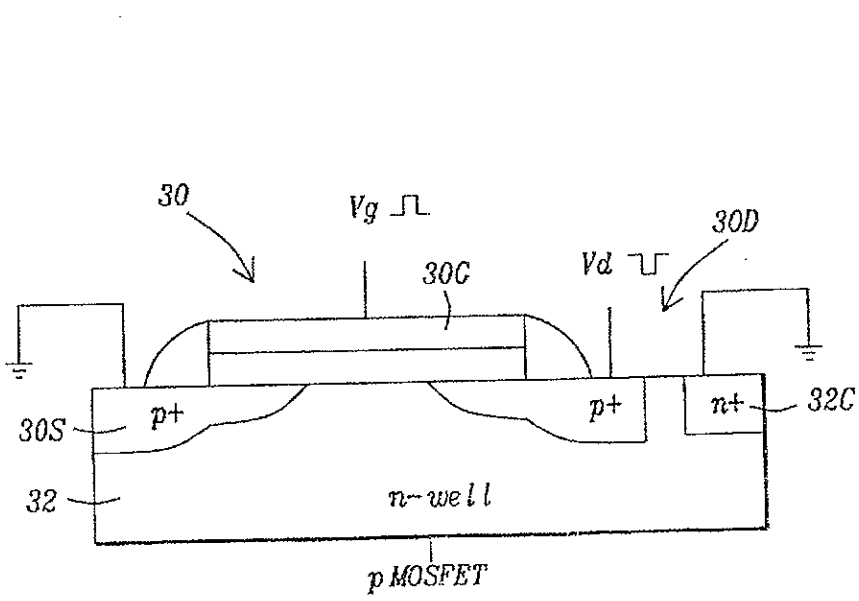


FIG. 3A – Prior Art

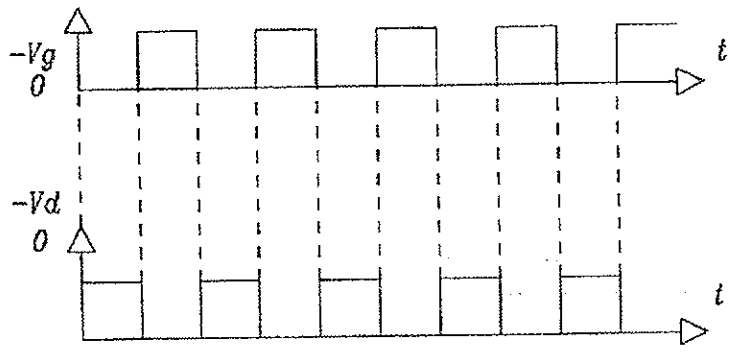


FIG. 3B – Prior Art

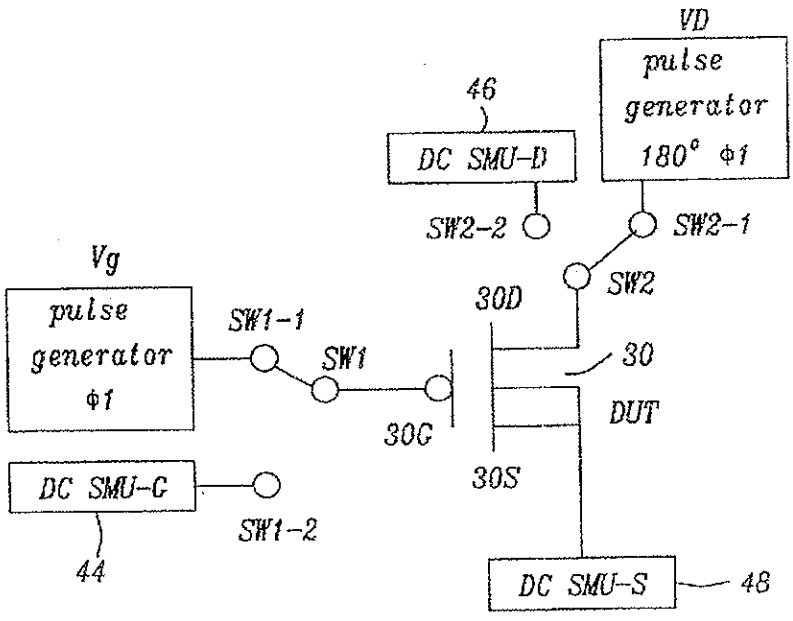


FIG. 3C – Prior Art

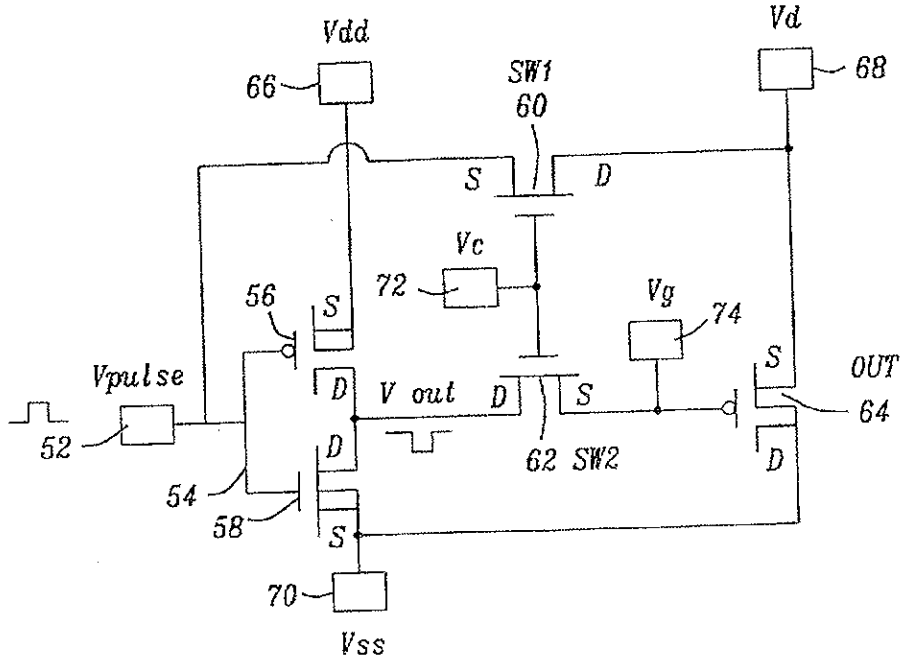


FIG. 4A

During stress,

- Vpulse = gate pulse varies between 0 and Vdd
- Vdd = Vdd
- Vss = 0V
- Vc = Vdd
- Vd = floating
- Vg = floating

During measurement,

- Vpulse = floating
- Vdd = Vdd
- Vss = 0V
- Vc = negative voltage
- Vd = Vd depending on measurement condition
- Vg = Vg depending on measurement condition

FIG. 4B

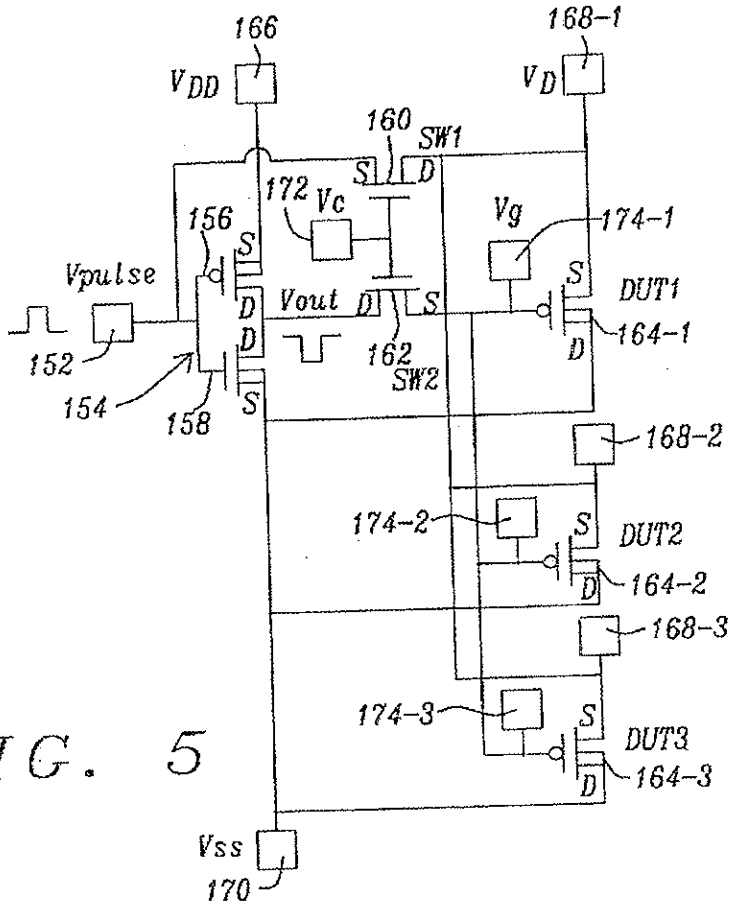

166
V_{DD}
168-1
V_D
160
SW1
S
D
172
V_C
156
S
Vg
174-1
Vpulse
D
Vout
D
S
DUT1
D
164-1
152
154
158
162
SW2
S
168-2
174-2
S
DUT2
D
164-2
168-3
174-3
S
DUT3
D
164-3
Vss
170

FIG. 5

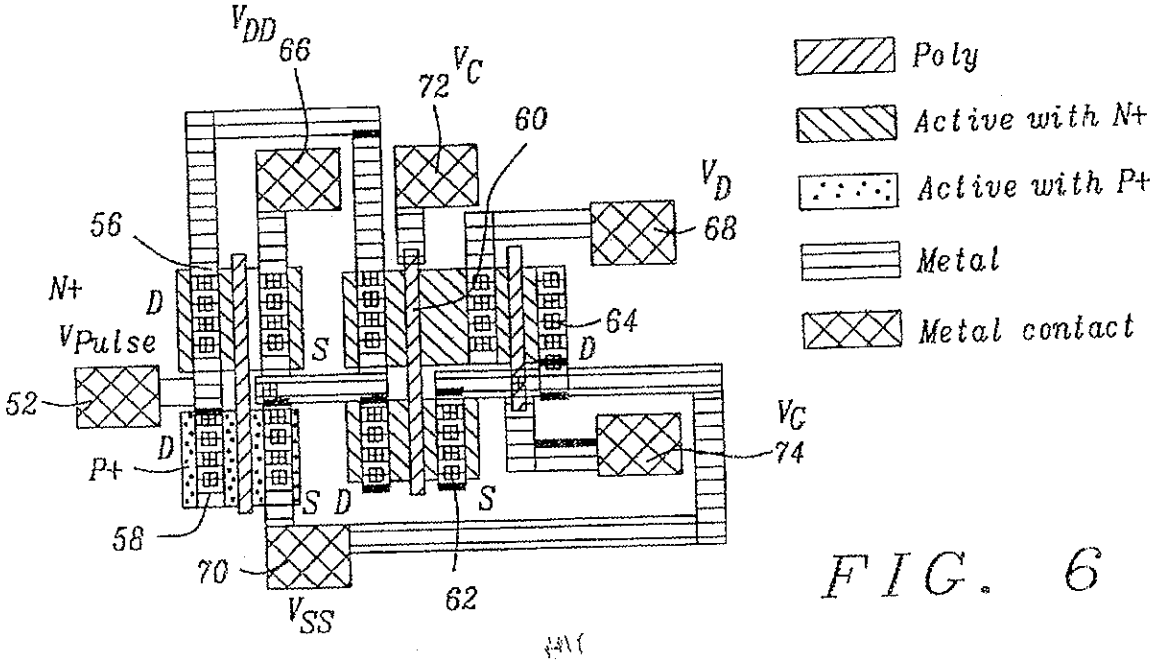

V_{DD}
66
72
V_C
60
V_D
68
56
N+
D
V_{Pulse}
S
64
D
52
D
P+
S
D
S
V_C
74
58
70
V_{SS}
62
Poly
Active with N+
Active with P+
Metal
Metal contact

FIG. 6

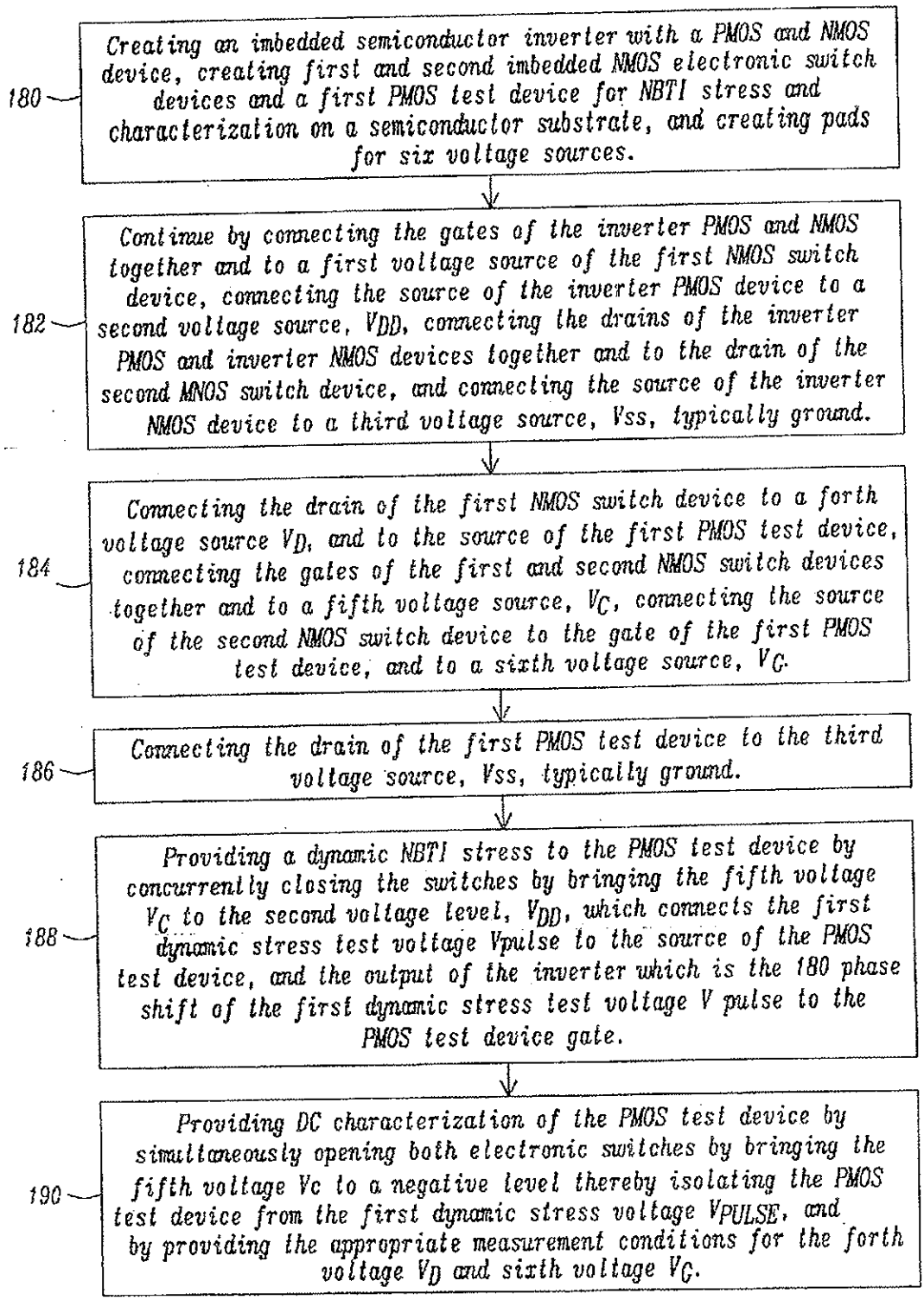

180
Creating an imbedded semiconductor inverter with a PMOS and NMOS device, creating first and second imbedded NMOS electronic switch devices and a first PMOS test device for NBTI stress and characterization on a semiconductor substrate, and creating pads for six voltage sources.
182
Continue by connecting the gates of the inverter PMOS and NMOS together and to a first voltage source of the first NMOS switch device, connecting the source of the inverter PMOS device to a second voltage source, VDD, connecting the drains of the inverter PMOS and inverter NMOS devices together and to the drain of the second MNOS switch device, and connecting the source of the inverter NMOS device to a third voltage source, Vss, typically ground.
184
Connecting the drain of the first NMOS switch device to a forth voltage source VD, and to the source of the first PMOS test device, connecting the gates of the first and second NMOS switch devices together and to a fifth voltage source, VC, connecting the source of the second NMOS switch device to the gate of the first PMOS test device, and to a sixth voltage source, VC.
186
Connecting the drain of the first PMOS test device to the third voltage source, Vss, typically ground.
188
Providing a dynamic NBTI stress to the PMOS test device by concurrently closing the switches by bringing the fifth voltage VC to the second voltage level, VDD, which connects the first dynamic stress test voltage Vpulse to the source of the PMOS test device, and the output of the inverter which is the 180 phase shift of the first dynamic stress test voltage V pulse to the PMOS test device gate.
190
Providing DC characterization of the PMOS test device by simultaneously opening both electronic switches by bringing the fifth voltage Vc to a negative level thereby isolating the PMOS test device from the first dynamic stress voltage VPULSE, and by providing the appropriate measurement conditions for the forth voltage VD and sixth voltage VC.

FIG. 7