SELECTIVE STRESS RELAXATION OF CONTACT ETCH STOP LAYER THROUGH LAYOUT DESIGN

Abstract

A structure and method of fabrication of a semiconductor device, where a stress layer is formed over a MOS transistor to put either tensile stress or compressive stress on the channel region. The parameters such as the location and area of the contact hole thru the stress layer are chosen to produce a desired amount of stress to improve device performance. In an example embodiment for a tensile stress layer, the PMOS S/D contact area is larger than the NMOS S/D contact area so the tensile stress on the PMOS channel is less than the tensile stress on the NMOS channel. In an example embodiment for a compressive stress layer, the NMOS contact area is larger than the PMOS contact area so that the compressive stress on the NMOS channel is less than the compressive stress on the PMOS channel.

Figure 5B