Complementary Field-Effect Transistors and Methods of Manufacture

ABSTRACT OF THE DISCLOSURE

A complementary FET and a method of manufacture is provided. The complementary FET utilizes a substrate having a surface layer with a <100> crystal orientation. Tensile stress, which increases performance of the NMOS FETs, is added by silicided source/drain regions, tensile-stress film, shallow trench isolations, inter-layer dielectric, or the like.

(FIG. 1a)