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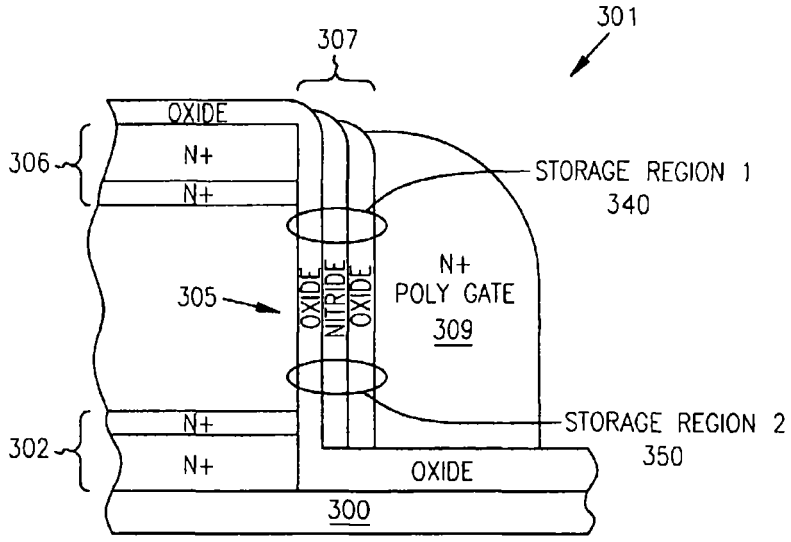
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(54) Title: VERTICAL NROM



(57) Abstract: Structures and methods for vertical memory cell. The vertical memory cell includes a vertical metal oxide semiconductor field effect transistor (MOSFET) (301) extending outwardly from a substrate (300). The MOSFET (301) has a first source/drain region (302), a second source/drain region (306), a channel region (305) between the first and the second source/drain regions, and a gate (309) separated from the channel region (305) by a gate insulator (307). A first transmission line is coupled to the first source/drain region (302). A second transmission line is coupled to the second source/drain region (306). The MOSFET (301) is adapted to be programmed to have a charge trapped in at least one of a first storage region (340) and a second storage region (350) in the gate insulator (307) and operated with either the first source/drain region or the second source/drain region (306) serving as the source region.

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