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(54) IMPROVEMENTS IN OR RELATING TO ELECTRONIC ALARM TIMEPIECES

(71) We, KABUSHIKI KAISHA SEIKO-SHA, a Japanese company, of 5, 2-chome, Kyobashi, Chuo-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electronic alarm timepieces, that is to say to electronic timepieces of the kind having an alarm for giving warning when a pre-set time is reached.

It is now common, in electronic alarm timepieces in which a crystal controlled relatively high frequency time standard oscillator feeds its output into a series of frequency dividing stages to produce a relatively low frequency signal for driving the time display of the timepiece, to use signals derived from one or more of the dividing stages to drive a loud speaker to generate the required alarm sound and, in conventional timepieces of this nature, most of the circuitry employed is, for obvious reasons of miniaturisation and reliability, integrated circuitry. It is important in such timepieces to keep the number of external connections to the integrated circuitry as few as possible because of the tendency of external connections to pick up electrical interference, extraneous electrostatic discharges and so on which may not only interfere with the correct operation of the timepiece by injecting noise signals into the integrated circuitry, but may even damage or destroy semi-conductor devices included in said circuitry. The difficulty of geeping down the number of connections to the integrated circuitry is especially severe in the case of timepieces which are provided with alarms which can be operated at will in accordance with different functional modes, e.g. with alarms the operation of which can be suspended for a time. In conventional electronic alarm timepieces having alarms which can function in accordance with several different modes, it is usual to provide a plurality of switches for selecting the mode of operation desired by the user and to connect

these switches by a plurality of connections to the integrated circuitry which they control. The provision of such a plurality of connections involves a correspondingly great liability to external interference with the correct operation of the timepiece and/or damage to semi-conductor devices in the integrated circuitry. Moreover the presence of such a plurality of connections obviously militates against the achievement of good miniaturisation and good reliability and also substantially increases manufacturing costs.

The present invention seeks to overcome the foregoing difficulties and disadvantages.

According to this invention an electronic timepiece includes a switch arranged to be operated by time actuated means; a manually operable switch; means for producing at a connection point in a circuit common to both switches different potentials representative of different operation states of said switches; a pulse generating circuit for producing a plurality of clock pulse trains; circuit means controlled by the potential at said connection point and by one of said pulse trains for producing different outputs representative of the different operation states; means for producing an alarm sound; and control means for controlling said sound producing means by an output from said circuit means.

Said time actuated switch and said manually operable switch may be connected in series, one of the terminals of the time actuated switch being connected to a point of one predetermined potential, while one of the terminals of the manually operable switch is connected to a point of different predetermined potential, the said connection point being the junction point between the two switches in the series circuit.

The timepiece may have a time standard oscillator and a chain of frequency dividers dividing down the output of said oscillator to produce a relatively low frequency pulse train dividing the time display of said timepiece and signals for driving the alarm sound producing means and employed for

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controlling the operation thereof may be derived from points in said divider chain.

The manually operable switch may be a magnetically responsive reed switch mounted adjacent a permanent magnet and arranged to be actuated by moving a magnetic shield into or out of a position in which it shields the switch from the field of the magnet.

In the preferred embodiment of the invention the aforesaid connection point is common to both switches. This enables the operational states of two switches to be detected with only one connection between them and the integrated circuitry, so that said circuitry has only a minimum number of terminals thereon.

The invention is illustrated in and further explained in connection with the accompanying drawings in which:

Figure 1 is a simplified block diagram of one embodiment of the invention;

Figure 2A is a part sectional perspective view of a practical form of arrangement for the switch 43 included in the circuit in the embodiment of Figure 1;

Figure 2B is a longitudinal sectional view showing the switch arrangement of Figure 2A mounted on an associated support member;

Figure 3 is an explanatory timing chart showing wave forms at various points in the block diagram of Figure 1, the points in question being identified in Figure 1 by lower case letters and the wave forms occurring there being identified by corresponding capital letters in Figure 3; and

Figure 4 is a simplified block diagram of another embodiment of the invention.

Referring to Figure 1, a crystal controlled time standard oscillator 1 supplies its output to a succession of frequency dividers 2, 3, 4, 5 and 6. For example, to quote practical figures, the output frequencies from the dividers 3, 4, 5 and 6 may be arranged to be 16Hz, 8Hz, 4Hz and 1Hz respectively, and the frequency of the oscillator 1 may be, in accordance with customary practice in so-called quartz timepieces, of the order of thousands or tens of thousands of Hz. 7 is a counter, the output from which is used to produce an intermittent alarm sound and which, as will be seen more clearly later, produces an output every five minutes.

Block 8 represents a time display and driving means and comprises a motor driven by output from the divider 4 and driving the time display, normally clock hands, through a suitable gear train. References 9 to 21 inclusive denote gates; references 22 to 29 inclusive denote inverters; and references 30 to 37 inclusive denote flip-flops. Block 38 represents an audio amplifier and 39 is a loud speaker. A resistance 40 is connected in series with what is herein termed a reference switch 42 to the positive term-

inal of a supply potential source and through a manually operable switch 43 to earth and the negative terminal of said source. The value of the resistance 40 is substantially smaller than that of a resistance 41, one end of which is connected to one end of said resistance 40 as shown. The reference switch 42 is arranged (by means not shown) to be actuated by a time mechanism, at a previously set time. Such time actuation is common in conventional alarm timepieces and needs no detailed description or illustration here. The switch 43 is the alarm setting switch, and a preferred arrangement of it is shown in detail in Figures 2A and 2B. Referring to these Figures there is a spindle 145 on one end of which is a push button 144. The central portion 145c of the length of the spindle is an enlarged diameter cylinder on which are formed radial projections 145a and 145b. 146 is a sleeve member which is flanged at one end and is of greater radial thickness over the half of its length nearer the flange than it is over the other half of its length, so that there is a step 146c where the portions of different thicknesses meet each other. Radial slots 146a and 146b are provided in the thicker portion of the sleeve 146 and are dimensioned to receive the projections 145a and 145b so as to allow them to be moved longitudinally, i.e. up and down as viewed in Figures 2A and 2B.

The switch proper—shown at 43 in Figure 1 as though it were an ordinary make and break contact switch—is constituted by an enclosed magnetically responsive reed switch which is in an enclosing envelope, part of which appears in Figure 2A at 143. The envelope is fixed to a stationary member (not shown). The sleeve 146 is fixed to a stationary plate 149 by means of screws (see Figure 2B). A helical spring 150 is fixed at one end to the inside of the bottom of the sleeve 146 and the other end is secured to the enlarged cylindrical portion 145c of the spindle. This spring biases the spindle 145 upwardly as seen in Figure 2B, and also normally causes the reed switch (Figure 2A) to be shielded magnetically by a shield plate 151 affixed to the spindle 145. This plate 151, when in the position shown, shields the reed switch from the field of a permanent magnet 147 which, when the plate 151 is moved away, actuates the switch. In Figure 2B, referenced 152, is a portion of the frame of the timepiece.

Referring now to the circuit diagram of Figure 1, suppose that the switches 42 and 43 are both open. The switch 43 will be open when the shield plate 151 is in the position shown in Figure 2A and shields the reed switch from the magnetic field of the magnet 147. Also assume the flip-flops 34, 36 and 37 to be in their reset states.

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The 4Hz pulse output from the frequency divider 5 is supplied through resistance 41 to one input of the NAND gate 9 and also through the inverter 23 to one input of the NAND gate 10. The 4Hz pulse output from divider 5, inverted by the inverter 22, is also applied to the remaining input of gate 9, while the remaining input of gate 10 receives the said 4Hz output directly. The outputs of the gates 9 and 10 will therefore be maintained at logic "1": the data input terminals D of the flip-flops 30 and 32 will be at "1", and the clock inputs CP of said flip-flops will receive pulses as will be explained later.

The 16Hz pulse output from divider 3 is delivered to one input of NAND gate 20 through the inverter 26, while the 8Hz pulse output from the frequency divider 4 is supplied directly to the remaining input of gate 20.

The wave forms occurring at points *a* and *b* of Figure 1 are as represented at A and B respectively in Figure 3 and a wave form as shown at C in Figure 3 appears at the output *c* of the inverter 27, and is delivered to one input of each of the NAND gates 11 and 12. The remaining input of gate 11 receives the 4Hz pulse output from divider 5 after inversion by the inverter 22, while the remaining input of gate 12 receives said 4Hz pulse output directly. A pulse output as shown at E in Figure 3 therefore appears at the output terminal *e* of the inverter 24; and this is supplied to the clock inputs CP of the flip-flops 31 and 32. Also a pulse output as shown at F in Figure 3 is obtained at the output terminal *f* of the inverter 25, and this is delivered to the clock inputs of the flip-flops 30, 33 and 35.

Since the outputs of the gates 9 and 10 are at "1", the $\bar{Q}$ outputs of the flip-flops 30 and 32 become "0" when pulses are supplied to their clock inputs CP. When the $\bar{Q}$ outputs of 32 becomes "0" the NAND gate 19 is closed and cannot pass any pulses reaching it via either of its other inputs. Accordingly the speaker 39 can receive no input and cannot sound an alarm. The $\bar{Q}$ output from the flip-flop 32, being "0", also keeps the output of the AND gate 13 at "0".

With the data inputs D of the flip-flops 31 and 33 at "0", the $\bar{Q}$ outputs of these flip-flops at "1", and the $\bar{Q}$ outputs of the flip-flops 30 and 32 also at "0", the data input D of the flip-flop 35 is "1" and the $\bar{Q}$ output thereof is "1" when a pulse is supplied to its clock input CP. This opens the AND gate 16 which accordingly passes the

pulse fed to said gate through the inverter 22 to the set terminal S of the flip-flop 34, the Q output of which thus becomes "1".

In this condition, when the reference switch 42 is closed by a time mechanism at a previously set time, the connection point *p* becomes "1", because the resistance 40 is of much smaller value than the resistance 41, and that input of NAND gate 9 connected to point *p* is also at "1" and this gate passes the pulses from the output of frequency divider 5 (see line D of Figure 3).

Meanwhile, since point *p* is "1", one input of NAND gate 10 is at "0", and its output is "1". When a pulse as shown in line E of Figure 3 is fed out from the inverter 24, during the period in which the pulse from the NAND gate 9 keeps the data input

D of the flip-flop 32 at "0", the $\bar{Q}$ output of the flip-flop 32 is inverted to "1" keeping one input of the three-input NAND gate

19 at "1". Consequently, as the $\bar{Q}$ and Q outputs of the respective flip-flops 33 and 34 are at "1", the output of the AND gate 13 is "1". When a pulse as shown in line F of Figure 3 appears at the output of the

inverter 25, the $\bar{Q}$ output of the flip-flop 33 becomes "0" resulting in a pulse at the output of the AND gate 13. This is applied to the set terminal S of the flip-flop 37, setting it, and is also applied, through the OR gate 17, to the reset terminals R of the flip-flop 36 and the counter 7, resetting both. The NAND gate 19 is opened by the Q output of the flip-flop 37 and accordingly a pulse of several KHz at a period of $\frac{1}{2}$ second is delivered via the NAND gate 18, the inverter 28, the gate 19, and the inverter 29 to the amplifier 38, so that an alarm sound is produced by the speaker 39.

The resetting of the flip-flop 36 causes its Q output to open the NAND gate 21, thus allowing the 1Hz pulses from the frequency divider 6 to pass to the counter 7. This counter 7 counts five minutes, after the elapse of which its output is supplied to the clock input CP of the flip-flop circuit 37,

to invert the levels of its Q and $\bar{Q}$ outputs. Consequently, the NAND gate 19 is closed,

stopping the alarm sound, and the Q output of the flip-flop 36 becomes "0", thus closing the NAND gate 21 and stopping the further supply of pulses to the counter 7.

It will be seen, therefore, that, when the preset time is reached, and the reference switch 42 is closed, the alarm sounds and stops 5 minutes later. It is, of course, not essential for the automatic time of con-

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5 continuation of the alarm sound to be 5 minutes, for obviously it can be arranged for this automatic time of continuation to be anything desired by suitably choosing the time of count of the counter 7.

10 Means are provided for manually stopping the alarm sound, if desired, without waiting until the end of the automatic continuation time—in the above example, 5 minutes. Assume that the reference switch 42 has closed and the alarm sound has commenced. If now the manually operated switch 43 is closed, i.e. the push button 144 of Figure 2A is depressed, the shield plate 151 is moved downwardly (as seen in Figure 2A) and allows the magnet 147 to close the reed switch. Consequently the point *p* is kept at "0", and the output of gate 9 at "1". The "0" potential at *p* is inverted to "1" by the inverter 23, and gate 10 opens passing pulses as shown at D in Figure 3. The output of gate 9 keeps the data input terminal of flip-flop 32 at "1" and conse-

25 quently the Q output becomes "0" when a pulse as shown at E of Figure 3 appears at the output of the inverter 24. Because a D-type flip-flop produces a logic output depending on the logic input at its D input terminal when a clock pulse is applied to its clock input terminal, the gate 19 is closed

30 when the Q output of flip-flop 32 becomes "0" and the alarm stops. In addition the data input terminal D of the flip-flop 30 becomes "0" when the output from the gate 10 becomes "0". Thus when a pulse as shown at F in Figure 3 is supplied to the flip-flop 30 from the inverter 25, the Q output of the flip-flop 30 becomes "1".

40 Since the Q output of the flip-flop 31 is kept at "1" until a pulse as shown at E in Figure 3 is supplied from the inverter 24, the output of the gate 14 remains at "1" during this period. Consequently, the flip-flop 37 is reset and inverts its output to "0", thereby keeping the input of the gate 19 at "0". The "1" output from the gate 14 resets the counter 7 and the flip-flop 36 through the OR gate 17. The counter 7 therefore commences time counting at this instant.

50 Meanwhile, by reason of inversion of the Q output of the flip-flop 30, the gate 15 is opened to allow a pulse as shown at D in Figure 3 to pass therethrough. Accordingly, the flip-flop 34 is reset to invert its output to "0", and close the gate 13. If now the manually operated switch 43 is again opened, the point *p* becomes "1" again, the outputs of the flip-flops 30 and 32 become

"0" and "1" respectively, and one input of the gate 13 becomes "1". However, since this gate 13 is closed by the "0" output from the flip-flop 34, the flip-flop 37 is in the reset state, so that the gate 19 is still kept closed.

70 When the counter 7 has counted 5 minutes, its output is supplied to the clock input CP of the flip-flop 37, the levels of the Q and

75 Q outputs are inverted, the gate 19 opens and the alarm sounds. At this time, the flip-flop 36 is still in the reset condition so that the gate 21 is open and the pulse supply to the counter 7 continues. When the next 5 minutes has been counted, the counter output is again supplied to the clock input CP of the flip-flop 37 which in turn provides an output to close the gate 19, thus stopping

80 the alarm sound. Meanwhile, the Q output from the flip-flop 37 is supplied to the clock input CP of the flip-flop 36 whose Q output then acts to close the gate 21.

90 The alarm can be sounded at will at any time. This is convenient in practice, for example to enable a salesman to demonstrate the alarm timepiece to a customer in a shop. This can be done by operating the reference switch 42 as follows:— If the reference switch 42 is opened after the alarm has been temporarily suspended, the flip-flops 30 and 35 will assume their initial states and subsequent closing of the said switch 42 will cause

100 the Q output from the flip-flop 32 to become "1", so that a pulse is produced from the gate 13 thus setting the flip-flop 37 to open the gate 19 to allow the alarm to sound. As already described, the alarm sound can be stopped temporarily and will become available five minutes later, by closing and then re-opening the manually operable switch 43. In addition, the alarm can be sounded at will at any time by opening and closing the reference switch 42 after a temporary suspension of the alarm.

110 The duration of the generation of the alarm sound is controlled by the count time of the counter 7. Therefore only one counter is needed, a fact which contributes to the simplicity of the whole timepiece.

120 For putting the alarm completely out of action the manually operable switch 43 is kept closed. To achieve this with the switch arrangement shown in Figure 2A, the push button 144 is depressed to bring the upper sides of the projections 145a and 145b on the spindle 145 slightly below the level of the bottoms of the recesses 146a and 146b on the sleeve 146, and the spindle is then rotated through an angle until the said projections 145a and 145b abut against the step 146c in the sleeve 146. If pressure is

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then taken off the button 144 the spindle will be held in its lowered position and the shielding plate 151 will remain lowered out of the space between the magnet 147 and the reed switch. This switch therefore will stay

closed preserving a "0" state at the $\bar{Q}$ output of the flip-flop 32 and maintaining the gate 19 closed so that the alarm cannot sound.

Figure 4 shows a modification. In this figure references 44 to 51 are flip-flops, 52 to 60 are gates and 61 is an inverter, similar references denoting similar parts in Figures 1 and 4.

In operation with Figure 4, when the reference and the manually operable switches 42 and 43 are both opened, 4Hz pulses as shown at D in Figure 3 appear at point p and are applied to the data inputs D of the flip-flops 44 and 45. The clock input terminals CP of these flip-flops are supplied, from the respective terminals f and e , with clock pulses as shown respectively at F and E in Figure 3. As the clock pulses are applied to said flip-flops 44 and 45 when the data input terminals thereof are "1" and "0" respectively, the Q outputs of those flip-flops become "1" and "0" respectively. As clock pulses are also supplied from point e to the flip-flop 47 in the condition that the Q output of the flip-flop 44 is "1", the Q output of the flip-flop 47 becomes "1", so that one input of the three-input NAND gate 52 is also "1".

However, as clock pulses are also supplied from point e to the clock input terminal CP of the flip-flop 46 in the conditions that the

Q output of the flip-flop 45 is at "0", the $\bar{Q}$ output of said flip-flop 46 is at "1", keeping another input of the gate 52 at "1". At

this time, since the $\bar{Q}$ output of the flip-flop 45 is at "1", all three inputs of the said gate 52 are at "1", so that the output of this gate is at "0". Therefore, the outputs of the NAND gate 55 and of the inverter 61 are "1" and "0" respectively. Meanwhile, the

Q output of the flip-flop 45 causes the outputs of the AND gates 53 and 56 to be "0". Therefore, both inputs of the OR gate 57 are "0" so that this gate as a "0" output. Consequently, the Q output of the flip-flop circuit 48 is turned to "0" by a clock pulse produced at the point e , one input of the four-input NAND gate 19 is kept at "0", and pulses which have passed the inverter 28 cannot pass the gate 19, so that no alarm can be sounded by the speaker 39. Since the Q output of the flip-flop 48 is supplied to the data input terminal D of the

flip-flop 49, the Q output of flip-flop 49 becomes "1" when a pulse is produced at

the point e , thus making one input of the AND gate 58 "1". Again, since the output of the flip-flop 45 acts to keep the output of

the AND gate 54 at "0", the Q and $\bar{Q}$ outputs of the flip-flop 50 are kept at "0" and "1" respectively.

The foregoing describes the position when the reference and the manually operable switches 42 and 43 are both open. When the reference switch 42 closes at a previously set time, the point p becomes "1". Consequently, when a clock pulse is supplied

to the flip-flop 45, its Q and $\bar{Q}$ outputs become "1" and "0" respectively. Meanwhile

the Q and $\bar{Q}$ outputs of the flip-flop 44 are kept at "1" and "0" respectively, both inputs of the AND gate 53 become "1" and its output inverts to "1". As a result, the output of the AND gate 56 becomes "1" and, acting through the OR gate 57, turns the data input terminal D of the flip-flop 48 to "1". Subsequent supply of clock pulses from point e to the clock terminal CP of the flip-flop 48 causes the Q output of this flip-flop to become "1", thus supplying a "1" to one of the inputs of each of the two gates 19 and 55. The pulses from point e are also applied to the clock input terminal CP of

the flip-flop 46, turning its $\bar{Q}$ output to "0" and the output of gate 52 to "1" so that the output of gate 55 becomes "0". Therefore, the output of inverter 61 becomes "1", making the data input terminal D of the flip-flop 48 "1" via the OR gate 57. Accordingly the output of the said flip-flop 48 is kept at "1", thus in effect "storing" the closing of the reference switch 42. Meanwhile, the inversion of the level of the Q output of the flip-flop 48 causes the output of the gate 58 to become "1", the output of the said gate remaining at "1" until the next clock pulse is supplied to the flip-flop 49 from the point e .

The flip-flop 51 is reset by the output of the gate 58 and its $\bar{Q}$ output becomes "1", thereby making one of the inputs of the gate

19 "1". Meanwhile, since the Q output of the flip-flop 50 is at "1", the gate 19 is opened and pulses from the inverter 28 pass this gate and cause the speaker 39 to sound the alarm.

The output of the gate 58 resets the counter 7 and the flip-flop 36 through the

OR gate 60. The Q output of the flip-flop 36 opens the gate 21 and 1Hz pulses from the divider 6 are counted by the counter 7.

Then, in the manner already described with reference to Figure 1, the counter 7

counts for five minutes and its output is then supplied to the input of the flip-flop 51 and causes the alarm sound to stop.

The operation initiated by opening the manually operable switch 43, after closing the same, subsequent to the closing of the reference switch 42, will now be described.

When the switch 43 is closed, after the reference switch 42 is closed to allow an alarm to be sounded, the point *p* becomes

"0". This causes the *Q* and $\bar{Q}$ outputs of the flip-flops 45 and 44 to be made "0" and "1" respectively, by the clock pulses delivered from the points *e* and *f*. Consequently, the output of the gate 54 becomes

"1", so that the *Q* and $\bar{Q}$ outputs of the flip-flop 50 are turned to "1" and "0" respectively, by the clock pulses from the point *e*.

The $\bar{Q}$ output from flip-flop 50 causes one input of the gate 19 to become "0", so that the alarm sound is stopped.

Meanwhile, the inverted *Q* output of the flip-flop 50 inverts the output level of the AND gate 59, thus setting the flip-flop 51, to the set terminal *S* of which the output of said AND gate is connected. This results in one input of the gate 19 being kept at "0". The output of the gate 59 also resets the counter 7 and the flip-flop 36, via the OR gate 60, while the flip-flops 48 and 49 remain unchanged in state due to the output of the OR gate 57.

Subsequent opening of the switch 43 causes the flip-flops 44 to 47 and the flip-flop 50 to return to the states in which they were when only the reference switch 42 was closed. However, the states of the flip-flops 48 and 49 are not changed. Therefore, the flip-flop 51 retains its set state and con-

tinues to have a $\bar{Q}$ output of "0". The gate 19 is accordingly kept closed and the alarm cannot sound. Meanwhile, by the above described return of the flip-flop 50 to its previous state, the output levels of the gates 59 and 60 invert, putting an end to the reset states of the counter 7 and of the flip-flop 36, and allowing the counter 7 to commence counting.

The sounding of the alarm is held off, until the counter 7 counts five minutes, similarly to the action which takes place with Figure 1. When the five minutes have been counted by the counter 7, the output therefrom inverts, the output of the flip-flop 51, the gate 19 opens and the alarm is sounded.

For rendering the alarm completely out of action, the manually operable switch 43 is kept closed, as with the case of the embodiment of Figure 1. As will be seen, if

this is done the $\bar{Q}$ output of the flip-flop 50

is kept at "0", thus keeping the gate 19 closed and holding the alarm out of action.

As will now be appreciated, the states of the switches 42 and 43 are, in effect, detected and responded to by the outputs of the flip-flops 44 and 45 which are supplied directly with the output obtained at the point *p*, so as to control the operation of the alarm.

It may be noted here that an equivalent effect could be obtained by modifying the circuit of Figure 1 by directly connecting the point *p* to the flip-flop 30, omitting the gates 9 and 10, connecting the inverter 23 directly to the flip-flop 32, and applying clock pulses from the points *e* and *f* to the flip-flops 30 and 32 respectively.

As will now be understood, the illustrated embodiments of the invention have the great practical advantage where integrated circuitry is employed, that because control of the alarm is effected by the state of the signal at the point *p*, only a single external lead (from the said point *p*) is required to be taken off from the integrated circuitry for the purpose of making connection to the output sides of the reference and manually operable switches 42 and 43.

In addition, since the reference switch used in a conventional alarm timepiece is usually connected to the electric supply source, it is a relatively simple matter to modify such conventional alarm timepieces into alarm timepieces in accordance with the invention using the conventional reference switch without substantial change.

Thus, to sum up, due to the provision, in the preferred way of carrying out the invention, of a common connection terminal at the output sides of the two switches and of two different respective voltage levels and controlling the generation of an alarm sound by the detection of the voltage level at the common connection terminal, the switching states of the switches can be detected, a minimum number of switches being required. This is of great practical importance from the point of view of integrating the circuitry, because the number of external connection pins required in the circuitry can be reduced to a minimum with consequent improved miniaturisation of the circuitry.

Although not limited to its application thereto, the invention is most advantageously applicable to compact, small, timepieces (not excluding watches), providing as it does the advantage of enabling a variety of alarm operation modes to be obtained by means of a minimum number of switches and connections thereto from the circuitry. In addition, because of the reduced number of external connections required to be made to the integrated circuitry, the said circuitry is much better protected against interference by externally produced electrostatic

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discharges and effects, and possible damage to semi-conductor elements in the circuitry by such discharges and effects than is the circuitry of conventional comparable integrated circuit alarm timepieces in which a considerable number of external connections are made to the integrated circuitry.

WHAT WE CLAIM IS: —

- 10 1. An electronic alarm timepiece including a switch arranged to be operated by time actuated means; a manually operable switch; means for producing at a connection point in a circuit common to both
15 switches different potentials representative of different operation states of said switches; a pulse generating circuit for producing a plurality of clock pulse trains; circuit means controlled by the potential at said connection point and by one of said pulse trains
20 for producing different outputs representative of the different operation states; means for producing an alarm sound; and control means for controlling said sound producing means by an output from said circuit means.
25 2. A timepiece as claimed in claim 1 wherein said connection point is common to both switches.
3. A timepiece as claimed in claim 2
30 wherein, to produce said different potentials at said connection point, said time actuated switch and said manually operable switch are connected in series, one of said terminals of the time actuated switch being

connected to a point of one predetermined potential, while one of the terminals of the manually operable switch is connected to a point of different predetermined potential, the said connection point being the function between the two switches.

4. A timepiece as claimed in any of the preceding claims having a time standard oscillator and a chain of frequency dividers dividing down the output of said oscillator to produce a relatively low frequency pulse train driving the time display of said timepiece wherein signals for driving the alarm sound producing means and employed for controlling the operation thereof are derived from points in said divider chain.

5. A timepiece as claimed in any of the preceding claims wherein the manually operable switch is a magnetically responsive reed switch mounted adjacent a permanent magnet and arranged to be actuated by moving a magnetic shield into or out of a position in which it shields the switch from the field of the magnet.

6. Electronic alarm timepieces substantially as herein described with reference to the accompanying drawings.

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discharges and effects, and possible damage to semi-conductor elements in the circuitry by such discharges and effects than is the circuitry of conventional comparable integrated circuit alarm timepieces in which a considerable number of external connections are made to the integrated circuitry.

WHAT WE CLAIM IS: —

1. An electronic alarm timepiece including a switch arranged to be operated by time actuated means; a manually operable switch; means for producing at a connection point in a circuit common to both switches different potentials representative of different operation states of said switches; a pulse generating circuit for producing a plurality of clock pulse trains; circuit means controlled by the potential at said connection point and by one of said pulse trains for producing different outputs representative of the different operation states; means for producing an alarm sound; and control means for controlling said sound producing means by an output from said circuit means.
2. A timepiece as claimed in claim 1 wherein said connection point is common to both switches.
3. A timepiece as claimed in claim 2 wherein, to produce said different potentials at said connection point, said time actuated switch and said manually operable switch are connected in series, one of said terminals of the time actuated switch being

connected to a point of one predetermined potential, while one of the terminals of the manually operable switch is connected to a point of different predetermined potential, the said connection point being the function between the two switches.

4. A timepiece as claimed in any of the preceding claims having a time standard oscillator and a chain of frequency dividers dividing down the output of said oscillator to produce a relatively low frequency pulse train driving the time display of said timepiece wherein signals for driving the alarm sound producing means and employed for controlling the operation thereof are derived from points in said divider chain.

5. A timepiece as claimed in any of the preceding claims wherein the manually operable switch is a magnetically responsive reed switch mounted adjacent a permanent magnet and arranged to be actuated by moving a magnetic shield into or out of a position in which it shields the switch from the field of the magnet.

6. Electronic alarm timepieces substantially as herein described with reference to the accompanying drawings.

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