FIG. 1

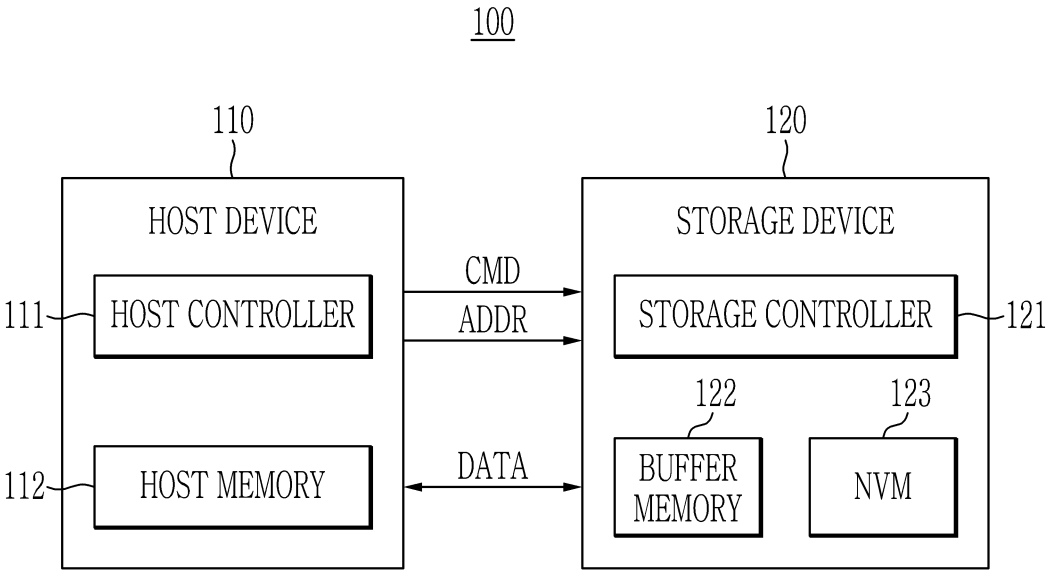

100
110
120
HOST DEVICE
STORAGE DEVICE
CMD
ADDR
111
HOST CONTROLLER
STORAGE CONTROLLER
121
122
123
112
HOST MEMORY
DATA
BUFFER MEMORY
NVM

FIG. 2

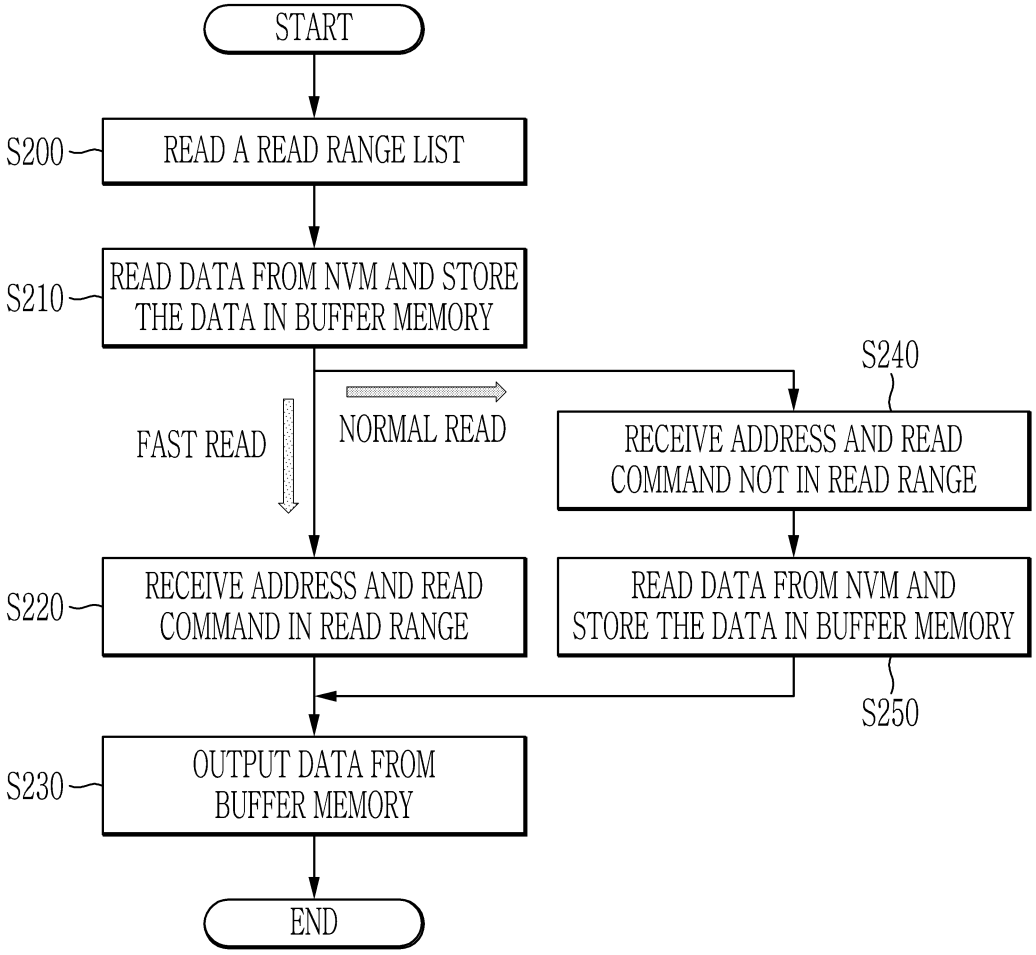

START
S200
READ A READ RANGE LIST
S210
READ DATA FROM NVM AND STORE THE DATA IN BUFFER MEMORY
FAST READ
NORMAL READ
S240
RECEIVE ADDRESS AND READ COMMAND NOT IN READ RANGE
S220
RECEIVE ADDRESS AND READ COMMAND IN READ RANGE
READ DATA FROM NVM AND STORE THE DATA IN BUFFER MEMORY
S250
S230
OUTPUT DATA FROM BUFFER MEMORY
END

FIG. 3

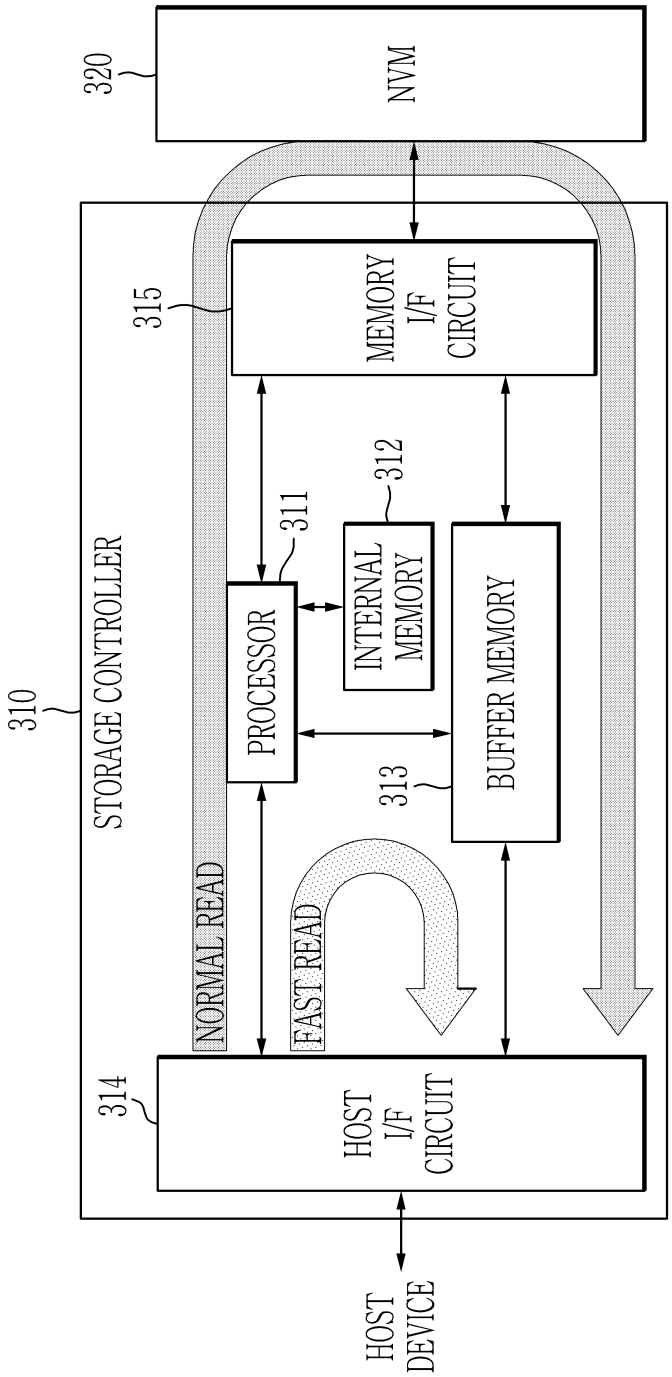

300
310
STORAGE CONTROLLER
320
NVM
315
MEMORY I/F CIRCUIT
311
PROCESSOR
312
INTERNAL MEMORY
313
BUFFER MEMORY
NORMAL READ
FAST READ
314
HOST I/F CIRCUIT
HOST DEVICE

FIG. 4

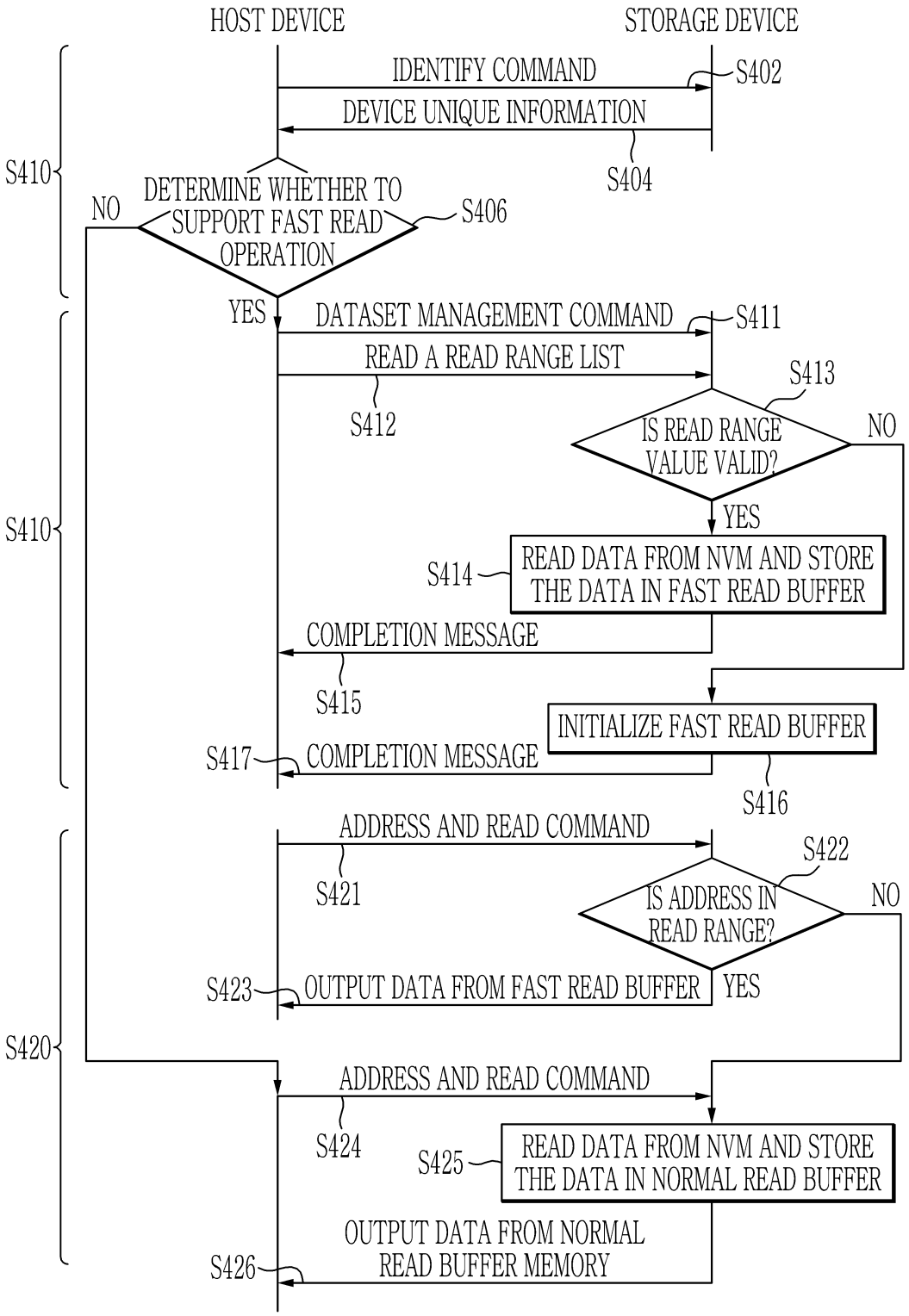

HOST DEVICE
STORAGE DEVICE
IDENTIFY COMMAND
S402
DEVICE UNIQUE INFORMATION
S404
S410
DETERMINE WHETHER TO SUPPORT FAST READ OPERATION
S406
NO
YES
DATASET MANAGEMENT COMMAND
S411
READ A READ RANGE LIST
S412
S413
IS READ RANGE VALUE VALID?
NO
YES
S410
S414
READ DATA FROM NVM AND STORE THE DATA IN FAST READ BUFFER
COMPLETION MESSAGE
S415
INITIALIZE FAST READ BUFFER
S417
COMPLETION MESSAGE
S416
ADDRESS AND READ COMMAND
S421
S422
IS ADDRESS IN READ RANGE?
NO
S423
OUTPUT DATA FROM FAST READ BUFFER
YES
S420
ADDRESS AND READ COMMAND
S424
S425
READ DATA FROM NVM AND STORE THE DATA IN NORMAL READ BUFFER
OUTPUT DATA FROM NORMAL READ BUFFER MEMORY
S426

FIG. 5

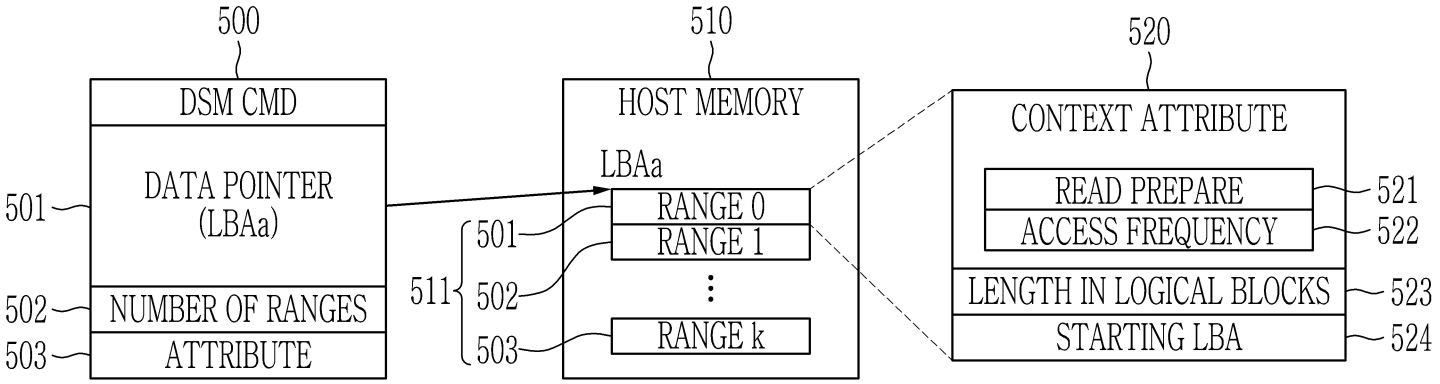

500
DSM CMD
DATA POINTER
(LBAa)
501
NUMBER OF RANGES
502
ATTRIBUTE
503
510
HOST MEMORY
LBAa
RANGE 0
RANGE 1
RANGE k
511
501
502
503
520
CONTEXT ATTRIBUTE
READ PREPARE
ACCESS FREQUENCY
LENGTH IN LOGICAL BLOCKS
STARTING LBA
521
522
523
524

FIG. 6

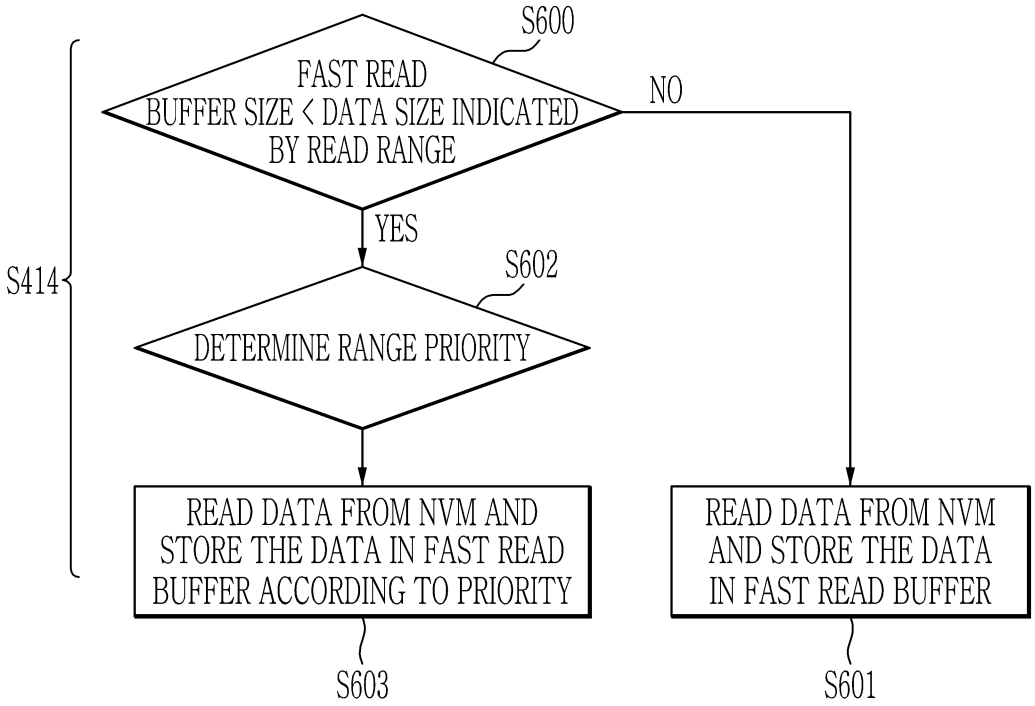

S600
FAST READ
BUFFER SIZE < DATA SIZE INDICATED BY READ RANGE
NO
YES
S414
S602
DETERMINE RANGE PRIORITY
READ DATA FROM NVM AND STORE THE DATA IN FAST READ BUFFER ACCORDING TO PRIORITY
READ DATA FROM NVM AND STORE THE DATA IN FAST READ BUFFER
S603
S601

FIG. 7

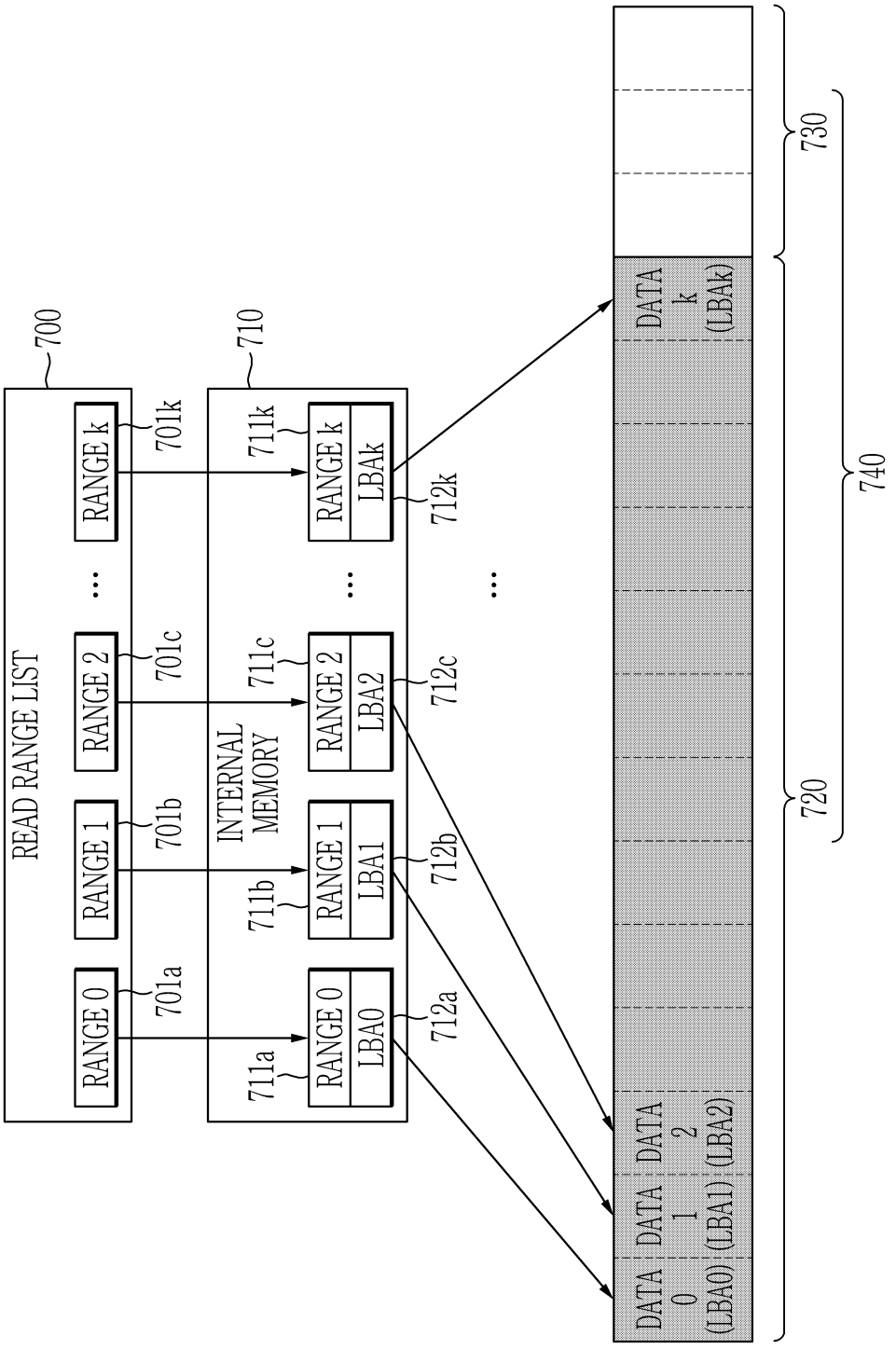

700
READ RANGE LIST
RANGE 0
RANGE 1
RANGE 2
RANGE k
701a
701b
701c
701k
710
INTERNAL MEMORY
711a
711b
711c
711k
RANGE 0
LBA0
RANGE 1
LBA1
RANGE 2
LBA2
RANGE k
LBAk
712a
712b
712c
712k
DATA 0 (LBA0)
DATA 1 (LBA1)
DATA 2 (LBA2)
DATA k (LBAk)
720
730
740

FIG. 8

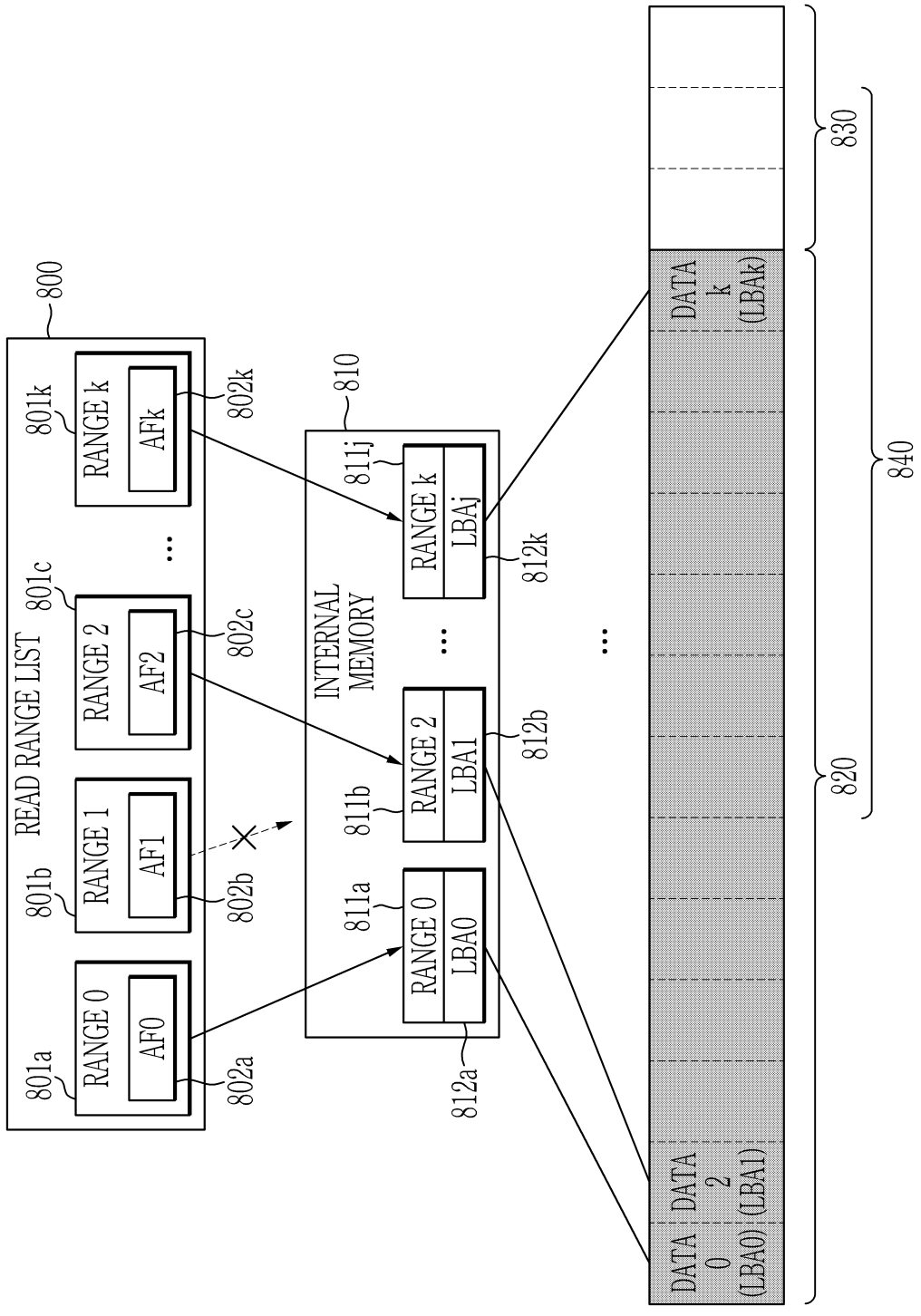

800
READ RANGE LIST
801a
RANGE 0
AF0
802a
801b
RANGE 1
AF1
802b
801c
RANGE 2
AF2
802c
...
801k
RANGE k
AFk
802k
INTERNAL MEMORY
810
811a
RANGE 0
LBA0
812a
811b
RANGE 2
LBA1
812b
...
811j
RANGE k
LBAj
812k
DATA 0 (LBA0)
DATA 2 (LBA1)
...
DATA k (LBAk)
820
830
840

FIG. 9

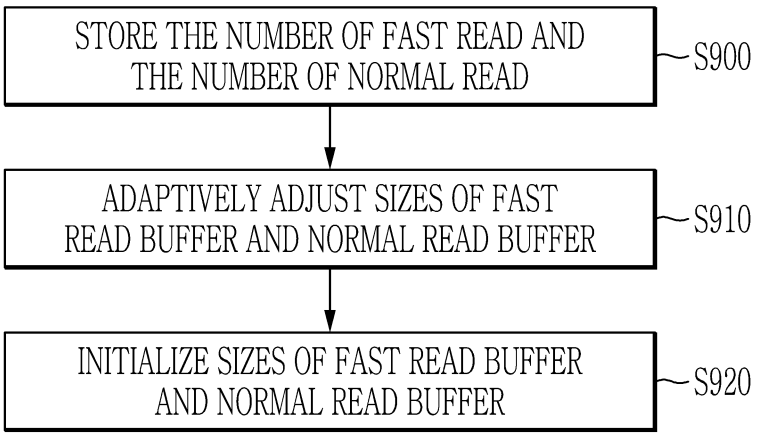

STORE THE NUMBER OF FAST READ AND THE NUMBER OF NORMAL READ
S900
ADAPTIVELY ADJUST SIZES OF FAST READ BUFFER AND NORMAL READ BUFFER
S910
INITIALIZE SIZES OF FAST READ BUFFER AND NORMAL READ BUFFER
S920

FIG. 10

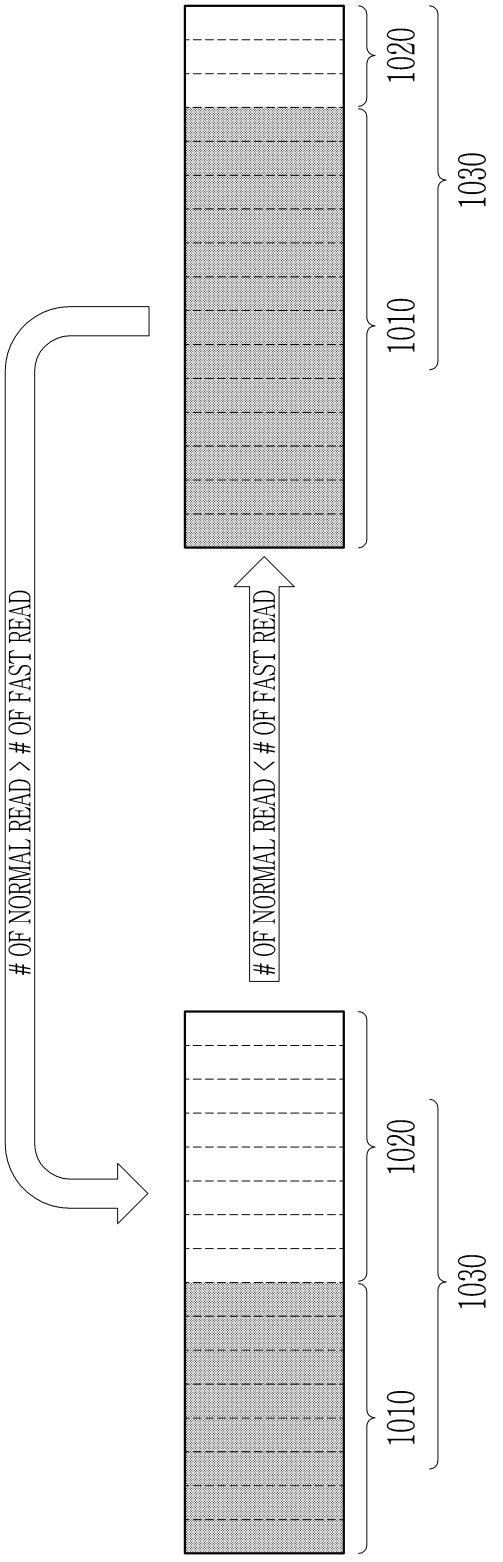

OF NORMAL READ > # OF FAST READ
OF NORMAL READ < # OF FAST READ
1020
1010
1030
1020
1010
1030

FIG. 11

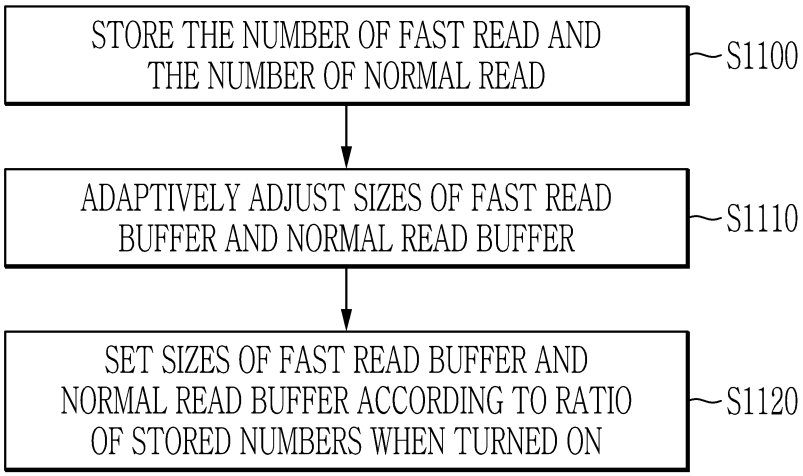

STORE THE NUMBER OF FAST READ AND THE NUMBER OF NORMAL READ
S1100
ADAPTIVELY ADJUST SIZES OF FAST READ BUFFER AND NORMAL READ BUFFER
S1110
SET SIZES OF FAST READ BUFFER AND NORMAL READ BUFFER ACCORDING TO RATIO OF STORED NUMBERS WHEN TURNED ON
S1120

FIG. 12

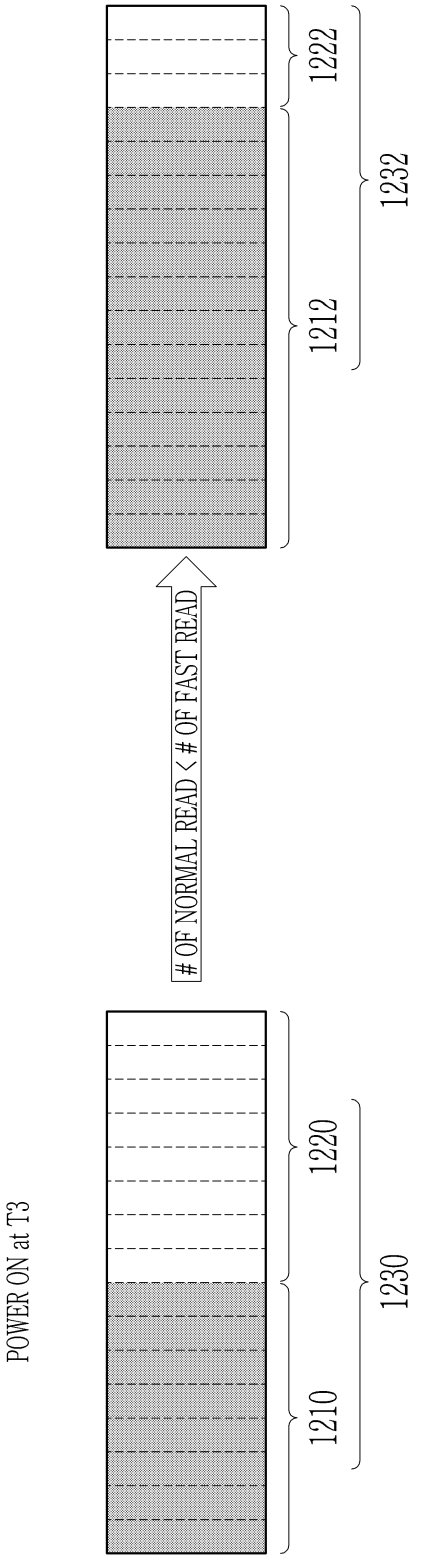

POWER ON at T3
1210
1220
1230
OF NORMAL READ < # OF FAST READ
1212
1222
1232

FIG. 13

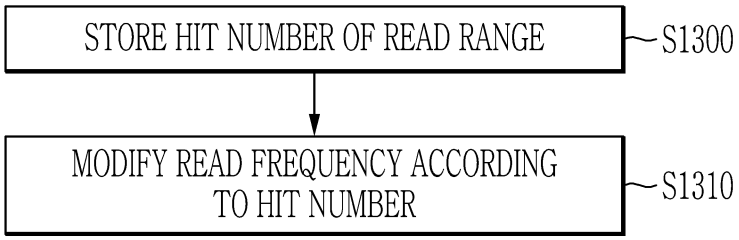

STORE HIT NUMBER OF READ RANGE
S1300
MODIFY READ FREQUENCY ACCORDING TO HIT NUMBER
S1310

FIG. 14

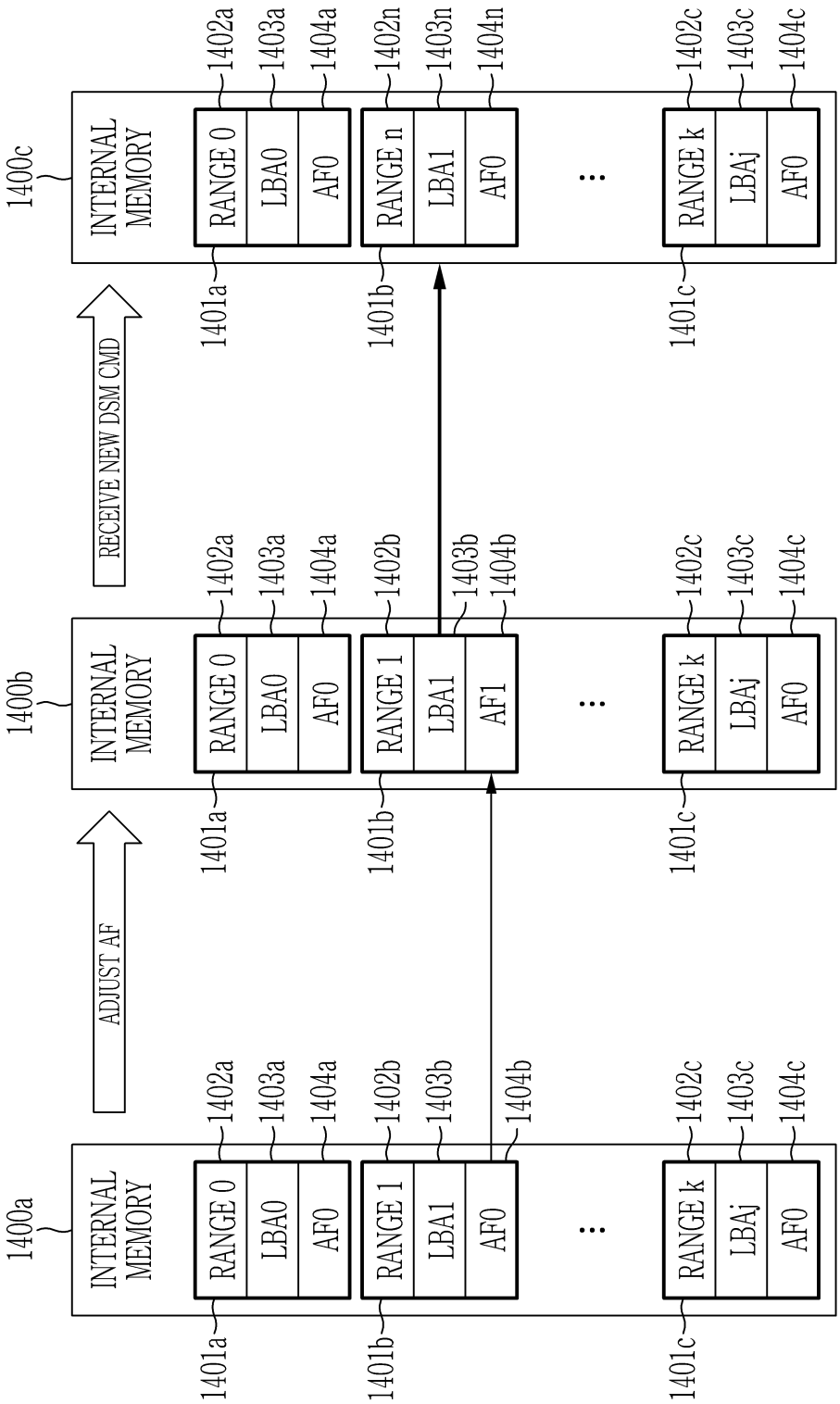

1400a
INTERNAL MEMORY
RANGE 0
LBA0
AF0
RANGE 1
LBA1
AF0
RANGE k
LBAj
AF0
1401a
1401b
1401c
1402a
1403a
1404a
1402b
1403b
1404b
1402c
1403c
1404c
ADJUST AF
1400b
INTERNAL MEMORY
RANGE 0
LBA0
AF0
RANGE 1
LBA1
AF1
RANGE k
LBAj
AF0
1401a
1401b
1401c
1402a
1403a
1404a
1402b
1403b
1404b
1402c
1403c
1404c
RECEIVE NEW DSM CMD
1400c
INTERNAL MEMORY
RANGE 0
LBA0
AF0
RANGE n
LBA1
AF0
RANGE k
LBAj
AF0
1401a
1401b
1401c
1402a
1403a
1404a
1402n
1403n
1404n
1402c
1403c
1404c

FIG. 15

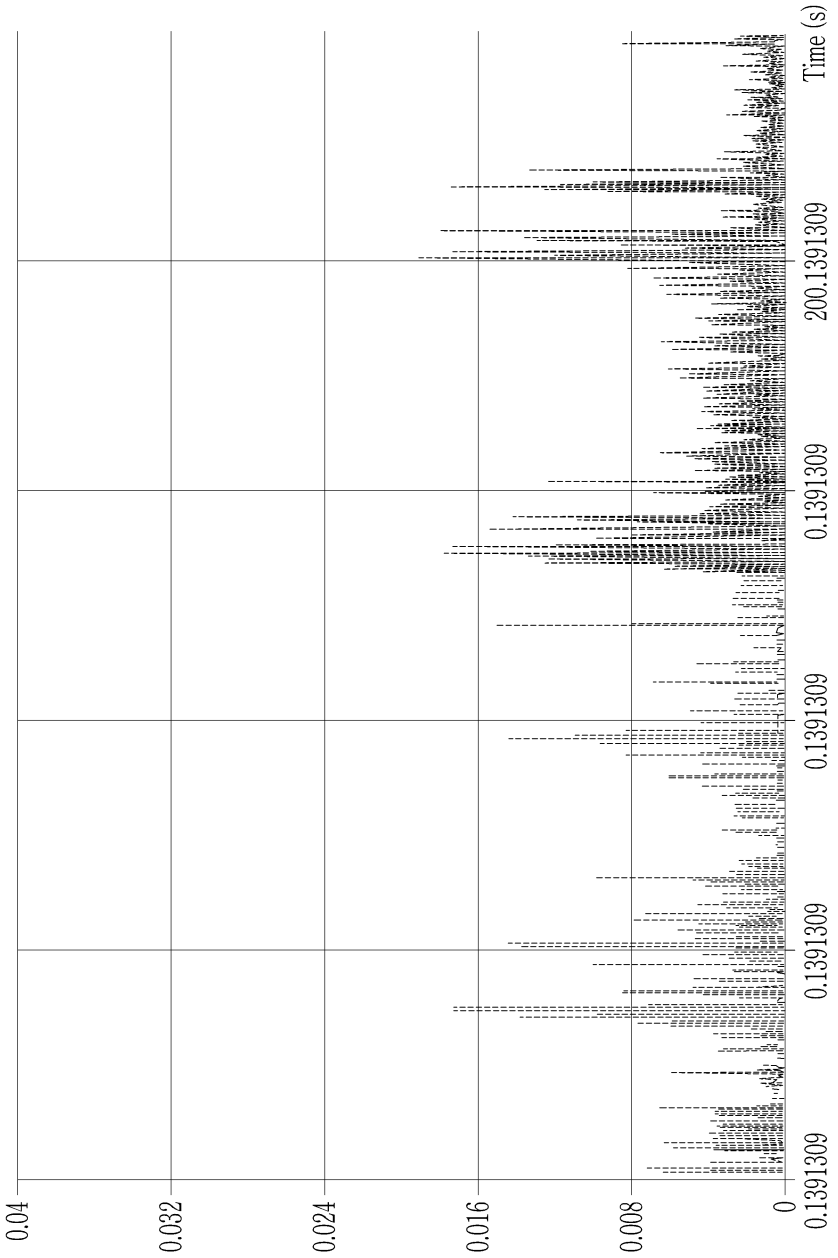

0.04
0.032
0.024
0.016
0.008
0
0.1391309
0.1391309
0.1391309
0.1391309
200.1391309
Time (s)

FIG. 16

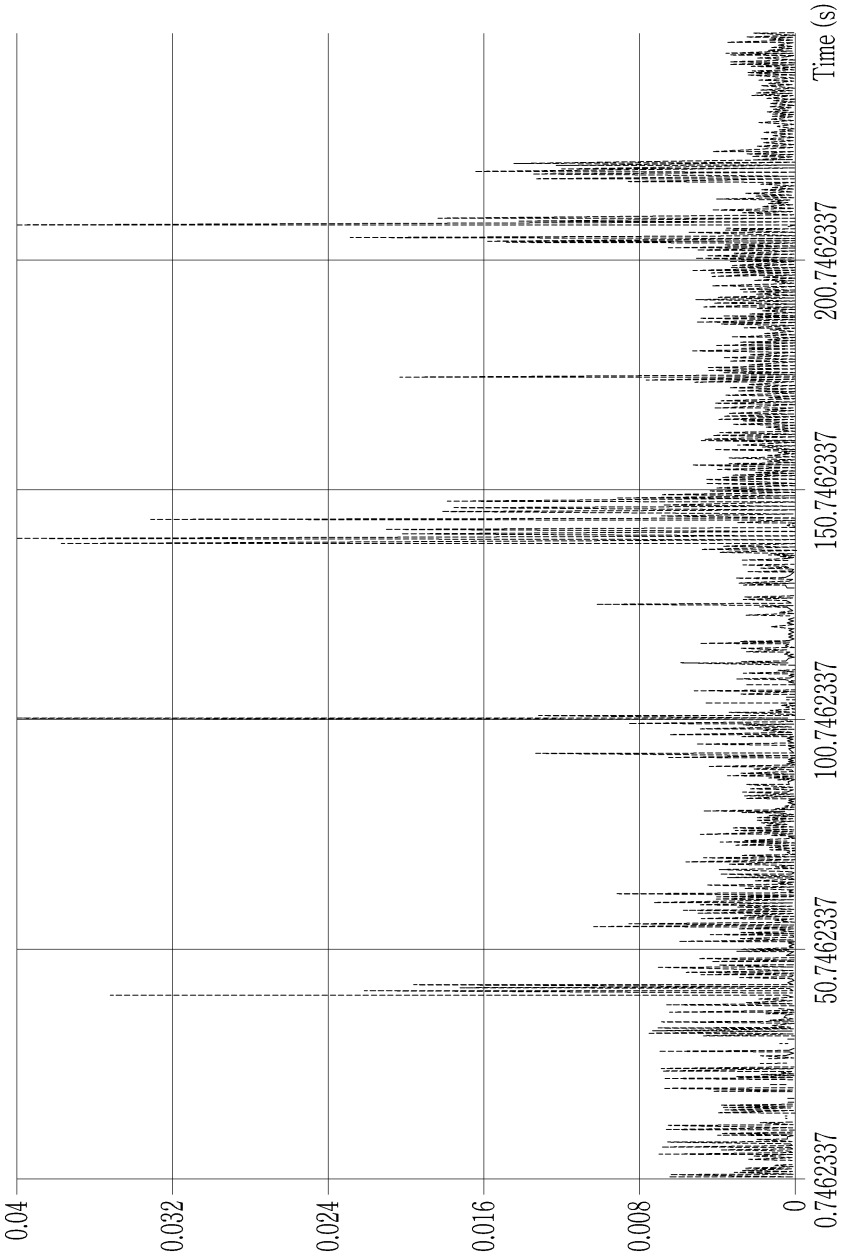

0.04
0.032
0.024
0.016
0.008
0
0.7462337
50.7462337
100.7462337
150.7462337
200.7462337
Time (s)

FIG. 17

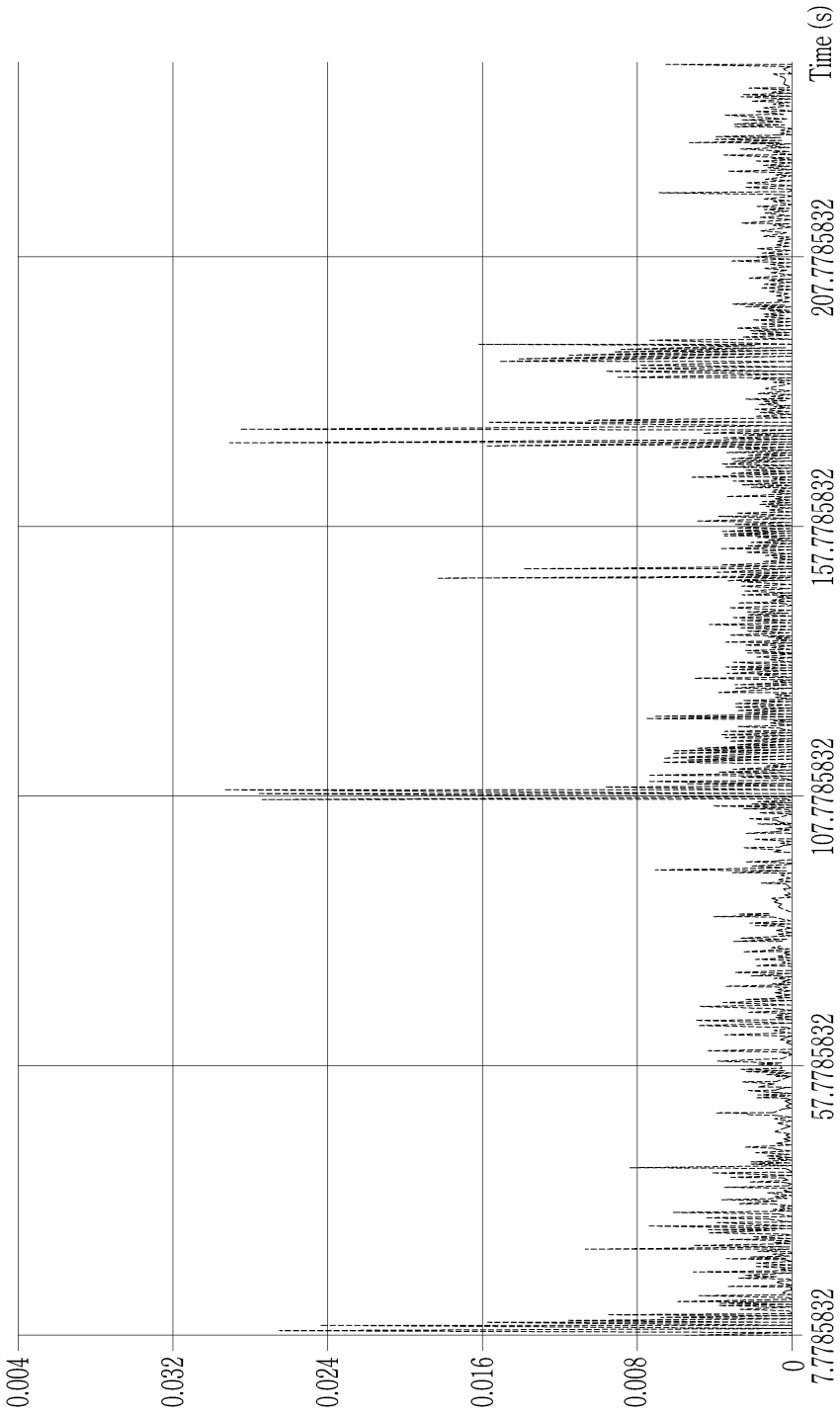
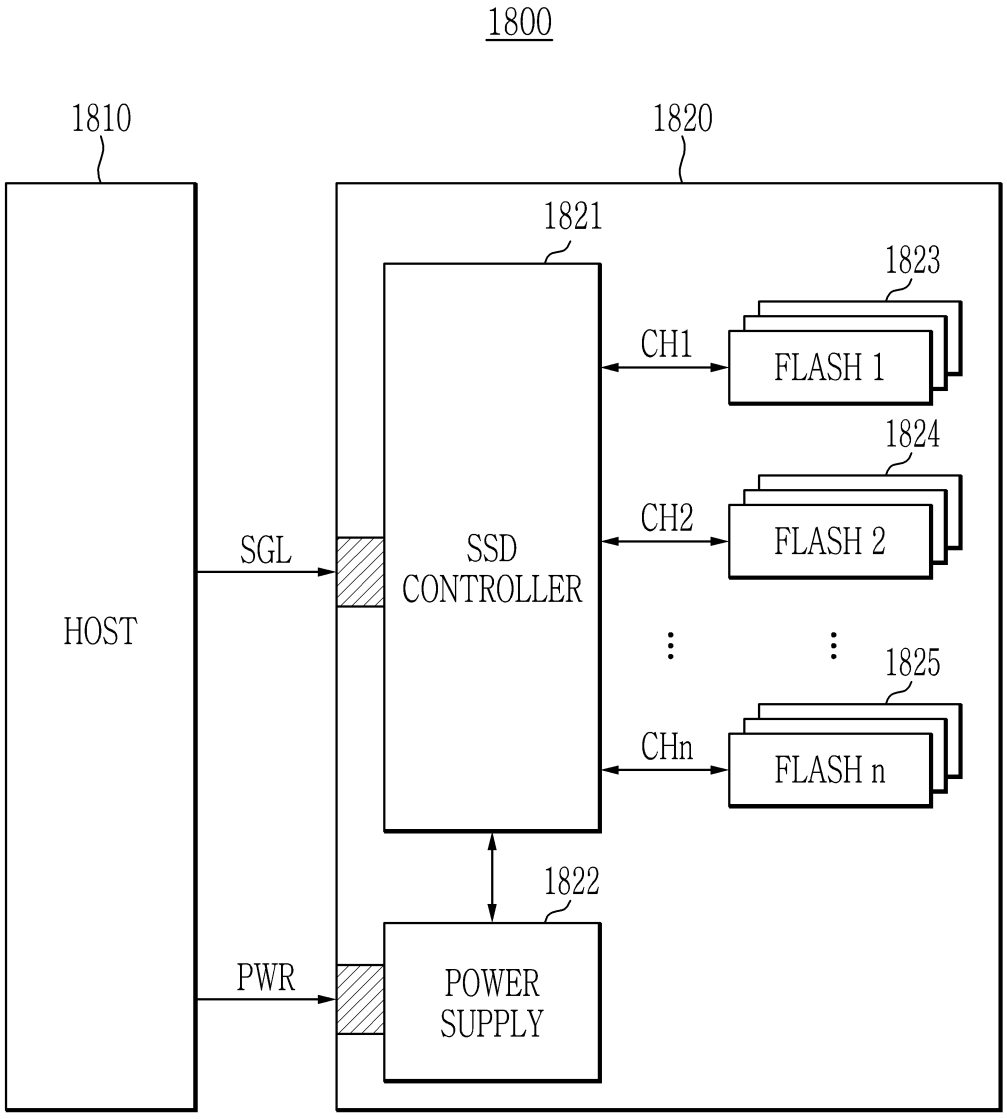

0.004
0.032
0.024
0.016
0.008
0
7.7785832
57.7785832
107.7785832
157.7785832
207.7785832
Time (s)

FIG. 18


1800
1810
1820
1821
1823
1824
1825
1822
HOST
SGL
PWR
SSD
CONTROLLER
POWER
SUPPLY
CH1
CH2
CHn
FLASH 1
FLASH 2
FLASH n