

HIGH PRESSURE ANNEALING PROCESS FOR METAL CONTAINING MATERIALS

BACKGROUND

Field

[0001] Embodiments of the present invention generally relate to a method for forming a metal containing layer in a film stack that may be utilized in TFT device structures, semiconductor, or memory applications.

Description of the Related Art

[0002] Display devices have been widely used for a wide range of electronic applications, such as TV, monitors, mobile phone, MP3 players, e-book readers, and personal digital assistants (PDAs) and the like. The display device is generally designed for producing desired image by applying an electric field to a liquid crystal that fills a gap between two substrates and has anisotropic dielectric constant that controls the intensity of the dielectric field. By adjusting the amount of light transmitted through the substrates, the light and image intensity, quality and power consumption may be efficiently controlled.

[0003] A variety of different display devices, such as active matrix liquid crystal display (AMLCD) or an active matrix organic light emitting diodes (AMOLED), may be employed as light sources for display devices which utilize touch screen panels. In the manufacturing of TFT devices, an electronic device with high electron mobility, low leakage current and high breakdown voltage, would allow more pixel area for light transmission and integration of circuitry, thus resulting in a brighter display, higher overall electrical efficiency, faster response time and higher resolution displays. Low film qualities of the material layers, such as metal electrode layer with impurities, formed in the device often result in poor device electrical performance and short service life of the devices. Thus, a stable and reliable method for forming and integrating film layers with in a TFT devices becomes crucial to provide a device structure with low film leakage, and high breakdown voltage, for use in manufacturing electronic

devices with lower threshold voltage shift and improved the overall performance of the electronic device are desired.

[0004] Therefore, there is a need for improved materials for manufacturing TFT devices that produce improved device electrical performance and device stability.

SUMMARY

[0005] The present disclosure provides methods for performing an annealing process on a metal containing layer in TFT display applications, semiconductor or resistive random access memory (ReRAM). In one example, a method of forming a metal containing layer on a substrate includes supplying an oxygen containing gas mixture on a substrate in a processing chamber, the substrate comprising a metal containing layer disposed on an optically transparent substrate, maintaining the oxygen containing gas mixture in the processing chamber at a process pressure between 2 bar and 50 bar, and thermally annealing the metal containing layer in the presence of the oxygen containing gas mixture.

[0006] In another example, a method for densifying a metal containing layer disposed on a substrate includes thermally treating a metal containing layer disposed on an optically transparent substrate at a pressure greater than 2 bar, and maintaining a substrate temperature less than 500 degrees Celsius during thermally treating the dielectric layer.

[0007] In yet another example, a method for densifying a metal containing layer disposed on a substrate includes forming a metal containing layer on a substrate, implanting dopants into the metal containing layer and thermally treating the metal containing layer on the substrate at a pressure greater than 2 bar while maintaining the substrate temperature less than 500 degrees Celsius.

DETAILED DESCRIPTION OF THE DRAWINGS

[0008] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments,

some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0009] Figure 1 is a simplified front cross-sectional view of a processing chamber with a cassette disposed therein in accordance with some embodiments;

[0010] Figure 2 is a cluster system that the processing chamber of Figure 1 may be incorporated thereto;

[0011] Figure 3 is a sectional view of one example of a thin film transistor device structure; and

[0012] Figure 4 is a sectional view of another example of a thin film transistor device structure.

[0013] Figure 5 depicts a flow diagram of an annealing process performed in a metal containing material in accordance with some embodiments;

[0014] Figures 6A-6D depict one embodiment of a sequence for thermal annealing the metal containing material of Figure 5 in accordance with some embodiments.

[0015] To facilitate understanding, identical reference numerals have been used, such as anneal at atmospheric pressure with similar anneal conditions where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

[0016] It is to be noted, however, that the appended drawings illustrate only exemplary embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

DETAILED DESCRIPTION

[0017] Embodiments of the disclosure generally provide a TFT device structures and methods of performing a thermal annealing process on an active layer of source, drain, interface and contact regions in the TFT device structures

so as to enhance electrical performance for display devices. Other applications, including semiconductor or memory device manufacturing process, may also utilize the embodiments described herein. The thermal annealing process may densify the active layer film properties of the metal electrodes, source/drain and/or contact regions, and/or film layers on the substrate. In one example, the thermal treatment process is performed to provide thermal energy of a metal containing layer, such as a metal containing layer (e.g., an active layer) or a metal electrode layer (e.g., a metal gate electrode, a source-drain and/or contact regions or electrode layers, or other suitable metal structures) is formed in the TFT devices. The thermal annealing process may densify or minimize oxygen deficiency in the active layer film structures to provide good quality, interface management and thermal stabilization to the device structure. The thermal annealing process may also increase the degree of crystalline of the metal containing material, improving electrical performance of the metal containing layer. Thus, desired film properties of metal electrodes and active layers of source/drain and/or contact regions in display devices may efficiently enhance the electrical performance of transistor and diode devices.

[0018] Figure 1 is a simplified front cross-sectional view of a single-substrate processing chamber 100 for a high-pressure annealing process of a single substrate. The single-substrate processing chamber 100 has a body 110 with an outer surface 112 and an inner surface 113 that encloses an internal volume 115. In some embodiments such as in Figure 1, the body 110 has an annular cross section, though in other embodiments the cross-section of the body 110 may be rectangular or any closed shape. The outer surface 112 of the body 110 may be made from a corrosion resistant steel (CRS), such as but not limited to stainless steel. One or more heat shields 125 are disposed on the inner surface 113 of the body 110 that prevents heat loss from the single-substrate processing chamber 100 into the outside environment. The inner surface 113 of the body 110 as well as the heat shields 125 may be made from nickel-based steel alloys that exhibit high resistance to corrosion, such as but not limited to HASTELLOY®, ICONEL®, and MONEL®.

[0019] A substrate support 130 is disposed within the internal volume 115. The substrate support 130 has a stem 134 and a substrate-supporting member 132 held by the stem 134. The stem 134 passes through a passage 122 formed through the chamber body 110. A rod 139 connected to an actuator 138 passes through a second passage 123 formed through the chamber body 110. The rod 139 is coupled to a plate 135 having an aperture 136 accommodating the stem 134 of the substrate support 130. Lift pins 137 are connected to the substrate-supporting member 132. The actuator 138 actuates the rod 139 such that the plate 135 is moved up or down to connect and disconnect with the lift pins 137. As the lift pins 137 are raised or lowered, the substrate-supporting member 132 is raised or lowered within the internal volume 115 of the chamber 100. The substrate-supporting member 132 has a resistive heating element 131 embedded centrally within. A power source 133 is configured to electrically power the resistive heating element 131. The operation of the power source 133 as well as the actuator 138 is controlled by a controller 180.

[0020] The single-substrate processing chamber 100 has an opening 111 on the body 110 through which one or more substrates 120 can be loaded and unloaded to and from the substrate support 130 disposed in the internal volume 115. The opening 111 forms a tunnel 121 on the body 110. A slit valve 128 is configured to sealably close the tunnel 121 such that the opening 111 and the internal volume 115 can only be accessed when the slit valve 128 is open. A high-pressure seal 127 is utilized to seal the slit valve 128 to the body 110 in order to seal the internal volume 115 for processing. The high-pressure seal 127 may be made from a polymer, for example a fluoropolymer, such as but not limited to a perfluoroelastomer and polytetrafluoroethylene (PTFE). The high-pressure seal 127 may further include a spring member for biasing the seal to improve seal performance. A cooling channel 124 is disposed on the tunnel 121 adjacent to the high-pressure seals 127 in order to maintain the high-pressure seals 127 below the maximum safe-operating temperature of the high-pressure seals 127 during processing. A cooling agent from a cooling fluid source 126, such as but not limited to an inert, dielectric, and high-performance heat transfer fluid, may be circulated within the cooling channel 124. The flow of the cooling

agent from the cooling fluid source 126 is controlled by the controller 180 through feedback received from a temperature sensor 116 or a flow sensor (not shown). An annular-shaped thermal choke 129 is formed around the tunnel 221 to prevent the flow of heat from the internal volume 115 through the opening 111 when the slit valve 128 is open.

[0021] The single-substrate processing chamber 100 has a port 117 through the body 110, which is fluidly connected to a fluid circuit 190 connecting the gas panel 150, the condenser 160 and the port 117. The fluid circuit 190 has a gas conduit 192, a source conduit 157, an inlet isolation valve 155, an exhaust conduit 163, and an outlet isolation valve 165. A number of heaters 196, 158, 152, 154, 164, 166 are interfaced with different portions of the fluid circuit 190. A number of temperature sensors 151, 153, 119, 167 and 169 are also placed at different portions of the fluid circuit 190 to take temperature measurements and send the information to the controller 180. The controller 180 uses the temperature measurement information to control the operation of the heaters 152, 154, 158, 196, 164, and 166 such that the temperature of the fluid circuit 190 is maintained at a temperature above the condensation point of the processing fluid disposed in the fluid circuit 190 and the internal volume 115.

[0022] The gas panel 150 is configured to provide a processing fluid under pressure the internal volume 115. The pressure of the processing fluid introduced into the internal volume 115 is monitored by a pressure sensor 114 coupled to the body 110. The condenser 160 is fluidly coupled to a cooling fluid source (not shown) and configured to condense the gas phase processing fluid exiting the internal volume 115 through the gas conduit 192. The condensed processing fluid is then removed by the pump 176. One or more heaters 140 are disposed on the body 110 and configured to heat the internal volume 115 within the single-substrate processing chamber 100. The heaters 140, 152, 154, 158, 196, 164, and 166 maintain the processing fluid within the fluid circuit 190 in a gaseous phase while the outlet isolation valve 165 to the condenser 160 is open to prevent condensation within the fluid circuit.

[0023] The controller 180 controls the operation of the single-substrate processing chamber 100. The controller 180 controls the operation of the gas

panel 150, the condenser 160, the pump 170, the inlet isolation valve 155, the outlet isolation valve 165, the power sources 133 and 145. The controller 180 is also communicatively connected to the temperature sensor 116, the pressure sensor 114, the actuator 138, the cooling fluid source 126 and the temperature reading devices 156 and 162.

[0024] The processing fluid may comprise an oxygen-containing and/or nitrogen-containing gas, and/or chalcogen or tellurium (such as S, Se, Te) gases or vapors such as oxygen, dry steam, water, hydrogen peroxide, ammonia, S vapor, Se vapor, H₂S, H₂Se, etc. The processing fluid may be reacted with the metal materials on the substrate to form metal oxynitrides, metal oxides, metal oxychalcogenides or metal chalcogenides. Alternatively or in addition to the oxygen-containing and/or nitrogen-containing gases, the processing fluid may comprise a silicon-containing gas. Examples of the silicon-containing gas include organosilicon, tetraalkyl orthosilicate gases and disiloxane. Organosilicon gases include gases of organic compounds having at least one carbon-silicon bond. Tetraalkyl orthosilicate gases include gases consisting of four alkyl groups attached to an SiO₄⁴⁻ ion. More particularly, the one or more gases may be (dimethylsilyl)(trimethylsilyl)methane ((Me)₃SiCH₂SiH(Me)₂), hexamethyldisilane ((Me)₃SiSi(Me)₃), trimethylsilane ((Me)₃SiH), trimethylsilylchloride ((Me)₃SiCl), tetramethylsilane ((Me)₄Si), tetraethoxysilane ((EtO)₄Si), tetramethoxysilane ((MeO)₄Si), tetrakis-(trimethylsilyl)silane ((Me₃Si)₄Si), (dimethylamino)dimethyl-silane ((Me₂N)SiHMe₂), dimethyldiethoxysilane ((EtO)₂Si(Me)₂), dimethyl-dimethoxysilane ((MeO)₂Si(Me)₂), methyltrimethoxysilane ((MeO)₃Si(Me)), dimethoxytetramethyl-disiloxane (((Me)₂Si(OMe))₂O), tris(dimethylamino)silane ((Me₂N)₃SiH), bis(dimethylamino)methylsilane ((Me₂N)₂CH₃SiH), disiloxane ((SiH₃)₂O), and combinations thereof.

[0025] During processing of the substrates 120, an environment of the high-pressure region 115 is maintained at a temperature and pressure that maintains the processing fluid within the high-pressure region in a vapor phase. Such pressure and temperature is selected based on the composition of the processing fluid. In the case of steam, the temperature and pressure is held at a

condition that maintains the steam in a dry steam state. In one example, high-pressure region 115 is pressurized to a pressure greater than atmosphere, for example greater than about 2 bars. In another example, high-pressure region 115 is pressurized to a pressure from between about 10 and about 50 bars, such as from between about 20 and about 50 bars. In another example, the high-pressure region 115 is pressurized to a pressure up to about 100 bars. During processing, the high-pressure region 115 is also maintained at a high temperature, for example, a temperature exceeding 225 degrees Celsius (limited by the thermal budget of the substrates 155 disposed on the cassette 150), such as between about 300 degrees Celsius and about 500 degrees Celsius.

[0026] Figure 2 is a schematic, top plan view of an exemplary processing system 200 that includes one or more of the processing chambers, such as the processing chamber 100 illustrated in Figure 1, that are incorporated and integrated therein. In one embodiment, the processing system 200 may be a Centura® or Endura® integrated processing system, commercially available from Applied Materials, Inc., located in Santa Clara, California. It is contemplated that other processing systems (including those from other manufacturers) may be adapted to benefit from the disclosure.

[0027] The system 200 includes a vacuum-tight processing platform 204, a factory interface 202, and a system controller 244. The platform 204 includes a plurality of processing chambers 100, 212, 232, 228, 220, such as the one of the processing chamber 100 depicted in Figure 1, and at least one load-lock chamber 222 that is coupled to a vacuum substrate transfer chamber 236. Two load lock chambers 222 are shown in Figure 2. The factory interface 202 is coupled to the transfer chamber 236 by the load lock chambers 222.

[0028] In one embodiment, the factory interface 202 comprises at least one docking station 208 and at least one factory interface robot 214 to facilitate transfer of substrates. The docking station 208 is configured to accept one or more front opening unified pod (FOUP). Two FOUPS 206A-B are shown in the embodiment of Figure 2. The factory interface robot 214 having a blade 216 disposed on one end of the robot 214 is configured to transfer the substrate

from the factory interface 202 to the processing platform 204 for processing through the load lock chambers 222. Optionally, one or more metrology stations 518 may be connected to a terminal 226 of the factory interface 202 to facilitate measurement of the substrate from the FOUPS 206A-B.

[0029] Each of the load lock chambers 222 have a first port coupled to the factory interface 202 and a second port coupled to the transfer chamber 236. The load lock chambers 222 are coupled to a pressure control system (not shown) which pumps down and vents the load lock chambers 222 to facilitate passing the substrate between the vacuum environment of the transfer chamber 236 and the substantially ambient (e.g., atmospheric) environment of the factory interface 202.

[0030] The transfer chamber 236 has a vacuum robot 230 disposed therein. The vacuum robot 230 has a blade 234 capable of transferring substrates 224 among the load lock chambers 222, the metrology system 210 and the processing chambers 212, 232, 228, 220.

[0031] In one embodiment of the system 200, the system 200 may include one or more processing chambers 100, 212, 232, 228, 220, which may be a annealing chamber (e.g., high pressure annealing chamber, RTP chamber, laser anneal chamber), deposition chamber, etch chamber, cleaning chamber, curing chamber, or other similar type of semiconductor processing chambers. In some embodiments of the system 200, one or more of processing chambers 100, 212, 232, 228, 220, the transfer chamber 236, the factory interface 202 and/or at least one of the load lock chambers 222.

[0032] The system controller 244 is coupled to the processing system 200. The system controller 244, which may include the computing device 201 or be included within the computing device 201, controls the operation of the processing system 200 using a direct control of the process chambers 100, 212, 232, 228, 220 of the system 200. Alternatively, the system controller 244 may control the computers (or controllers) associated with the process chambers 100, 212, 232, 228 and the system 200. In operation, the system controller 244 also enables data collection and feedback from the respective chambers to optimize performance of the system 200.

[0033] The system controller 244, much like the computing device 201 described above, generally includes a central processing unit (CPU) 238, a memory 240, and support circuit 242. The CPU 238 may be one of any form of a general purpose computer processor that can be used in an industrial setting. The support circuits 242 are conventionally coupled to the CPU 238 and may comprise cache, clock circuits, input/output subsystems, power supplies, and the like. The software routines transform the CPU 238 into a specific purpose computer (controller) 244. The software routines may also be stored and/or executed by a second controller (not shown) that is located remotely from the system 200.

[0034] Figure 3 depicts an example of a TFT device 350 that include a metal containing layer that may undergo a thermal annealing process in a high pressure annealing chamber, such as the high pressure annealing process 100 depicted in Figure 1, which may be incorporated into the system 200 depicted in Figure 2. The thin film transistor device structure 350 is a bottom gate TFT structure disposed on a substrate 301. It is noted that the substrate 301 may have different combination of films, structures or layers previously formed thereon to facilitate forming different device structures or different film stack on the substrate 301. In one example, the substrate 301 may have the device structure 350 formed thereon, as shown in Figure 3. Alternatively, the substrate 301 may have another device structure 450 disposed thereon, as further shown in Figure 4, which will be further described below. The substrate 301 may be any one of glass substrate, plastic substrate, polymer substrate, metal substrate, singled substrate, roll-to-roll substrate, or other suitable transparent substrate suitable for forming a thin film transistor thereon.

[0035] A gate electrode layer 302 is formed and patterned on the substrate 301 followed by a gate insulator layer 304. In one embodiment, the gate electrode layer 302 may be fabricated from any suitable metallic material, such as aluminum (Al), tungsten (W), chromium (Cr), tantalum (Ta), molybdenum (Mo), copper (Cu) or combination thereof. Suitable materials for the gate insulator layer 304 include silicon oxide (SiO_2), silicon oxynitride (SiON), silicon nitride (SiN), and the like. It is noted that the thin film transistor device structure

350 depicted in Figure 3 is a bottom gate device structure with the gate electrode layer 302 formed on a bottom of the device structure 350.

[0036] An active layer 306 is formed on the gate insulator layer 304. The material utilized for the active layer 306 may be selected from a transparent metallic oxide material that has high electron mobility that is suitable low temperature manufacturing that allows flexible substrate materials, such as plastic materials, to be processed at a low temperature without substrate damage. Suitable examples of materials that can be utilized for the active layer 306 include a-IGZO (amorphous indium gallium zinc oxide), InGaZnON, ZnO, ZnON, ZnSnO, CdSnO, GaSnO, TiSnO, CuBO₂, CuAlO₂, CuGaO₂, SrCuO, LaCuOS, GaN, InGaN, AlGaN or InGaAlN, among others.

[0037] After formation of the active layer 306, a barrier layer 308 may be formed on the active layer 306. The barrier layer 308 may be formed from a metal containing material so as to provide a good interface adhesion as well as good barrier properties (e.g., diffusion barrier) to a metal electrode layer 310 (e.g., for a source-drain electrode) subsequently formed thereon. The barrier layer 308 may be patterned to form a desired pattern on the active layer 306 to facilitate transfer of features on the film layers disposed on the substrate 301 in the subsequent etching processes. Although the barrier layer 308 as depicted in Figure 3 is patterned to a desired pattern, it is noted that the barrier layer 308 could be in any form, including a whole continuous blank film in the device structure 350 or any different features as needed as long as the barrier layer 308 may efficiently provide a blocking/diffusion barrier property to prevent elements from the active layer 306 diffusing into the metal electrode layer 310, or vice versa. In one embodiment, the barrier layer 308 may be a single layer of a metal containing dielectric layer, as depicted in Figure 3, fabricated by a metal dielectric layer, such as Ta₂O₅ or TiO₂, or any suitable metal dielectric layer as needed. In another embodiment, the barrier layer 308 may be in form of a composite film as needed.

[0038] After the metal electrode layer 310, such as a source-drain metal electrode layer, is disposed over the barrier layer 308, subsequently, an etching process is performed to form a channel 320 in the metal electrode layer 310.

After etching, an insulating material layer 314, such as a passivation layer, is then formed over the metal electrode layer 310 to complete the process of forming the thin film transistor device structure 350.

[0039] In one embodiment, examples of materials that may be used as the metal electrode layer 310 include copper (Cu), gold, silver (Ag), aluminum (Al), tungsten (W), molybdenum (Mo), chromium (Cr), tantalum (Ta), alloys thereof and combination thereof. Suitable materials that may be used as the insulating material layer 314 include silicon oxide (SiO_2), silicon oxynitride (SiON), or silicon nitride (SiN), and the like.

[0040] Figure 4 depicts an example of a top gate low temperature polysilicon (LTPS) TFT device structure 450 that may be formed on the substrate 301, rather than the bottom gate device structure 350 depicted in Figure 3. The LTPS TFT devices 450 are MOS devices built with active layers 452 including a source region 409a, channel region 408, and drain region 409b (e.g., or called metal contact regions, or source-drain metal contacts) formed on the optically transparent substrate 301 with or without an optional insulating layer 404 disposed thereon. In one example, the active layer including the source region 409a, channel region 408, and drain region 409b may be fabricated from a transparent metal containing layer, such as metallic oxide material, that has high electron mobility that is suitable for low temperature manufacturing that allows flexible substrate materials, such as plastic materials, to be processed at a low temperature without substrate damage. Suitable examples of such materials that can be utilized for the source region 409a, channel region 408, and drain region 409b include a-IGZO (amorphous indium gallium zinc oxide), doped IGZO, InGaZnON, ZnO, ZnON, ZnSnO, CdSnO, GaSnO, TiSnO, CuBO_2 , CuAlO_2 , CuGaO_2 , SrCuO, LaCuOS, GaN, InGaN, AlGaN or InGaAlN, among others.

[0041] A gate insulating layer 406 is then deposited on top of the deposited polysilicon layer(s) to isolate a barrier layer 411 and a metal electrode layer 414, such as a gate electrode, disposed thereon from the channel region 408, source region 409a and drain region 409b. The barrier layer 411 may be formed from a metal containing material so as to provide a good interface adhesion as well as

good barrier properties (e.g., diffusion barrier) to the metal electrode layer 414 (e.g., the gate electrode) subsequently formed thereon. The barrier layer 411 may be patterned to form a desired pattern on the gate insulating layer 406 to facilitate transfer of features on the film layers disposed on the substrate 102 in the subsequent etching processes. The barrier layer 411 may efficiently provide a blocking/diffusion barrier property to prevent elements from the gate insulating layer 406 diffusing into the metal electrode layer 414, or vice versa. In one embodiment, the barrier layer 411 may be a single layer of a metal containing dielectric layer, as depicted in Figure 4, fabricated by a metal dielectric layer, such as Ta₂O₅ or TiO₂, or any suitable metal dielectric layer as needed. In another embodiment, the barrier layer 411 may be in form of a composite film as needed.

[0042] The gate electrode layer 414 is formed on top of the gate insulating layer 406 with the barrier layer 411 interposed therebetween. The gate insulating layer 406 is also commonly known as a gate oxide layer since it is commonly made of a silicon dioxide (SiO₂) layer. An insulating material layer 412, such as an interlayer insulator, and device connections (not shown) are then made through the insulating material layer 412 to allow control of the TFT devices.

[0043] After the insulating material layer 412 is formed, a source-drain metal electrode layer 410a, 410b is then deposited, formed and patterned in the insulating material layer 412. After the source-drain metal electrode layer 410a, 410b is patterned, a passivation layer 418 is then formed over the source-drain metal electrode layer 410a, 410b.

[0044] Figure 5 depicts a flow diagram of one example of a thermal annealing process 500 performed on a metal containing layer, such as the active layers 306, 452 in Figures 3-4, or the metal electrodes 302, 310, 410a, 410b, 414 in Figures 3-4 respectively.

[0045] The method 500 begins at operation 502 by providing a substrate, such as the substrate 301 in Figures 3 and 4. The substrate 301 may be an optical transparent substrate. The substrate 301 may comprise a material layer 601 disposed thereon, as shown in Figure 6A. The material layer 601 may be a

single layer or multiple layers that may be utilized to form a TFT device structure. Alternatively, the material layer 601 may be a structure may include multiple materials that may be utilized to form a TFT device structure.

[0046] The substrate 301 further includes a metal containing layer 602 formed on the material layer 601, as shown in Figure 6B. In the examples wherein the material layer 601 is not present, the metal containing layer 602 may be directly formed on the substrate 301. In some examples, the metal containing layer 602 may be used as the active layers 306, 452 in Figure 3 or 4, or the metal electrodes 302, 310, 410a, 410b, 414 in Figures 3-4. In an example, the metal containing layer 602 is a metal oxide layer selected from a group consisting of a-IGZO (amorphous indium gallium zinc oxide), doped IGZO, InGaZnON, ZnO, ZnON, ZnSnO, CdSnO, GaSnO, TiSnO, CuBO₂, CuAlO₂, CuGaO₂, SrCuO, LaCuOS, GaN, InGaN, AlGaN or InGaAlN and the like. In one example, the metal containing layer 602 is a IGZO or doped IGZO layer. Alternatively, the metal containing layer 602 may be a metal layer, such as copper (Cu), gold, silver (Ag), aluminum(Al), tungsten (W), molybdenum (Mo), chromium (Cr), tantalum (Ta), alloys thereof, or the like.

[0047] At operation 504, an optional ion doping/implantation process is performed to implant ions into the metal containing layer 602, forming a doped metal containing layer 610, as shown in Figure 6C. In the examples wherein the ion implantation process is eliminated, the thermal annealing process at operation 506, which will be described in greater detail below, may be performed directly on the metal containing layer 602. The ion doping/implantation process is performed to dope, coat, treat, implant, insert or modify certain film/surface properties on certain locations of the metal containing layer 602 with dopants formed into, forming the doped metal containing layer 610. The ion doping/implantation process utilizes incident ions to modify film/surface properties on the metal containing layer 602, with dopants doped thereto to form the doped metal containing layer 610. The ion doping/implantation process may be performed in any suitable ion implantation/doping processing tools. The ions, which include a desired type of atoms, may be doped into the metal containing layer 602 with desired

concentration. The ions doped into the metal containing layer 602 may modify the film/surface properties of the metal containing layer 602, which may affect, improve or alter the lattice structure, degree of crystalline, bonding structure or film density of the metal containing layer 602, forming the doped metal containing layer 610.

[0048] In the embodiment wherein the metal containing layer 602 includes InGaZnO, the ions doped into the metal containing layer 602 may include indium (In) or molybdenum (Mo), gallium (Ga), zinc (Zn) and the like. It is believed that In or Mo dopants doped into the metal containing layer 602 (e.g., a InGaZnO) may alter the electrical properties such as high mobility, crystallinity (e.g., from amorphous structure, C-axis aligned crystalline structure (CAAC), polycrystalline structure or even single crystalline structure) of the InGaZnO material, thus, providing the doped metal containing layer 610 with desired film properties. For example, higher degree of the crystallinity provided by the In or Mo dopants in the InGaZnO material is believed to increase the electron mobility of the film properties, thus enhancing the electrical performance of the TFT device structure or semiconductor devices, when doped metal containing layer 610 is utilized thereof.

[0049] Furthermore, it is also believed that the gallium (Ga) and zinc oxide (ZnO) ratio included in the InGaZnO material may also affect the resultant lattice structure of the doped metal containing layer 610. It is believed the ratio of Ga elements included in the InGaZnO material may increase the film transparency as well as the overall film bandgap. The ratio of Zn or ZnO elements included in the InGaZnO material may increase the mobility as well as the reducing the thermal annealing temperature requirements for crystallinity enhancement. Thus, by selecting a proper dosage of the In dopants into the InGaZnO material, a desired crystalline of the InGaZnO material may be obtained. Furthermore, the desired crystalline of the InGaZnO material may also help reducing the temperature requirement in the following thermally annealing process at operation 506, providing process advantages in TFT device applications as the substrate 301 is often optical transparent material with relatively low thermal cycle budgets.

[0050] In one embodiment, the resultant In dopant in the InGaZnO material may have a doping concentration of between about 5×10^{15} ions/cm² and about 9×10^{15} ions/cm², such as about 8.5×10^{15} ions/cm², formed in the doped metal containing layer 610. Furthermore, the ratio of the In or Mo element in the InGaZnO material may be increased from about 10%-13% to about 14%-16% (between about 15 % and about 30 % increase) by atomic weight.

[0051] Several process parameters may be controlled during the ion doping/implantation process. The ion doping/implantation process may be performed by supplying an ion doping gas mixture into the ion doping/implantation tool along with a desired amount of the power energy to dope the ions from the ion doping gas mixture into the substrate 301. The ion doping gas mixture may be supplied into the ion doping/implantation tool at a flow rate between about 10 sccm and about 1000 sccm. Suitable elements for supplying in the ion doping used in vapor state during implant include indium vapor and molybdenum vapor. A RF power, such as capacitive or inductive RF power, DC power, electromagnetic energy, ion beam, or magnetron sputtering, may be supplied into the ion doping/implantation process to assist dissociating the ion doping gas mixture during processing. Ions generated by the dissociative energy may be accelerated toward the substrate using an electric field produced by applying a DC or RF electrical bias to the substrate support or to a gas inlet above the substrate support, or both. In some embodiments, the gas containing energetic ions may be a plasma. An energy of between about 20 keV and about 80 keV, such as between about 35 keV and about 55 keV, for example about 45 keV, may be used to implant ions into the metal containing layer 602. The substrate temperature may be controlled at between about 5 degrees Celsius and about 50 degrees Celsius, such as about 15 degrees Celsius.

[0052] At operation 506, a high pressure annealing process is performed. The annealing process performed at high process pressure, such as greater than 2 bar but less than, may assist densifying and repairing the vacancies in the doped metal containing layer 610, forming the annealed metal containing layer 603 with the desired film properties, as shown in Figure 6D. In some

examples, the high process pressure may go up to 100 bar. In the embodiment wherein the ion doping/implantation process at operation 504 is not performed, the high pressure annealing process may be performed directly on the metal containing layer 602 from Figure 6B to form the annealed metal containing layer 603, as shown in Figure 6D. The annealing process may be performed at a processing chamber, such as the processing chamber 100 depicted in Figure 1, or other suitable processing chambers, including those that process substrate one at a time.

[0053] The high pressure annealing process performed at operation 506 maintains processing pressure at the high-pressure region in a vapor phase, for example in a dry vapor phase that has substantially no liquid droplets present. The processing pressure and temperature is controlled to density the film structures, so as to repair the film defects, driving out impurities and increasing film density. In one example, the high-pressure region 115 is pressurized to a pressure greater than atmosphere, for example greater than about 2 bar. In another example, the high-pressure region 115 is pressurized to a pressure from about 5 to about 100 bars, such as from about 5 to about 50 bars, such as about 35 bar. As the high pressure may efficiently assist densifying the film structure, a relatively low processing temperature, such as less than 500 degrees Celsius, to reduce likelihood of thermal cycle damage to the substrate 301.

[0054] During processing, the high-pressure region 115 is maintained at a relatively low temperature, for example, a temperature less than 500 degrees Celsius, such as between about 150 degrees Celsius and about 350 degrees Celsius, by the heaters 122 disposed within the outer chamber 110. Thus, a low thermal budget to the substrate may be obtained by utilizing the high pressure annealing process along with low temperature regime.

[0055] It is believed that the high pressure process may provide a driving force to drive out the dangling bonds in the metal containing layer 602 or the doped metal containing layer 610, thus, repairing, reacting and saturating the dangling bonds in the metal containing layer 602 during the annealing process. In one example, an oxygen containing gas, such as O₃ gas, O₂ gas, air, H₂O,

H₂O₂, N₂O, NO₂, CO₂, CO and dry steam, or chalcogen vapor including sulfur (S) vapor and selenium (Se) vapor, or tellurium vapor or other suitable gases may be supplied during the annealing process. In one specific example, the oxygen containing gas comprises steam, for example, dry steam and/or air. The oxygen elements from the oxygen containing gas during the annealing process may be driven into the metal containing layer 602, altering the bonding structures and removing the atomic vacancies therein, thus, densifying and enhancing lattice structures and increasing the crystallinity of the metal containing layer 602. In some examples, an inert gas or a carrier gas, such as Ar, N₂, He, Kr and the like, may be supplied with the oxygen containing gas. In one embodiment, the oxygen containing gas supplied in the oxygen containing gas mixture is dry steam supplied at a pressure greater than 2 bar.

[0056] In one exemplary implementation, a process pressure is regulated at a pressure greater than 2 bar, such as between 5 bar and 100 bar, such as between 20 bar and about 80 bar, for example between about 25 bar and 75 bar, such as about 35 bar. The process temperature may be controlled at greater than 150 degrees Celsius but less than 500 degrees Celsius, such as between about 150 degrees Celsius and about 380 degrees Celsius, such as between about 180 degrees Celsius and about 400 degrees Celsius. In one example, chalcogen vapor, such as sulfur (S) vapor, selenium (Se) vapor, may be supplied during the annealing process for metal oxychalcogen, such as InGaZnO comprising S or Se.

[0057] After the annealing process at high pressure, the metal containing layer 602 or the doped metal containing layer 610 has a densified film structure, which provides a relatively robust film structure with amorphous morphology that provides higher film density, high film mobility, low carrier concentration and low film resistivity as compared to the metal containing layer 602 or doped metal containing layer 610 annealed by a conventional annealing process at a pressure around one atmospheric pressure, while both annealing process are at the same anneal temperature. In one example, the mobility of the high pressure annealed metal containing layer 603 with indium dopants (formed from the doped metal containing layer 610) is increased between about 5 times and

about 20 times, resistivity increased about 10 times and carrier concentration decreased about 100 times, as compared to a conventional annealing process at 1 atmospheric pressure while under the same anneal temperature.

[0058] In one example, the mobility of the high pressure annealed metal containing layer 603 without indium dopants (formed from the metal containing layer 602) is increased between about 1.5 times and about 5 times, resistivity increased from about 20 percent to about 99 percent and carrier concentration decreased about 100 times, as compared to a conventional annealing process at 1 atmospheric pressure while under the same anneal temperature.

[0059] Thus, methods for thermal annealing a metal containing layer are provided. The metal containing layer may be thermally treated/annealed by a high pressure annealing process with high process pressure, such as greater than 2 bar but less than 50 bar. By utilizing such high pressure annealing process, the process temperature may be maintained less than 500 degrees Celsius, thus reducing the thermal budge contributed to the substrate where the metal containing layer is formed thereon, providing a good film quality with desired crystallinity and structure integration management.

[0060] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.