

PATENT SPECIFICATION

(11) 1 203 087

DRAWINGS ATTACHED



1 203 087

- (21) Application No. 13609/70 (22) Filed 15 Sept. 1967
 (62) Divided out of No. 1 203 086
 (31) Convention Application No. 606 064 (32) Filed 30 Sept. 1966 in
 (33) United States of America (US)
 (45) Complete Specification published 26 Aug. 1970
 (51) International Classification H 01 1 19/00
 (52) Index at acceptance

H1K 217 312 352 353 415 417 41Y 422 424 42X 441
 454 459 469 470 477 479 482 486 490 507 511
 52Y 53Y 54Y 551 552 55Y 563 581 583 615 616
 618 61Y

C7F 1A 1V1 1V2 2A 2G 2L 2M 2N 2U 2V 2Z2 4A
 4E 4F 4J 4X

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(54) OHMIC CONTACT AND MULTI-LEVEL INTERCONNECTION SYSTEM
 FOR INTEGRATED CIRCUITS

(71) We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices and provision of combined electrical leads and ohmic contacts therefor. This application is divided from our co-pending Application No. 42214/67 (Serial No. 1,203,086) which incorporates part of the disclosure of this specification. More particularly, the present invention relates to integrated circuits having circuit components connected by an ohmic contact and electrical lead arrangement which forms a first level interconnection pattern and is connected at one or more selected locations to a second level interconnection pattern separated from the first level pattern by electrical insulation and which itself may be connected to further levels of interconnection patterns separated by layers of electrical insulation.

The increased demand for micro-miniaturization has been reflected in the field of electronics by the development of semiconductor integrated circuits or networks, whereby a plurality of active and/or passive circuit components are formed in or on a single slice of semiconductor material, each of the circuit components thereafter being interconnected in a particular manner to provide the desired circuit function. For

example, an integrated circuit device of the monolithic type may have a number of transistors and resistors formed by diffusion beneath one major face of a slice or wafer of semiconductor material (a suitable one being silicon), a protective layer (usually of silicon oxide) upon the face of the wafer, and metallic films upon the oxide layer interconnecting the resistors and the various regions of the transistors in a desired pattern through apertures in this oxide. With increasing complexity of circuitry, however, and the corresponding increase in complexity of the interconnection pattern, it has become necessary to form more than one level of metallic film interconnections, with adequate electrical insulation or isolation between the various levels at the cross-over points. This is particularly true when, upon a single slice of semiconductor material, a plurality of separate circuits are formed and it becomes necessary to interconnect the circuits for cooperative action to produce one unitary circuit function.

The materials of which the metal films and the electrical insulating layer or layers are formed must in themselves exhibit favorable chemical, electrical, thermal, and mechanical properties, including compatibility with one another to provide an adequate multi-level contact and interconnection system. For example, the metallic film or films of the first level should provide low resistance ohmic contact to the semiconductor material, should adhere well to the protective layer of oxide upon the face of the slice or wafer, should not excessively alloy with the semiconductor material at temperatures encountered in the processing or packaging of the device

[Price 5s. 0d. (25p)]

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so as to degrade device characteristics, and should not have a melting point below the temperature to which the devices will be exposed during processing and device operation. The insulating material between levels of metal films, on the other hand, should afford adequate electrical isolation and be substantially free of pinholes to avoid the possibility of electrical shorting between levels. In addition, the entire system should be fabricated of metals and insulators or oxides which are hard, structurally strong materials that will not yield or break up during wafer or slice handling and testing; all of the materials should be physically and chemically stable when subjected to high temperatures so that none of the materials will undesirably react with one another or with the semiconductor substrate; the metals and the isolation or insulation medium should tightly adhere to one another and there should be good "inter-level" ohmic contact between the last or exposed metallic film of one level and the first film of the next level at conductive cross points.

In some of the embodiments of this invention to be described, use is made of molybdenum and gold in combination because of the many superior properties that this combination offers. A detailed description of some of these properties appears in British Patent Specification No. 1,104,804, some of the most favorable ones including the fact that molybdenum makes good electrical contact to silicon semiconductor material, particularly if the contact regions are heavily doped, but yet does not undesirably alloy with the silicon surface so as to degrade the device. Furthermore, the molybdenum adheres well to silicon oxide, can be etched in a controlled manner with an etchant not incompatible with other materials used during the fabrication process, and when used in combination with gold is virtually impervious to the gold. In this regard, it is to be noted that when molybdenum is formed in contact with the silicon semiconductor material and a gold layer overlies the molybdenum, there results a virtually "alloyless" contact system, the molybdenum not alloying with the silicon and the gold not alloying with the molybdenum. Gold, in addition to its excellent conductivity is easily deposited by conventional evaporation techniques, lends itself nicely to photoresist etch procedures associated with defining the contact and interconnection patterns and, is easily bondable with an external gold wire.

In addition, the molybdenum-gold contact system is not subject to increasing electrical resistivity due to the inter-dif-

fusion or compound formation associated with many other metallic film combinations. For example, copper wire manufacturers go to great expense to provide ultra high purity copper to obtain high conductivity. This may be explained on the basis that any impurity atoms in even a relatively pure metal tend to scatter the moving electrons in the metal, thus increasing their resistance to current flow. This, however, is not present in the molybdenum-gold film combination because molybdenum and gold have very low mutual solubilities (so that interdiffusion is concentration limited) and also because they form no compounds with one another.

The molybdenum-gold system also offers reliability advantages in high current-density applications. It has been observed that expanded ohmic contacts for integrated circuits and discrete transistors, for example, become electrically open-circuit after prolonged operation at current densities of the order of 1×10^6 A/cm² or higher thus causing device failure. This failure mechanism is believed related to a phenomenon termed current-induced mass transport, the rate of which is approximately inversely proportional to the activation energy of self diffusion of the particular metal conductor or conductors involved. It has been observed that some metals which have low values of activation energy, aluminum for example, have a greater reliability risk associated with them than other metals which have higher values of activation energy. Gold and particularly molybdenum, on the other hand, have very high values of this activation energy of self diffusion, and thus have minimal susceptibility to current-induced mass transport problems.

The invention provides an integrated circuit device comprising: an integrated circuit device comprising a plurality of circuit elements disposed at a common face of a substrate, each circuit element including at least one semiconductor region, the semiconductor regions being covered by a protective coating of insulating material disposed on the said surface of the substrate, a plurality of superposed interconnection levels separated by one or more layers of insulating material except at areas of interconnection between the respective levels, the lowermost interconnection level being disposed on the said protective coating and forming desired interconnections between selected ones of said semiconductor regions through apertures in the protective coating, in which the interconnection levels each comprises a layer of molybdenum, titanium, tantalum, rhodium, cobalt, nickel or aluminum,

and in which the uppermost interconnection level is overlaid by a layer of gold. In one embodiment, the lowermost interconnection level is connected to the uppermost interconnection level through an aperture in an insulating layer separating those two interconnection levels. Advantages can be obtained by oxidizing the upper surface of the or each interconnection level prior to formation of an insulating layer thereon and in such arrangements, the interconnection levels may usefully be interconnected with each other by a layer of oxidation resistant metal disposed in an aperture of the or each said insulating layer.

The invention also provides a method for providing ohmic contacts and multi-level electrical interconnections in an integrated circuit having a plurality of circuit elements formed as integral parts of a body, each circuit element including at least one semiconductor region extending to a surface of the body beneath a protective coating upon that surface, comprising the steps of: forming a plurality of apertures in the protective coating to expose the surfaces of selected ones of the semiconductor regions; depositing a first film of molybdenum upon the protective coating and within the apertures to contact the selected regions (in a particular embodiment a second film of gold is deposited upon the first film); selectively etching the first film (and the second film) to provide ohmic contacts to the selected regions and a plurality of first level interconnectors electrically interconnecting desired groups of the selected regions, (in the particular embodiment the second film is selectively removed from each of the first level interconnectors except for a discrete portion of gold overlying a corresponding portion of molybdenum of one or more of the first level of interconnectors, the remainder of the first film being exposed, and then the surface portions only of the exposed molybdenum are converted to molybdenum oxide, the or each said discrete portion of gold serving to mask the oxidizing of the underlying molybdenum region); depositing a layer of insulating medium overlying each of the first level interconnectors; selectively etching the layer of insulating medium to expose a portion of one or more of the first level interconnectors (in the particular embodiment to expose the or each gold portion); and selectively forming a second level interconnector upon the insulating medium to electrically interconnect with the exposed portion of the or each said first level interconnector (or in the particular embodiment with the or each said gold portion), the second level interconnector

comprising a film of molybdenum deposited on the insulating medium and a film of gold deposited on that said molybdenum film.

Reference in the preceding paragraphs to "molybdenum" and "gold" is to be construed as including the inclusion of added trace impurities e.g. to improve the adherence thereof. The invention also provides specific methods for providing multi-level ohmic contacts and electrical interconnections in a semiconductor integrated circuit of the type having a plurality of circuit components formed as integral parts of a body, by semiconductor regions defining pn junctions extending to a surface of the body beneath the protective coating upon that surface.

By way of example, embodiments of the invention will now be described in greater detail with reference to the accompanying drawings, in which:

Figure 1 is a plan view, greatly enlarged, of a semiconductor wafer or slice containing a plurality of electrical circuit functional elements and suitable for carrying out this invention;

Figure 2 is a circuit diagram of one of the functional elements shown in Figure 1;

Figure 3 is a plan view, greatly enlarged, of the layout of circuit components in one of the functional elements in the wafer of Figure 1, these same circuit components being illustrated in schematic diagram form in Figure 2;

Figures 4-6 are sectional views of a portion of the integrated circuit structure shown in Figures 3 taken along the section line 4-4, showing subsequent steps in the provision of the multi-level interconnection system of the present invention; and

Figures 7-10 are sectional views of the portion of the wafer taken along the section line 4-4 in Figure 3, showing subsequent steps and another method of construction of a multi-level interconnection system in accordance with the invention.

All of the figures are not necessarily to scale, but in some instances relative dimensions have been exaggerated to emphasize particular features of the invention.

Referring now to the drawings, a slice or wafer substrate 10 of semiconductor material, in this case silicon semiconductor material, is illustrated in Figure 1, having a number of electrical circuit functional elements therein. Although only sixteen such functional elements are shown for illustration, ordinarily a much larger number is utilized. Each of the functional elements 11-26 contains the necessary number of transistors, resistors, capacitors or other components, interconnected to produce a desired electrical cir-

cuit function. For example, the functional element 13 may comprise the circuit shown schematically in Figure 2 and by plan view in Figure 3. The circuit of this functional element 13 would then include the P-N-P transistors 32, 33, 34 and 35 and the N-P-N transistors 36, 37, 43, 45, 46, 47 and 50, the three input terminals A, B, and X and an output terminal G. These terminals, along with the voltage supply terminal V, would correspond to the five identically designated terminals on the functional element 13 in Figure 1.

Let us assume that it is desired to appropriately interconnect the four functional elements 13, 16, 21 and 26 of the sixteen functional elements 11-26 for their cooperative action to produce a unitary electrical function. As depicted in Figure 1, therefore, the terminals B, D, J, and O of functional elements 13, 16, 21 and 26, respectively, are electrically joined by the interconnector 28; similarly, the terminals V, F, L and R are electrically joined by the interconnector 29, and the terminals X, H, M and Q are electrically joined by the interconnector 30. Recognizing that there are already a large number of first level electrical interconnections joining the various transistors with one another as well as with the other circuit components and terminals, as shown in Figure 3, it will be appreciated that the interconnectors 28, 29 and 30 must necessarily overlie some of the first level metal interconnection pattern shown in Figure 3. For this reason, and also because the interconnections between functional elements are preferably made in an operation separate from the one by which the interconnections within an element are formed, the interconnection pattern of Figure 1 must necessarily be formed as a second level, separated from the first level interconnection pattern by an insulating medium.

The transistors and the other circuit components may be formed within or upon the semiconductor substrate 10 by any of the techniques known in the integrated circuit art such as, for example, epitaxial growth or diffusion. Thus, looking at Figure 4 there is depicted, in section, a portion of the integrated circuit structure of Figure 3 before the application of any of the metal interconnectors. The N-P-N transistor 36 comprises an N-type collector formed by the substrate 10, the diffused P-type base region 51, and an N-type diffused emitter region 52. The resistor R_1 is provided by the P-type diffused region 53, formed simultaneously with the base region 51 of the transistor. An oxide coating 54 on the top surface of the substrate acquires a stepped con-

figuration, as shown, due to the successive diffusion operations. Thereafter apertures or holes are cut in the oxide coating 54 where the first level interconnection ohmic contacts are to be made.

As the next step, a thin metal film 55 of 20,000 angstroms, for example, formed of molybdenum, one of the better electrical conductors, (see Figure 5) is deposited upon the surface of the oxide layer 54 and in ohmic contact with the semiconductor material within the apertures or holes in the oxide layer. Various techniques may be utilized for the deposition of the molybdenum film 55, for example sputtering, evaporation, or sublimation; one evaporation technique being described more particularly in British Patent Specification No. 1,104,804. Using conventional photographic masking and etching techniques known in the industry, selected portions of the molybdenum film 55 are removed to provide the first level pattern of ohmic contacts and interconnections, the interconnector 71 ohmically connecting the base of the transistor 36 to one end of the resistor R_1 , the interconnector 72 making ohmic contact to the transistor 36 emitter; while the interconnector 73 ohmically connects the collector of the transistor 36 to the supply terminal V, as illustrated in Figure 5.

A layer 56 of insulating medium is then deposited by any suitable technique, for example evaporation, sputtering or electron beam deposition, over the molybdenum film 55, and then selectively etched to expose the surface of the molybdenum film solely at the terminal point V, as depicted in Figure 6. The purpose of the insulating layer 56 is to electrically isolate the metal of the first level interconnectors from the metal of the second level interconnectors which are to be subsequently deposited. Accordingly, the layer 56 may be formed of inorganic materials such as silicon nitride, aluminum oxide, tantalum oxide, or various organic insulating materials. In this particular example the insulating layer 56 is silicon dioxide, deposited by RF sputtering to a thickness of 10,000 angstroms. The layer is then selectively removed to expose the top surface of the molybdenum film 55 at the bonding pad V.

Another molybdenum film 57 is now deposited upon the insulating oxide layer 56 to a thickness of, say, 1200 angstroms, followed by the deposition by evaporation, for example, of a gold film 58, formed to a thickness of approximately 7500 angstroms, for example. The metal films 57 and 58 are then selectively etched to provide the pattern for the second level interconnector 29, the inter-level contact be-

ing provided at the bonding pad V between the molybdenum films 57 and 55, respectively. The top layer 58, being of gold, has an extremely high conductivity and adheres well to the molybdenum film 57. An external bonding wire of gold, for example, may then be bonded by thermocompression to the gold film 58. Among the advantages of this system, as illustrated in Figure 6, is the extremely good adherence of the molybdenum layers or films 55 and 57 to the insulating layer 56. If a three, four, or a higher level contact and interconnection system is desired, each of the levels besides the final one could be of a pure molybdenum film with the final level being a molybdenum-gold combination, the overlying layer of gold facilitating bonding with an external wire.

Prior to the deposition of the molybdenum film 57, it may be desirable to carry out a careful pre-deposition cleanup, for example by sputter-cleaning, of the surface of the insulating film 56 and the exposed surface of the molybdenum film 55. This cleaning minimizes or eliminates any surface oxides that may have formed upon the exposed surface of the molybdenum film 55, thus insuring good inter-level ohmic contact between the molybdenum films 55 and 57, as well as the adherence of molybdenum film 57 to the insulating film 56.

Another embodiment of the present invention is illustrated in Figures 7-10 and described below. A pair of thin metal films 60 and 61 of molybdenum and gold, respectively, are deposited as before and selectively etched to provide the first level interconnection pattern including the interconnectors 71, 72 and 73 as illustrated in Figure 7. The molybdenum layer 60 should desirably be deposited to a thickness of from 10,000 to 30,000 angstroms, followed by a thinner (approximately 1,000 angstroms) film of gold 61. The gold film is then selectively etched, for example, to remove all the gold film except a surface area portion 75, as shown in Figure 8 providing the bonding pad terminal V, the area where the second level of metallic interconnections are to make contact to the first level. The selective removal of the gold film 61 is accomplished by applying an etchant, for example a cyanide solution, which selectively removes gold, but substantially unaffected the underlying molybdenum film.

A very thin insulating skin 60a of molybdenum oxide (MoO_3) is then genetically formed from and adjacent to the molybdenum film 60. This may be accomplished by placing the entire assembly in an oxygen atmosphere for about 10 minutes at approximately 400°C to therm-

ally oxidize the surface of the molybdenum film 60, thus forming a molybdenum oxide insulating skin a few thousand angstroms thick. The gold region or area 75 is substantially unaffected by this thermal oxidation operation, and provides an oxidation mask for the portion of the molybdenum film 60 underlying the area 75. The resulting structure is shown in Figure 10 wherein the unoxidized portion of the molybdenum film 60 is illustrated as providing the ohmic interconnectors of the first level, an oxide or insulating skin overlying this molybdenum film except for a thin film of gold 61 which overlies the unoxidized portion of the molybdenum film 60 at the interlevel bonding terminal pad V.

A layer 56 of insulating material, for example silicon dioxide, is then deposited to a thickness of from 10,000 to 20,000 angstroms, for example, upon the entire face of the assembly shown in Figure 9, this layer then being selectively etched to expose the surface of the gold film portion 75, and films 57 and 58 of molybdenum and gold are then deposited as before and selectively etched to provide the second or final level interconnector 29.

The resulting structure is shown in Figure 10. It provides the additional advantage of two distinctly different insulating layers or oxides 60a and 56 sandwiched together to avoid any congruent pinholes, thereby increasing the electrical isolation between the levels of interconnectors. These isolating films 60a and 56 may be composed of two different materials and formed by different physical or chemical processes. In addition, it is to be particularly noted that the oxidation of the molybdenum layer of film 60 provides isolation or insulation not only at the top of this layer but also around the edges of the film, thereby additionally increasing the electrical isolation. While this embodiment contemplates the use of molybdenum and gold as the metal films due to their superior characteristics, and the advantages obtained as discussed above, other combinations of metals may be utilized when practicing the described method, noting that the metallic layer 60 could be formed of an oxidizable metal such as titanium, tantalum, rhodium, cobalt, nickel or even aluminum, if desired, while the overlying layer 61 should be of an oxidation resistant metal, gold being a very desirable one due to its excellent conductivity.

Various modifications of the above described embodiments and processes may be utilized in accordance with the invention. For example, it may be desirable to perform very shallow

low diffusions of impurities at the points of contact between the molybdenum film (films) and the semiconductor surface to provide low resistance ohmic contacts at these points. In addition, instead of depositing the molybdenum film directly upon the semiconductor surface, regions or zones of metallic material may be deposited intermediate the silicon surface and the molybdenum film. These metallic regions may be, for example, platinum-silicide deposits formed in the contact areas prior to the deposition of the molybdenum film, or a flash or very thin layer of aluminum applied prior to the deposition of the molybdenum film. Further, it is to be understood that throughout the above description the use of the metals molybdenum and gold are to include not only pure molybdenum and gold layers, but also molybdenum and gold layers that may have a minor percentage of impurities added thereto. For example, trace impurities may be added to the molybdenum film to increase its adherence and the gold films may have a minor percentage of platinum added thereto to increase the adhesion of the gold to the molybdenum.

While the embodiments and processes of the present invention have been directed toward monolithic integrated circuits and the application of multi-level interconnections to these monolithic integrated circuits, the processes and structures described above may have other applications such as in the areas of hybrid integrated circuits, whenever it is desired to provide alternating layers or films of metal and electrical insulating material. Various other modifications of the disclosed processes and embodiments will become apparent to persons skilled in the art without departing from the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. An integrated circuit device comprising a plurality of circuit elements disposed at a common face of a substrate, each circuit element including at least one semiconductor region, the semiconductor regions being covered by a protective coating of insulating material disposed on the said surface of the substrate, a plurality of superposed interconnection levels separated by one or more layers of insulating material except at areas of interconnection between the respective levels, the lowermost interconnection level being disposed on the said protective coating and forming desired interconnections between selected ones of said semiconductor regions through apertures in the protective coating, in which the interconnection levels

each comprise a layer of molybdenum, titanium, tantalum, rhodium, cobalt, nickel or aluminum, and in which the uppermost interconnection level is overlaid by a layer of gold.

2. An integrated circuit device as claimed in Claim 1, in which the lowermost interconnection level is connected to the uppermost interconnection level through an aperture in an insulating layer separating the two said interconnection levels.

3. An integrated circuit device as claimed in Claim 2, in which the lowermost and uppermost interconnection levels are molybdenum layers making direct contact with each other through the aperture in the said insulating layer.

4. An integrated circuit device as claimed in Claim 2, in which the lowermost and uppermost interconnection levels are molybdenum layers making contact with each other through a layer of gold disposed in the aperture of the said insulating layer.

5. An integrated circuit device as claimed in Claim 1, in which the upper surface of the or each interconnection level other than the uppermost level is oxidized prior to formation of the said insulating layer thereon.

6. An integrated circuit device as claimed in Claim 5, in which the superposed interconnection levels are connected with each other by layers of oxidation resistant metal disposed in an aperture of the or each said insulating layer.

7. An integrated circuit device as claimed in Claim 6, wherein the oxidation resistant metal is gold.

8. An integrated circuit device as claimed in any preceding claim, in which the said circuit elements are formed as integral parts of a single body of semiconductor material.

9. An integrated circuit device according to Claim 8, in which the said body is composed of silicon.

10. An integrated circuit device as claimed in any preceding claim in which the said insulating medium is composed of silicon oxide.

11. An integrated circuit device as claimed in any preceding claim, in which the said protective coating is composed of silicon oxide.

12. An integrated circuit device as claimed in Claim 8 or Claim 9, in which the said insulating medium is composed of silicon nitride, aluminum oxide or tantalum oxide.

13. An integrated circuit device as claimed in any preceding claim, in which the lowermost interconnection level di-

low diffusions of impurities at the points of contact between the molybdenum film (films) and the semiconductor surface to provide low resistance ohmic contacts at these points. In addition, instead of depositing the molybdenum film directly upon the semiconductor surface, regions or zones of metallic material may be deposited intermediate the silicon surface and the molybdenum film. These metallic regions may be, for example, platinum-silicide deposits formed in the contact areas prior to the deposition of the molybdenum film, or a flash or very thin layer of aluminum applied prior to the deposition of the molybdenum film. Further, it is to be understood that throughout the above description the use of the metals molybdenum and gold are to include not only pure molybdenum and gold layers, but also molybdenum and gold layers that may have a minor percentage of impurities added thereto. For example, trace impurities may be added to the molybdenum film to increase its adherence and the gold films may have a minor percentage of platinum added thereto to increase the adhesion of the gold to the molybdenum.

While the embodiments and processes of the present invention have been directed toward monolithic integrated circuits and the application of multi-level interconnections to these monolithic integrated circuits, the processes and structures described above may have other applications such as in the areas of hybrid integrated circuits, whenever it is desired to provide alternating layers or films of metal and electrical insulating material. Various other modifications of the disclosed processes and embodiments will become apparent to persons skilled in the art without departing from the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. An integrated circuit device comprising a plurality of circuit elements disposed at a common face of a substrate, each circuit element including at least one semiconductor region, the semiconductor regions being covered by a protective coating of insulating material disposed on the said surface of the substrate, a plurality of superposed interconnection levels, separated by one or more layers of insulating material except at areas of interconnection between the respective levels, the lowermost interconnection level being disposed on the said protective coating and forming desired interconnections between selected ones of said semiconductor regions through apertures in the protective coating, in which the interconnection levels

each comprise a layer of molybdenum, titanium, tantalum, rhodium, cobalt, nickel or aluminum, and in which the uppermost interconnection level is overlaid by a layer of gold.

2. An integrated circuit device as claimed in Claim 1, in which the lowermost interconnection level is connected to the uppermost interconnection level through an aperture in an insulating layer separating the two said interconnection levels.

3. An integrated circuit device as claimed in Claim 2, in which the lowermost and uppermost interconnection levels are molybdenum layers making direct contact with each other through the aperture in the said insulating layer.

4. An integrated circuit device as claimed in Claim 2, in which the lowermost and uppermost interconnection levels are molybdenum layers making contact with each other through a layer of gold disposed in the aperture of the said insulating layer.

5. An integrated circuit device as claimed in Claim 1, in which the upper surface of the or each interconnection level other than the uppermost level is oxidized prior to formation of the said insulating layer thereon.

6. An integrated circuit device as claimed in Claim 5, in which the superposed interconnection levels are connected with each other by layers of oxidation resistant metal disposed in an aperture of the or each said insulating layer.

7. An integrated circuit device as claimed in Claim 6, wherein the oxidation resistant metal is gold.

8. An integrated circuit device as claimed in any preceding claim, in which the said circuit elements are formed as integral parts of a single body of semiconductor material.

9. An integrated circuit device according to Claim 8, in which the said body is composed of silicon.

10. An integrated circuit device as claimed in any preceding claim in which the said insulating medium is composed of silicon oxide.

11. An integrated circuit device as claimed in any preceding claim, in which the said protective coating is composed of silicon oxide.

12. An integrated circuit device as claimed in Claim 8 or Claim 9, in which the said insulating medium is composed of silicon nitride, aluminum oxide or tantalum oxide.

13. An integrated circuit device as claimed in any preceding claim, in which the lowermost interconnection level di-



rectly contacts the said selected semiconductor regions.

14. An integrated circuit device as claimed in any of Claims 1—12, in which the lowermost interconnection pattern makes ohmic connection with the selected regions through interposed metallic regions.

15. An integrated circuit device as claimed in Claim 14, in which the said interposed metallic regions are composed of aluminum or platinum-silicide.

16. An integrated circuit device according to Claim 1, substantially as described herein with reference to and as illustrated by Figs. 1—3 in conjunction with Figs. 4—6 or in conjunction with Figs. 7—10 of the accompanying drawings.

17. A method for providing ohmic contacts and multi-level electrical interconnections in an integrated circuit having a plurality of circuit elements formed as integral parts of a body, each circuit element including at least one semiconductor region extending to a surface of the body beneath an insulating protective coating upon that surface, comprising the steps of:

- a) forming a plurality of apertures in the protective coating to expose the surfaces of selected ones of the semiconductor regions,
- b) depositing a first film of molybdenum upon the protective coating and within the said apertures to contact the selected regions,
- c) selectively etching the first film to provide ohmic contacts to the selected regions and a plurality of first level interconnectors electrically interconnecting desired groups of the selected regions,
- d) depositing a layer of insulating medium overlying each of the said first level interconnectors,
- e) selectively etching the layer of insulating medium to expose a portion of one or more of the first level interconnectors, and
- f) selectively forming a second level interconnector upon the insulating medium to electrically interconnect with the exposed portion of the or each said first level interconnector, the second level interconnector comprising a layer of molybdenum overlaid by a layer of gold.

18. A method for providing ohmic contacts and multi-level electrical interconnections in a semiconductor integrated circuit having a plurality of electrical cir-

cuit elements formed as integral parts of a body, each circuit element including a semiconductor region extending to a surface of the body beneath an insulating protective coating upon that surface, comprising the steps of:

- a) forming a plurality of apertures in the protective coating to expose the surface of selected ones of the semiconductor regions,
- b) depositing a first film of molybdenum upon the protective coating and within the said apertures to contact the selected regions, and depositing a second film of gold upon the first film,
- c) selectively etching the first and second films to provide ohmic contacts to the selected regions and a plurality of first level interconnectors electrically interconnecting desired groups of the selected regions,
- d) selectively removing the second film from each of the first level interconnectors except for a discrete portion of gold overlying a corresponding portion of molybdenum of one or more of the first level interconnectors, the remainder of the first film being exposed, and converting only the surface portions of the exposed molybdenum to molybdenum oxide, the or each said discrete portion of gold serving to mask the oxidizing of the underlying molybdenum region,
- e) depositing a layer of insulating medium overlying the first level interconnectors,
- f) selectively etching the layer of insulating medium to expose the surface of the or each said discrete portion of gold, and
- g) selectively forming a second level interconnector upon the insulating medium to electrically interconnect with the or each first level interconnector through the or each said gold portion, the second level interconnector comprising a film of molybdenum deposited upon the insulating medium and a film of gold deposited on that said molybdenum film.

19. A method as claimed in Claim 17 or Claim 18, in which following the said step a) but before the said step b), a film of aluminum or platinum silicide is deposited in the apertures in the said protective coating formed by the said step a).

20. A method as claimed in any of Claims 17—19, in which the said body is composed of silicon and in which the said protective coating and insulating



medium is comprised of silicon oxide.

21. A method according to Claim 18
or Claim 19, substantially as described
herein with reference to the accompany-
5 ing drawings.

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Printed for Her Majesty's Stationery Office by Burgess & Son (Abingdon), Ltd.—1970.
Published at The Patent Office, 25 Southampton Buildings, London, WC2A 1AY
from which copies may be obtained.

