

CLAIMS

I/We claim:

1. A memory structure, comprising:
an access line extending along a first direction;
a first contact line and a second contact line extending along a second direction different than the first direction, the first and second contact lines being generally parallel to each other;
a memory node including:
a first memory cell electrically connected between the access line and the first contact line to form a first circuit; and
a second memory cell electrically connected between the access line and the second contact line to form a second circuit electrically independent from the first circuit.
2. The memory structure of claim 1 wherein the first and second contact lines form an oblique angle with the access line.
3. The memory structure of claim 1 wherein
the first and second directions form an oblique angle of about 63° ; and
the memory node further includes:
a first rectifier having a first input terminal and a first output terminal;
a second rectifier having a second input terminal and a second output terminal;
the first input terminal of the first rectifier and the second input terminal of the second rectifier being electrically connected to the access line;
the first and second memory cells including chalcogenide glass;
the first memory cell being electrically connected to the first output terminal of the first rectifier and the first contact line; and
the second memory cell is electrically connected to the second output terminal of the second rectifier and the second contact line.

4. The memory structure of claim 1 wherein:
the first and second directions form an oblique angle of about 63° ; and
the first and second circuits are electrically isolated from each other.
5. The memory structure of claim 1 wherein
the first and second directions form an oblique angle; and
the memory node further includes:
a first rectifier having a first input terminal and a first output terminal;
a second rectifier having a second input terminal and a second output terminal;
the first input terminal of the first rectifier and the second input terminal of the
second rectifier are electrically connected to the access line; and
the first output terminal of the first rectifier and the second output terminal of the
second rectifier are electrically connected to the first and second memory
cells, respectively.
6. The memory structure of claim 1, further comprising:
a first contact rectifier between the first memory cell and the first contact line; and
a second contact rectifier between the second memory cell and the second contact line.
7. The memory structure of claim 1 wherein
the first and second directions form an oblique angle;
the memory node further includes:
a first rectifier having a first input terminal and a first output terminal;
a second rectifier having a second input terminal and a second output terminal;
the first input terminal of the first rectifier and the second input terminal of the
second rectifier are electrically connected to the access line; and
the first output terminal of the first rectifier and the second output terminal of the
second rectifier are electrically connected to the first and second memory
cells, respectively; and
the memory structure, further comprising a first contact rectifier between the first
memory cell and the first contact line; and
a second contact rectifier between the second memory cell and the second contact line.

8. The memory structure of claim 1 wherein the first and second contact lines are generally orthogonal relative to the access line.

9. The memory structure of claim 1 wherein:
the first and second contact lines are generally orthogonal relative to the access line;
the memory node further includes:
a first rectifier having a first input terminal and a first output terminal;
a second rectifier having a second input terminal and a second output terminal;
and
the first input terminal of the first rectifier and the second input terminal of the second rectifier are electrically connected to the access line.

10. A memory structure, comprising:
a plurality of access lines extending along a first direction;
a plurality of contact lines extending along a second direction different from the first direction, the individual contact lines and the individual access lines forming a plurality of pairs of access and contact lines;
a plurality of memory nodes electrically connected to the access and contact lines, the individual memory nodes including:
a first memory cell electrically connected between a first pair of access and contact lines; and
a second memory cell electrically connected between a second pair of access and contact lines, the first and second pairs of access and contact lines are electrically isolated from each other.

11. The memory structure of claim 10 wherein the contact lines form an oblique angle with the access lines.

12. The memory structure of claim 10 wherein
the individual memory nodes further include:
a first rectifier having a first input terminal and a first output terminal;
a second rectifier having a second input terminal and a second output terminal;

the first input terminal of the first rectifier and the second input terminal of the second rectifier are electrically connected to the access line; and
the first output terminal of the first rectifier and the second output terminal of the second rectifier are electrically connected to the first and second memory cells, respectively.

13. The memory structure of claim 10, further comprising:

a first contact rectifier between the first memory cell and the individual contact lines;
and
a second contact rectifier between the second memory cell and the individual contact lines.

14. The memory structure of claim 10 wherein the contact lines are generally orthogonal relative to the access lines.

15. The memory structure of claim 10 wherein:

the contact lines are generally orthogonal relative to the access lines;

the contact lines include a first contact line and a second contact line;

the access lines include a first access line and a second access line;

the memory nodes include a first memory node and a second memory node;

the first memory node includes:

a first memory cell electrically connected to the first contact line;

a first rectifier having a first input terminal electrically connected to the first access line and a first output terminal electrically connected to the first memory cell, the first contact line, the first memory cell, the first rectifier, and the first access line forming a first circuit;

a second memory cell electrically connected to the second contact line; and

a second rectifier having a second input terminal electrically connected to the first access line and a second output terminal electrically connected to the second memory cell, the second contact line, the second memory cell, the second rectifier, and the first access line forming a second circuit; and

the second memory node includes:

a first memory cell electrically connected to the first contact line;
a first rectifier having a first input terminal electrically connected to the second access line and a first output terminal electrically connected to the first memory cell, the first contact line, the first memory cell, the first rectifier, and the second access line forming a third circuit;
a second memory cell electrically connected to the second contact line;
a second rectifier having a second input terminal electrically connected to the second access line and a second output terminal electrically connected to the second memory cell, the second contact line, the second memory cell, the second rectifier, and the second access line forming a fourth circuit;
the first, second, third, and fourth circuits are electrically isolated from one another.

16. The memory structure of claim 10 wherein:
the contact lines are generally orthogonal relative to the access lines;
the contact lines form a first pair of contact lines and a second pair of contact lines adjacent to the first pair of contact lines; and
the first and second pairs of contact lines are electrically isolated from each other.

17. The memory structure of claim 10 wherein:
the contact lines are generally orthogonal relative to the access lines;
the contact lines form a first pair of contact lines and a second pair of contact lines adjacent to the first pair of contact lines;
the memory nodes include a first memory node electrically connected to one of the access lines and the first pair of contact lines, and a second memory node electrically connected to the one of the access lines and the second pair of contact lines; and
the first and second memory nodes are electrically isolated from each other.

18. The memory structure of claim 10 wherein:
the contact lines are generally orthogonal relative to the access lines;
the contact lines include first and second contact lines;
the access lines include first and second access lines;

the memory nodes include a first memory node electrically connected to the first access line and the first and second contact lines, and a second memory node electrically connected to the second access line and the first and second contact lines; and the first and second memory nodes are electrically isolated from each other.

19. The memory structure of claim 10 wherein:

the contact lines are generally orthogonal relative to the access lines;

the contact lines include first and second contact lines;

the access lines include first and second access lines;

the memory nodes include a first memory node and a second memory node;

the first memory node includes:

a first memory cell electrically connected between the first access line and the first contact line forming a first circuit; and

a second memory cell electrically connected between the first access line and the second contact line forming a second circuit;

the second memory node includes:

a first memory cell electrically connected between the second access line and the first contact line forming a third circuit; and

a second memory cell electrically connected between the second access line and the second contact line forming a fourth circuit; and

the first, second, third, and fourth circuits are electrically isolated from one another.

20. The memory structure of claim 10 wherein:

the contact lines are generally orthogonal relative to the access lines;

the contact lines include first and second contact lines;

the access lines include first and second access lines;

the memory nodes include a first memory node and a second memory node;

the first memory node includes:

a first memory cell and a first rectifier electrically connected between the first access line and the first contact line forming a first circuit; and

a second memory cell and a second rectifier electrically connected between the first access line and the second contact line forming a second circuit;

the second memory node includes:

- a first memory cell and a first rectifier electrically connected between the second access line and the first contact line forming a third circuit; and
- a second memory cell and a second rectifier electrically connected between the second access line and the second contact line forming a fourth circuit; and

the first, second, third, and fourth circuits are electrically isolated from one another.

21. A memory structure, comprising:

a dielectric having a first sidewall, a second sidewall, and a third wall between the first and second sidewalls;

a first memory cell on the first sidewall;

a second memory cell on the second sidewall; and

a doped material on the third wall of the dielectric, the doped material having a first portion, a second portion, and a third portion between the first and second portions, the first and second portions including a first dopant, the third portion including a second dopant different than the first dopant.

22. The memory structure of claim 21 wherein:

the dielectric has a generally rectangular shape;

the first and second memory cells include chalcogenide glass;

the first and second portions of the doped material include an N-type material; and

the third portion of the doped material includes a P-type material.

23. The memory structure of claim 21 wherein the first and second memory cells include a layer of chalcogenide glass.

24. The memory structure of claim 21 wherein:

the dielectric is a first dielectric;

the first and second memory cells have an L shape; and

the memory structure further includes a second dielectric partially enclosed by the first and second memory cells.

25. A method for manufacturing a memory structure, comprising:
forming a first contact line and a second contact line in a substrate material, the first and second contact lines extending along a first direction;
electrically connecting a memory node to the first and second contact lines, the memory node including a first memory cell electrically connected to the first contact line and a second memory cell electrically connected to a second contact line;
forming an access line in and/or on the substrate material, the access line extending along a second direction different from the first direction; and
electrically connecting the access line to the first and second memory cells, the access line, the first memory cell, and the first contact line forming a first circuit, the access line, the second cell, and the second contact line forming a second circuit electrically isolated from the first circuit.

26. The method of claim 25 wherein:
forming a first contact line and a second contact line includes:
depositing a conductive material onto the substrate material;
removing a portion of the deposited conductive material;
forming the first and second contact lines with the remaining conductive material; and
insulating the first and second contact lines with an insulation material;
electrically connecting a memory node to the first and second contact lines includes:
depositing a first dielectric onto the first and second contact lines;
forming a plurality of openings in the first dielectric, the openings exposing the first and second contact lines; and
depositing a first conductive material in the openings, and thereby forming a plurality of conductive contacts between the memory node and the first and second contact lines; and
forming an access line in and/or on the substrate material includes:
depositing a second dielectric onto the conductive contacts and the memory node;
forming a trench in the second dielectric, the trench exposing at least a portion of the memory node and extending along a second direction that is at an oblique angle with the first direction; and

depositing a second conductive material in the trench, and thereby forming the access line.

27. The method of claim 25 wherein:

forming a first contact line and a second contact line includes:

depositing a conductive material onto the substrate material;

removing a portion of the deposited conductive material;

forming the first and second contact lines with the remaining conductive material; and

insulating the first and second contact lines with an insulation material; and

forming an access line in the substrate material includes:

depositing a dielectric onto the memory node;

forming a trench in the dielectric, the trench exposing at least a portion of the memory node and extending along a second direction that is at an angle of about 63° with the first direction; and

depositing a conductive material in the trench, and thereby forming the access line.

28. The method of claim 25 wherein:

forming a first contact line and a second contact line includes:

depositing a conductive material onto the substrate material;

removing a portion of the deposited conductive material;

forming the first and second contact lines with the remaining conductive material, the first and second contact lines having a first width a therebetween; and

insulating the first and second contact lines with an insulation material;

forming an access line in the substrate material includes:

depositing a dielectric onto the memory node;

forming a first trench and a second trench in the dielectric, the first and second trenches having a second width b therebetween and extending along a second direction forming an angle α according to the following formula:

$$\alpha = \arctan\left(\frac{b}{a}\right); \text{ and}$$

depositing a conductive material in the first and second trenches, and thereby forming a first access line and a second access line.

29. The method of claim 25 wherein:

forming a first contact line and a second contact line includes:

depositing a conductive material onto the substrate material;

removing a portion of the deposited conductive material;

forming the first and second contact lines with the remaining conductive material; and

insulating the first and second contact lines with an insulation material; and

forming an access line in the substrate material includes:

depositing a dielectric onto the memory node;

forming a trench in the dielectric, the trench exposing at least a portion of the memory node and extending along a second direction that is generally orthogonal to the first direction; and

depositing a conductive material in the trench, and thereby forming the access line.

30. A method for manufacturing a memory structure, comprising:

forming a column on a substrate material, the column having of a dielectric in direct contact with the substrate material and a doped material on the dielectric, the column having a first sidewall and a second sidewall;

depositing a memory material on the column and the substrate material; and

selectively removing a portion of the memory material from the column and the substrate material such that a first portion of the memory material remains on the first sidewall and a second portion of the memory material remains on the second sidewall.

31. The method of claim 30 wherein forming a column on a substrate material includes:

depositing the dielectric on the substrate;

depositing the doped material on the dielectric; and

selectively removing a portion of the dielectric and the doped material to form the column.

32. The method of claim 30 wherein forming a column on a substrate material includes:

depositing the dielectric on the substrate;

depositing the doped material on the dielectric, the doped material including a first dopant;

selectively removing a portion of the dielectric and the doped material to form the column; and

the method further includes selectively introducing a second dopant into the doped material, the second dopant being different from the first dopant.

33. The method of claim 30 wherein forming a column on a substrate material includes:

depositing the dielectric on the substrate;

depositing the doped material on the dielectric, the doped material including an N-type dopant;

selectively removing a portion of the dielectric and the doped material to form the column; and

the method further includes selectively introducing a P-type dopant into the doped material and forming a first P/N junction and a second P/N junction in the doped material.

34. The method of claim 30 wherein depositing a memory material includes depositing a memory material containing chalcogenide glass.

35. The method of claim 30 wherein:

the column includes a third wall between the first and second sidewalls;

depositing a memory material includes depositing a memory material containing chalcogenide glass onto the first and second sidewalls and the third wall; and

selectively removing a portion of the memory material includes selectively removing a portion of the memory material from the third wall of the column and the substrate material such that the first portion of the memory material remains on the first sidewall and the second portion of the memory material remains on the second sidewall.

36. The method of claim 30 wherein:
the column includes a third wall between the first and second sidewalls;
depositing a memory material includes depositing a memory material containing chalcogenide glass onto the first and second sidewalls and the third wall; and
selectively removing a portion of the memory material includes spacer etching the memory material such that the first portion of the memory material remains on the first sidewall and the second portion of the memory material remains on the second sidewall.

37. The method of claim 30 wherein:
the dielectric is a first dielectric; and
the method further includes:
depositing a second dielectric on the memory material; and
selectively removing a portion of the memory material by spacer etching the memory material and the second dielectric such that a first portion of the memory material and the second dielectric remains on the first sidewall and a second portion of the memory material and the second dielectric remains on the second sidewall.

38. The method of claim 30 wherein:
the dielectric is a first dielectric; and
the method further includes:
depositing a second dielectric on the memory material;
selectively removing a portion of the memory material by spacer etching the memory material and the second dielectric such that a first portion of the memory material and the second dielectric remains on the first sidewall

and a second portion of the memory material and the second dielectric remains on the second sidewall; and
removing a portion of the column after removing a portion of the memory material, and thereby forming a plurality of discrete nodes.

CLAIMS

I/We claim:

1. A memory structure, comprising:
 - an access line extending along a first direction;
 - a first contact line and a second contact line extending along a second direction different than the first direction, the first and second contact lines being generally parallel to each other;
 - a memory node including:
 - a first memory cell electrically connected between the access line and the first contact line to form a first circuit;
 - a second memory cell electrically connected between the access line and the second contact line to form a second circuit electrically independent from the first circuit; and
 - a rectifier device between the access line and the first and second memory cells, wherein the first and second circuits include a common circuit path through at least a portion of the rectifier device.
2. The memory structure of claim 1 wherein the first and second contact lines form an oblique angle with the access line.
3. The memory structure of claim 1 wherein
 - the first and second directions form an oblique angle of about 63° ; and
 - the rectifier device of the memory node further includes:
 - a first rectifier having an input terminal and a first output terminal;
 - a second rectifier having the input terminal and a second output terminal;
 - the input terminal of the first and second rectifiers being electrically connected to the access line;
 - the first and second memory cells including chalcogenide glass;
 - the first memory cell being electrically connected to the first output terminal of the first rectifier and the first contact line; and

the second memory cell is electrically connected to the second output terminal of the second rectifier and the second contact line.

4. The memory structure of claim 1 wherein:

the first and second directions form an oblique angle of about 63°; and
the first and second circuits are electrically isolated from each other.

5. The memory structure of claim 1 wherein

the first and second directions form an oblique angle; and
the rectifier device of the memory node further includes:

a first rectifier having an input terminal and a first output terminal;

a second rectifier having the input terminal and a second output terminal;

the input terminal of the first and second rectifiers is electrically connected to the access line; and

the first output terminal of the first rectifier and the second output terminal of the second rectifier are electrically connected to the first and second memory cells, respectively.

6. The memory structure of claim 1 wherein

the first and second directions form an oblique angle;

the rectifier device of the memory node further includes:

a first rectifier having an input terminal and a first output terminal;

a second rectifier having the input terminal and a second output terminal;

the input terminal of the first and second rectifiers is electrically connected to the access line; and

the first output terminal of the first rectifier and the second output terminal of the second rectifier are electrically connected to the first and second memory cells, respectively; and

the memory structure, further comprising a first contact rectifier between the first memory cell and the first contact line; and

a second contact rectifier between the second memory cell and the second contact line.

7. The memory structure of claim 1 wherein the first and second contact lines are generally orthogonal relative to the access line.

8. The memory structure of claim 1 wherein:

the first and second contact lines are generally orthogonal relative to the access line;
the memory node further includes:

a first rectifier having a first input terminal and a first output terminal;

a second rectifier having a second input terminal and a second output terminal;

and

the first input terminal of the first rectifier and the second input terminal of the second rectifier are electrically connected to the access line.

9. The memory structure of claim 1 wherein the rectifier device includes two back-to-back P/N junction devices.

10. The memory structure of claim 1 wherein the rectifier device includes two back-to-back N/P junction devices.

11. The memory structure of claim 1 wherein:

the first memory cell includes a first region of chalcogenide glass; and

the second memory cell includes a second region of chalcogenide glass,

wherein the first and second regions of chalcogenide glass are mechanically isolated from one another.

12. The memory structure of claim 1, further comprising:

a first contact rectifier between the first memory cell and the first contact line; and

a second contact rectifier between the second memory cell and the second contact line.

13. The memory structure of claim 12 wherein:

the first contact rectifier comprises a first P/N diode; and

the second contact rectifier comprises a second P/N diode.

14. The memory structure of claim 12 wherein:

the first contact rectifier is buried beneath at least a portion of the first contact line; and
the second contact rectifier is buried beneath at least a portion of the second contact line.

15. A memory structure, comprising:

a plurality of access lines extending along a first direction;

a plurality of contact lines extending along a second direction different from the first direction, the individual contact lines and the individual access lines forming a plurality of pairs of access and contact lines;

a plurality of memory nodes electrically connected to the access and contact lines, the individual memory nodes including:

a rectifier device including a first junction device and second junction device, wherein the first junction device includes a first doping region arranged with a second doping region to define a first junction, and wherein the second junction device includes a third doping region arranged with the second doping region to define a second junction;

a first memory cell electrically connected between a first pair of access and contact lines with the rectifier device between the first pair of access lines and the first memory cell; and

a second memory cell electrically connected between a second pair of access and contact lines with the rectifier device between the second pair of access lines and the second memory cell, the first and second pairs of access and contact lines are electrically isolated from each other, wherein the first and second memory cells are connected to the rectifier device, the same access line and adjacent contact lines.

16. The memory structure of claim 15 wherein the contact lines form an oblique angle with the access lines.

17. The memory structure of claim 15 wherein

the rectifier device of the individual memory nodes further include:

a first rectifier having an input terminal and a first output terminal;

a second rectifier having the input terminal and a second output terminal;
the input terminal of the first and second rectifiers is electrically connected to the access line; and
the first output terminal of the first rectifier and the second output terminal of the second rectifier are electrically connected to the first and second memory cells, respectively.

18. The memory structure of claim 15, further comprising:

a first contact rectifier between the first memory cell and the individual contact lines; and
a second contact rectifier between the second memory cell and the individual contact lines.

19. The memory structure of claim 15 wherein the contact lines are generally orthogonal relative to the access lines.

20. A memory structure, comprising:

a plurality of access lines extending along a first direction;

a plurality of contact lines extending along a second direction that is non-orthogonal to the first direction such that the contact lines are canted relative to the access lines, the individual contact lines and the individual access lines forming a plurality of pairs of access and contact lines;

a plurality of memory nodes electrically connected to the access and contact lines, the individual memory nodes including:

two back-to-back junction devices that share a common doping region;

a first memory cell electrically connected between a first access line and a first contact line with the common doping region of the two back-to-back junction devices between the first access line and the first memory cell;
and

a second memory cell electrically connected between the first access line and a second contact line with the common doping region of the two back-to-back junction devices between the first access line and the second memory cell .

21. The memory structure of claim 20 wherein the contact lines form an angle of about 63° with the access lines.

22. The memory structure of claim 20 wherein the back-to-back junction devices form:

a first rectifier having an input terminal and a first output terminal;

a second rectifier having the input terminal and a second output terminal;

the input terminal of the first and second rectifiers is electrically connected to the first access line; and

the first output terminal of the first rectifier and the second output terminal of the second rectifier are electrically connected to the first and second memory cells, respectively.

23. The memory structure of claim 20, further comprising:

a first contact rectifier between the first memory cell and the individual contact lines; and

a second contact rectifier between the second memory cell and the individual contact lines.

24. The memory structure of claim 20 wherein at least one of the first and second memory cells includes chalcogenide glass.