WHAT IS CLAIMED IS:

1. A display apparatus, comprising:

a first substrate;

a plurality of data lines, configured on the first substrate and arranged in a first direction;

a plurality of first gate lines, configured on the first substrate, and arranged in a second direction, wherein the first direction crisscrosses the second direction;

a plurality of pixel structures, configured on the first substrate and electrically connected to the data lines and the first gate lines;

a plurality of second gate lines, configured on the first substrate, wherein the data lines and the second gate lines are arranged in the first direction, and the second gate lines are electrically connected to the first gate lines;

a plurality of first common lines, configured on the first substrate, wherein the pixel structures are arranged in a plurality of pixel columns, the pixel columns are arranged in the first direction, each of the first common lines and the corresponding second gate line are configured between two adjacent pixel columns of the pixel columns, the first common line and the corresponding second gate line are configured respectively on the opposite sides of the first gate line which is electrically connected to the second gate line, and the first common line and the corresponding second gate line are structurally separated;

a second substrate, configured to be opposite to the first substrate; and

a display medium, configured between the first substrate and the second substrate.

2. The display apparatus according to claim 1, wherein a signal of the first common line and a gate-off signal of the second gate line are substantially the same.

3. The display apparatus according to claim 1, wherein each of the first gate lines is electrically connected to n number of the second gate lines, n is a positive integer, each of the first gate lines and the n number of the second gate lines have 1^{st} to n^{th} connection points arranged in

sequence in the first direction, the second gate lines include 1^{st} to n^{th} second gate line groups arranged in sequence in the first direction, the second gate lines of m^{th} second gate line group of the 1^{st} to n^{th} second gate line groups and the corresponding first gate lines have m^{th} connection point of the 1^{st} to n^{th} connection points, m is a positive integer, and $n \geq m \geq 1$, and the display apparatus further comprising:

a common electrode, configured on the second substrate and located between the second substrate and the display medium;

a plurality of common pad groups, configured on the first substrate, and configured to correspond respectively to the 1^{st} to n^{th} second gate line groups, wherein the pixel structures have a first side and a second side opposite to each other, the common pad groups are configured on the second side of the pixel structures, and each of the common pad groups includes a plurality of first common pads;

a plurality of first transfer elements, configured respectively on the first common pads of the common pad groups, and electrically connected to the first common pads of the common pad groups and the common electrode;

n number of a plurality of second common pads, configured on the first substrate, and configured to correspond respectively to the 1^{st} to n^{th} second gate line groups, and located on the first side of the pixel structures; and

n number of a plurality of second transfer elements, configured respectively on the n number of the second common pads, and electrically connected to the n number of the second common pads and the common electrode,

wherein a common pad group of the common pad groups and a second common pad of the n number of the second common pads correspond to the same second gate line group, and a potential of the second common pad is greater than a plurality of potentials of the first common pads of the common pad group.

4. The display apparatus according to claim 3, further comprising:

a third common pad, configured on the first substrate, and located on the first side of the pixel structures, wherein the third common pad and the second common pads are arranged in sequence in the first direction and are structurally separated from each other, the third common pad is configured to correspond to the 1^{st} second gate line group of the 1^{st} to n^{th} second gate line groups, and a potential of the third common pad is greater than a plurality of potentials of the corresponding second common pads; and

a third transfer element, configured on the third common pad, and electrically connected to the third common pad and the common electrode.

5. The display apparatus according to claim 1, further comprising:

a plurality of second common lines, configured on the first substrate, and the second gate lines and the second common lines are arranged in the first direction, wherein each of the second common lines is configured between two adjacent pixel columns of the pixel columns;

a first peripheral line, configured on the first substrate and located on a first side of the pixel structures, wherein the first common lines are electrically connected to the first peripheral line; and

a second peripheral line, configured on the first substrate and located on a second side of the pixel structures, wherein two ends of each of the second common lines are electrically connected respectively to the first peripheral line and the second peripheral line.

6. The display apparatus according to claim 1, wherein the first gate lines include an odd number of the first gate lines and an even number of the first gate lines, the odd number of the first gate lines include $(1+2\cdot K)^{th}$ first gate line, K=0, 1,..., p, and p is a positive integer greater than or equal to 2, the even number of the first gate lines include $2L^{th}$ first gate line, L=1, 2,... , q, and q is a positive integer greater than or equal to 3; the second gate lines include 1^{st} to $(p+1)^{th}$ second gate lines and (p+2) to $(p+q+1)^{th}$ second gate lines arranged in sequence in the first

direction; the 1^{st} to $(p+1)^{th}$ second gate lines are electrically connected to the $(1+2\cdot K)^{th}$ first gate line, and the (p+2) to $(p+q+1)^{th}$ second gate lines are electrically connected to the $2L^{th}$ first gate line.

7. The display apparatus according to claim 6, wherein a plurality of connection points of the 1^{st} to $(p+1)^{th}$ second gate lines and the $(1+2\cdot K)^{th}$ first gate line as well as a plurality of connection points of the (p+2) to $(p+q+1)^{th}$ second gate lines and the $2L^{th}$ first gate line are generally distributed along a plurality of diagonal lines parallel to each other.

8. The display apparatus according to claim 6, wherein a plurality of connection points of the 1^{st} to $(p+1)^{th}$ second gate lines and the $(1+2\cdot K)^{th}$ first gate line as well as a plurality of connection points of the (p+2)to $(p+q+1)^{th}$ second gate lines and the $2L^{th}$ first gate line are distributed generally in a V-shaped pattern.

9. A display apparatus, comprising:

a first substrate;

a plurality of data lines, configured on the first substrate and arranged in a first direction;

a plurality of first gate lines, configured on the first substrate, and arranged in a second direction, wherein the first direction crisscrosses the second direction;

a plurality of pixel structures, configured on the first substrate, electrically connected to the data lines and the first gate lines, and arranged in x number of pixel columns and y number of pixel rows, wherein the x number of pixel columns are arranged in the first direction, the y number of pixel rows are arranged in the second direction, and x and y are positive integers greater than 2;

a plurality of second gate lines, configured on the first substrate, wherein the data lines and the second gate lines are arranged in the first direction, and the second gate lines are electrically connected to the first gate lines;

a plurality of first common lines, configured on the first substrate;

a second substrate, configured to be opposite to the first substrate; and

a display medium, configured between the first substrate and the second substrate,

wherein each of the first common lines and the corresponding second gate line are configured between two adjacent pixel columns of the x number of the pixel columns, the first common line and the corresponding second gate line are configured respectively on the opposite sides of the first gate line which is electrically connected to the second gate line, and the first common line and the corresponding second gate line are structurally separated; and

wherein each of the first gate lines is electronically connected to n number of the second gate lines.

10. The display apparatus according to claim 9, wherein a signal of the first common line and a gate-off signal of the second gate line are substantially the same.

11. The display apparatus according to claim 9, wherein each of the first gate lines is electrically connected to the n number of the second gate lines, n is a positive integer, each of the first gate lines and the n number of the second gate lines have 1^{st} to n^{th} connection points arranged in sequence in the first direction, the second gate lines include 1^{st} to n^{th} second gate line groups arranged in sequence in the first direction, and the second gate lines of m^{th} second gate line group of the 1^{st} to n^{th} second gate line groups and the corresponding first gate lines have m^{th} connection point of the 1^{st} to n^{th} connection points, m is a positive integer, and $n \geq m \geq 1$, and the display apparatus further comprising:

a common electrode, configured on the second substrate and is located between the second substrate and the display medium;

a plurality of common pad groups, configured on the first substrate, and configured to correspond respectively to the 1^{st} to n^{th} second gate line groups, wherein the pixel structures have a first side and a second side opposite to each other, the common pad groups are configured on the

second side of the pixel structures, and each of the common pad groups includes a plurality of first common pads;

a plurality of first transfer elements, configured respectively on the first common pads of the common pad groups, and electrically connected to the first common pads of the common pad groups and the common electrode;

n number of a plurality of second common pads, configured on the first substrate, configured to correspond respectively to the 1^{st} to n^{th} second gate line groups, and located on the first side of the pixel structures; and

n number of a plurality of second transfer elements, configured respectively on the n number of the second common pads, and electrically connected to the n number of the second common pads and the common electrode,

wherein a common pad group of the common pad groups and a second common pad of the n number of the second common pads correspond to the same second gate line group, and a potential of the second common pad is greater than a plurality of potentials of the first common pads of the common pad group.

12. The display apparatus according to claim 11, further comprising:

a third common pad, configured on the first substrate, and located on the first side of the pixel structures, wherein the third common pad and the second common pads are arranged in sequence in the first direction and are structurally separated from each other, the third common pad is configured to correspond to the 1st second gate line group of the 1^{st} to n^{th} second gate line groups, and a potential of the third common pad is greater than a plurality of potentials of the corresponding second common pads; and

a third transfer element, configured on the third common pad, and electrically connected to the third common pad and the common electrode.

13. The display apparatus according to claim 9, further comprising:

a plurality of second common lines, configured on the first substrate, and the second gate lines and the second common lines are arranged in the first direction, wherein each of the second common lines is configured between two adjacent pixel columns of the pixel columns;

a first peripheral line, configured on the first substrate and located on a first side of the pixel structures, wherein the first common lines are electrically connected to the first peripheral line; and

a second peripheral line, configured on the first substrate and located on a second side of the pixel structures, wherein two ends of each of the second common lines are electrically connected respectively to the first peripheral line and the second peripheral line.

14. The display apparatus according to claim 9, wherein the first gate lines include an odd number of the first gate lines and an even number of the first gate lines, the odd number of the first gate lines include $(1+2\cdot K)^{th}$ first gate line, K=0, 1,..., p, and p is a positive integer greater than or equal to 2, the even number of the first gate lines include $2L^{th}$ first gate line, L=1, 2,... , q, and q is a positive integer greater than or equal to 3; the second gate lines include 1^{st} to $(p+1)^{th}$ second gate lines and $(p+2)$ to $(p+q+1)^{th}$ second gate lines arranged in sequence in the first direction; the 1^{st} to $(p+1)^{th}$ second gate lines are electrically connected to the $(1+2\cdot K)^{th}$ first gate line, and the $(p+2)$ to $(p+q+1)^{th}$ second gate lines are electrically connected to the $2L^{th}$ first gate line.

15. The display apparatus according to claim 14, wherein a plurality of connection points of the 1^{st} to $(p+1)^{th}$ second gate lines and the $(1+2\cdot K)^{th}$ first gate line as well as a plurality of connection points of the $(p+2)$ to $(p+q+1)^{th}$ second gate lines and the $2L^{th}$ first gate line are generally distributed along a plurality of diagonal lines parallel to each other.

16. The display apparatus according to claim 14, wherein a plurality of connection points of the 1^{st} to $(p+1)^{th}$ second gate lines and the $(1+2\cdot K)^{th}$ first gate line as well as a plurality of connection

points of the (p+2) to $(p+q+1)^{th}$ second gate lines and the $2L^{th}$ first gate line are distributed generally in a V-shaped pattern.