ABSTRACT

METHOD FOR FABRICATING A MOS DEVICE

A method of fabricating a MOS device having raised source/drain, raised isolation regions having isolation spacers, and a gate conductor having gate spacers is achieved. A layer of gate silicon oxide is grown over the surface of a semiconductor structure. A polysilicon layer is deposited overlying the gate silicon oxide layer. The polysilicon layer, gate silicon oxide layer and semiconductor structure are patterned and etched to form trenches. The trenches are filled with an isolation material to at least a level even with a top surface of the polysilicon layer to form raised isolation regions. The remaining polysilicon layer is patterned to remove polysilicon adjacent the raised isolation regions forming a gate conductor between the raised isolation regions. The gate conductor and the raised isolation regions having exposed sidewalls. The gate oxide layer between the gate conductor and raised isolation regions is removed. Isolation spacers are formed on the exposed sidewalls of the raised isolation regions and gate spacers are formed on the exposed sidewalls of the gate conductor. A layer of silicon is deposited and patterned to form raised source and drain adjacent the gate spacers with source and drain being doped to form a MOS device.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)