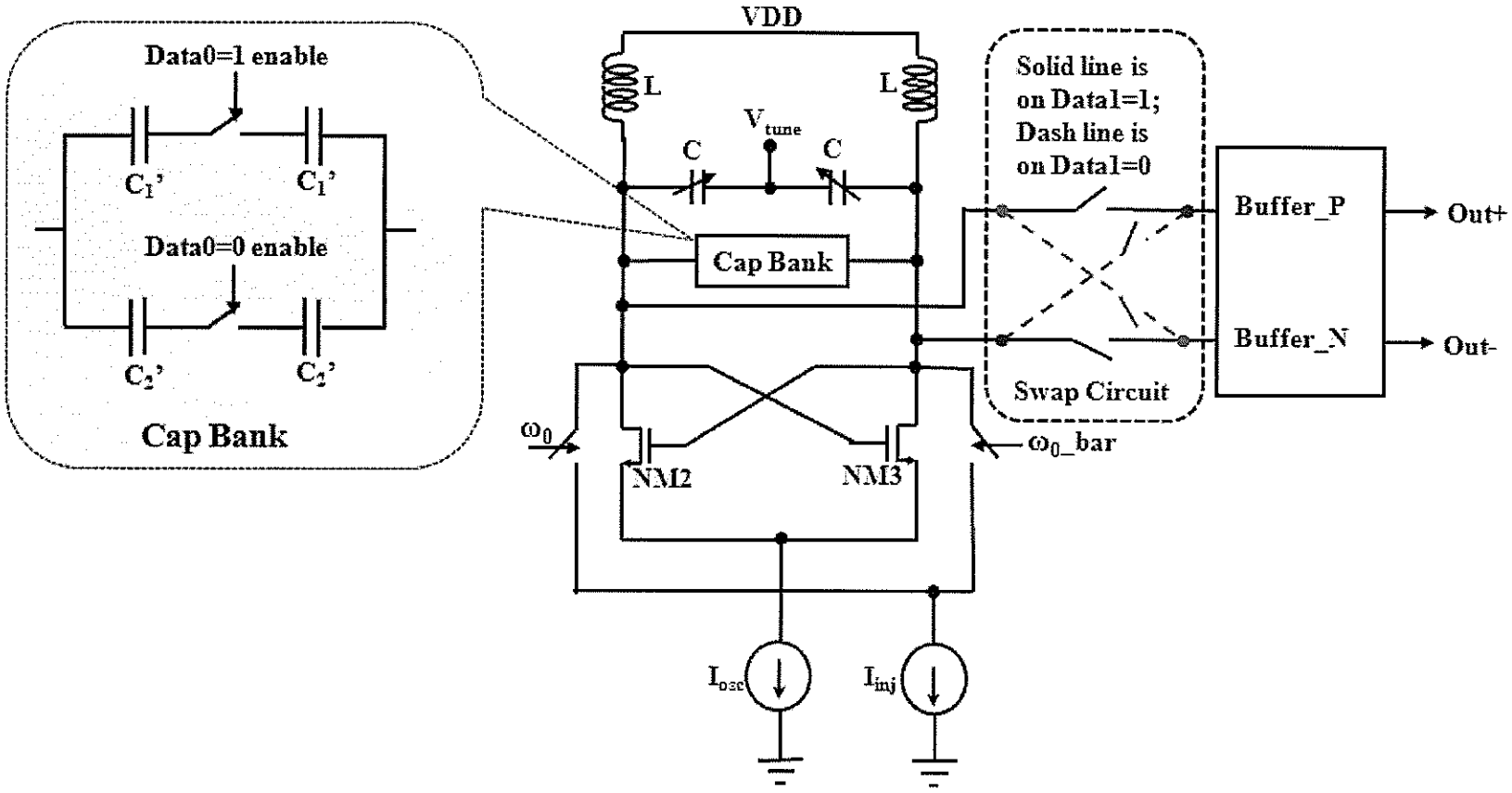
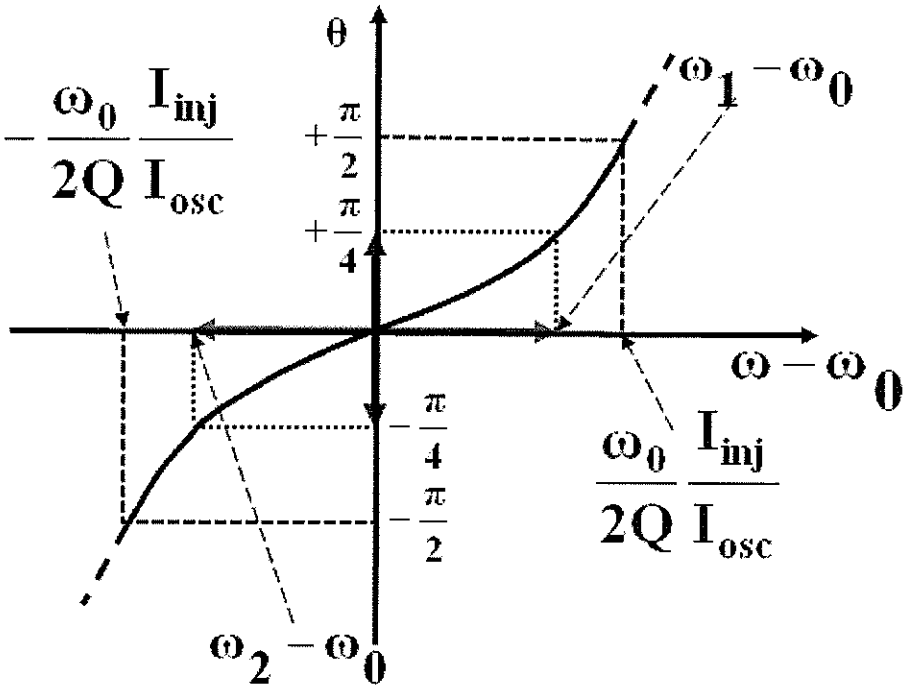

Data0=1 enable
C1'
C1'
Data0=0 enable
C2'
C2'
Cap Bank
VDD
L
L
Vtune
C
C
Cap Bank
Solid line is on Data1=1; Dash line is on Data1=0
Buffer_P
Buffer_N
Out+
Out-
Swap Circuit
ω0
ω0_bar
NM2
NM3
Iosc
Iinj

Fig. 1




$$\omega_1 = \frac{1}{\sqrt{LC_1}} = \frac{1}{\sqrt{L(C_1' + C)}}$$

$$\omega_2 = \frac{1}{\sqrt{LC_2}} = \frac{1}{\sqrt{L(C_2' + C)}}$$

**Fig. 2**

| Data1 | Data0 | Output Phase |
|---|---|---|
| 1 | 1 | 45° |
| 1 | 0 | -135° |
| 0 | 0 | 135° |
| 0 | 1 | -45° |

Fig. 3

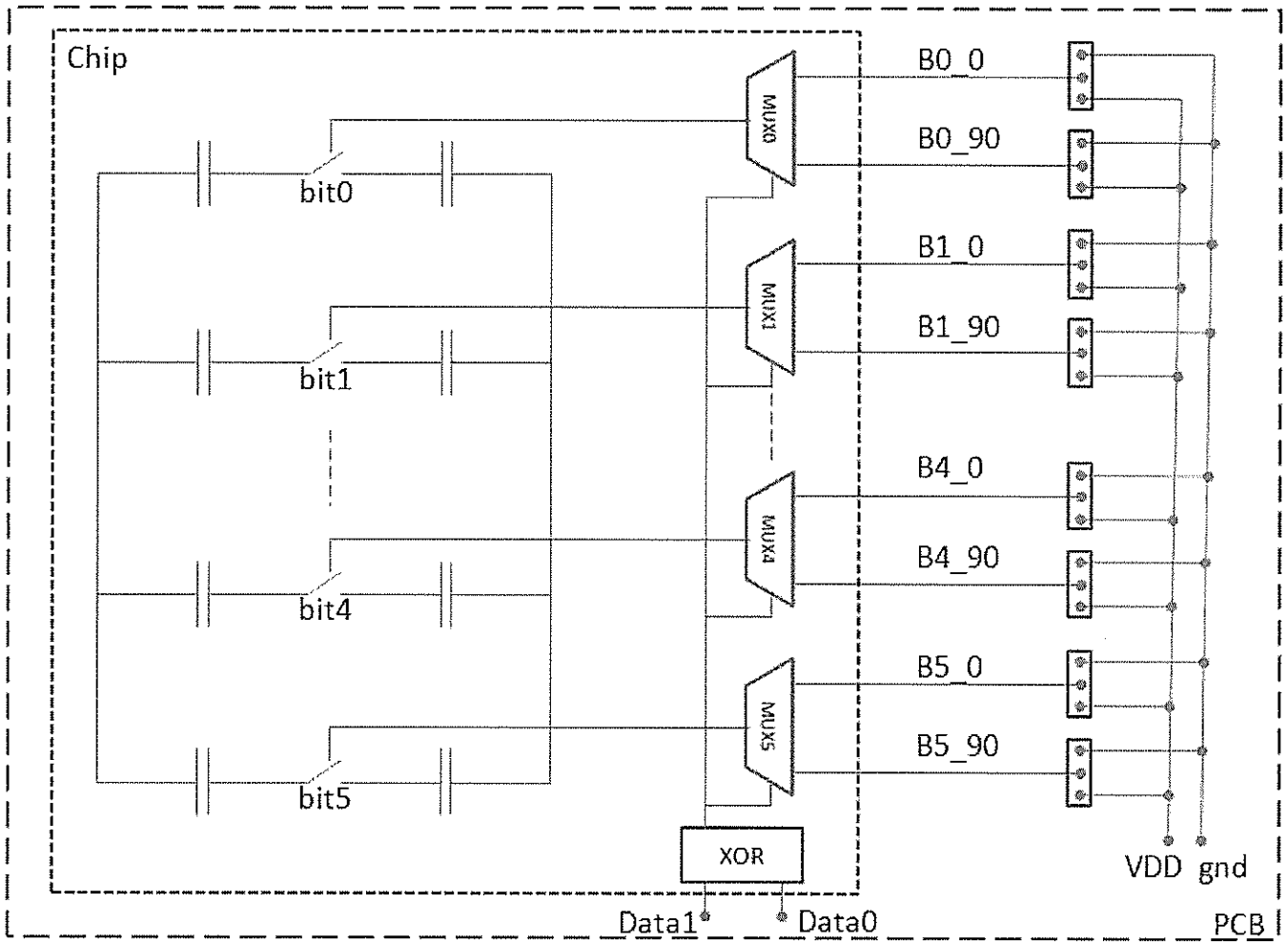

Chip
bit0
bit1
bit4
bit5
MUX0
MUX1
MUX4
MUX5
XOR
B0_0
B0_90
B1_0
B1_90
B4_0
B4_90
B5_0
B5_90
VDD
gnd
Data1
Data0
PCB

**Fig. 4**

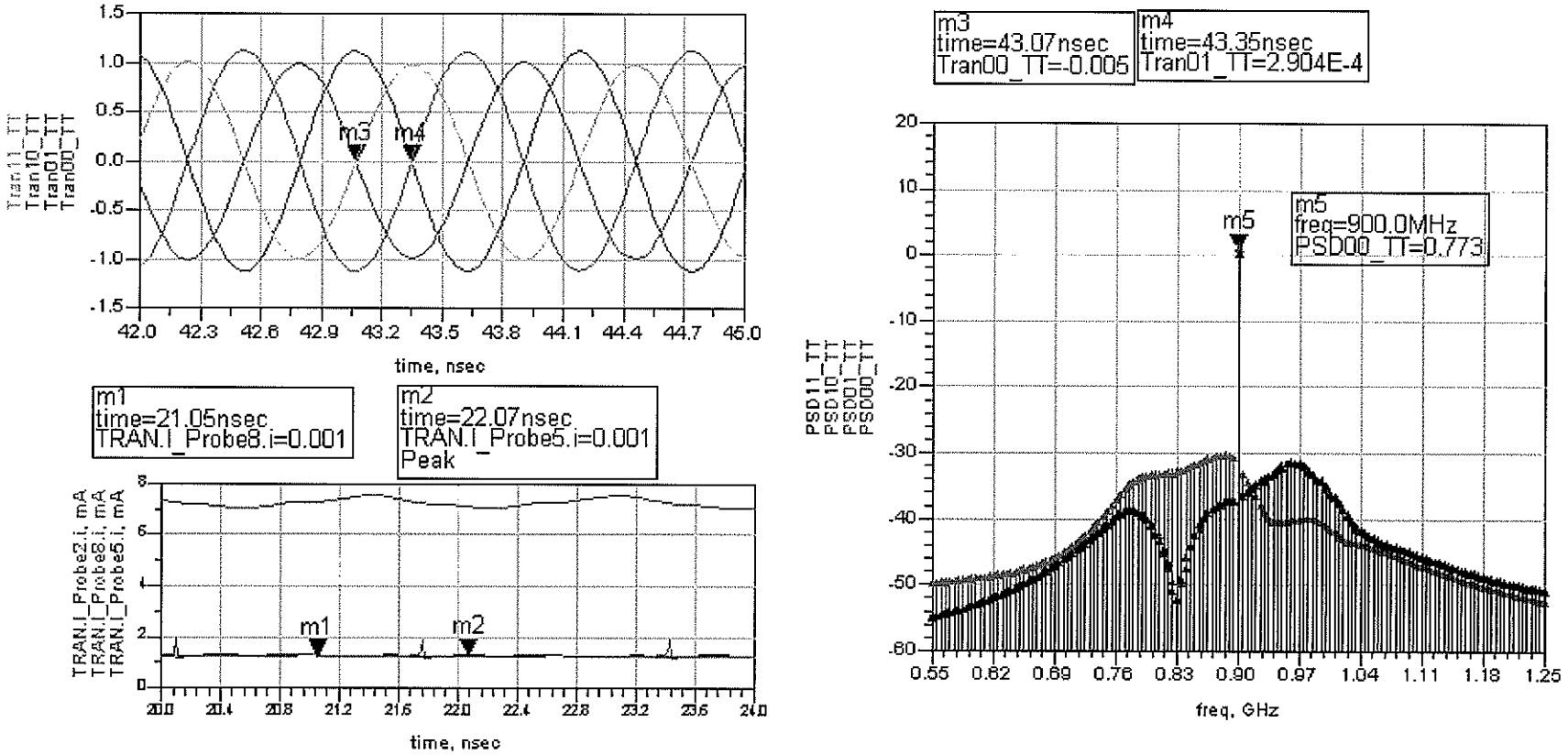
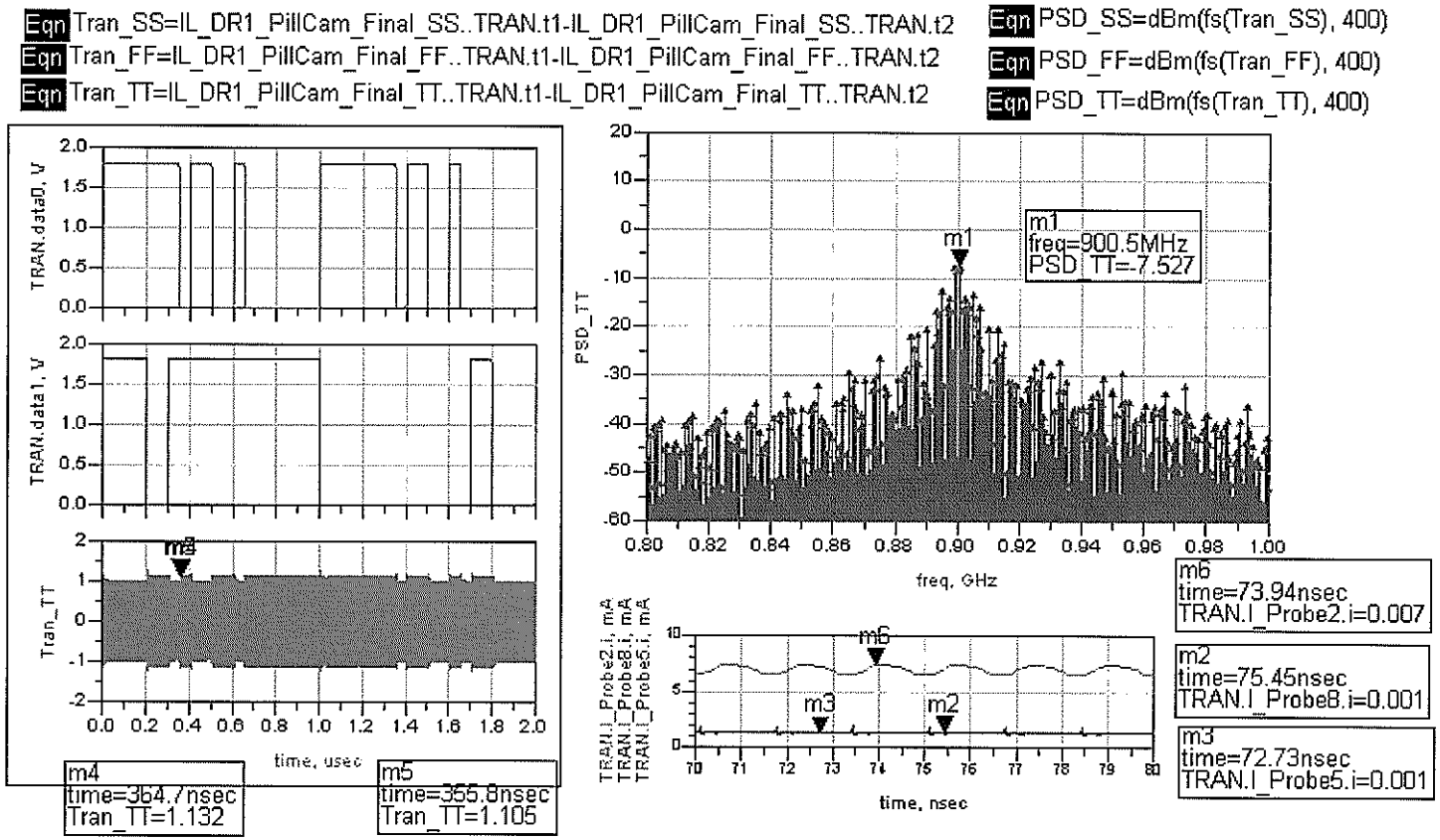

Tran11_TT
Tran10_TT
Tran01_TT
Tran00_TT
m3
m4
time, nsec
m1
time=21.05nsec
TRAN.I_Probe8.i=0.001
m2
time=22.07nsec
TRAN.I_Probe5.i=0.001
Peak
TRAN.I_Probe2.i, mA
TRAN.I_Probe8.i, mA
TRAN.I_Probe5.i, mA
m1
m2
time, nsec
m3
time=43.07nsec
Tran00_TT=-0.005
m4
time=43.35nsec
Tran01_TT=2.904E-4
PSD11_TT
PSD10_TT
PSD01_TT
PSD00_TT
m5
m5
freq=900.0MHz
PSD00_TT=0.773
freq, GHz

**Fig. 5**




| | Vpp (V) | Icore (mA) | Tsettle (ns) | Pout (dBm) | Varamp (V) | Varphi (Degree) | Icon (mA) |
|---|---|---|---|---|---|---|---|
| TT | 2.11 | 2.8 | 6.7 | -7.5 | 0.2 | + - 2 | 7 |
| FF | 3.35 | 3.89 | 11 | -3.13 | 0.01 | + -3 | 11 |
| SS | 0.5 | 2 | 12 | -18.9 | 0.09* | + - 3 | 3.61 |

**Fig. 6**

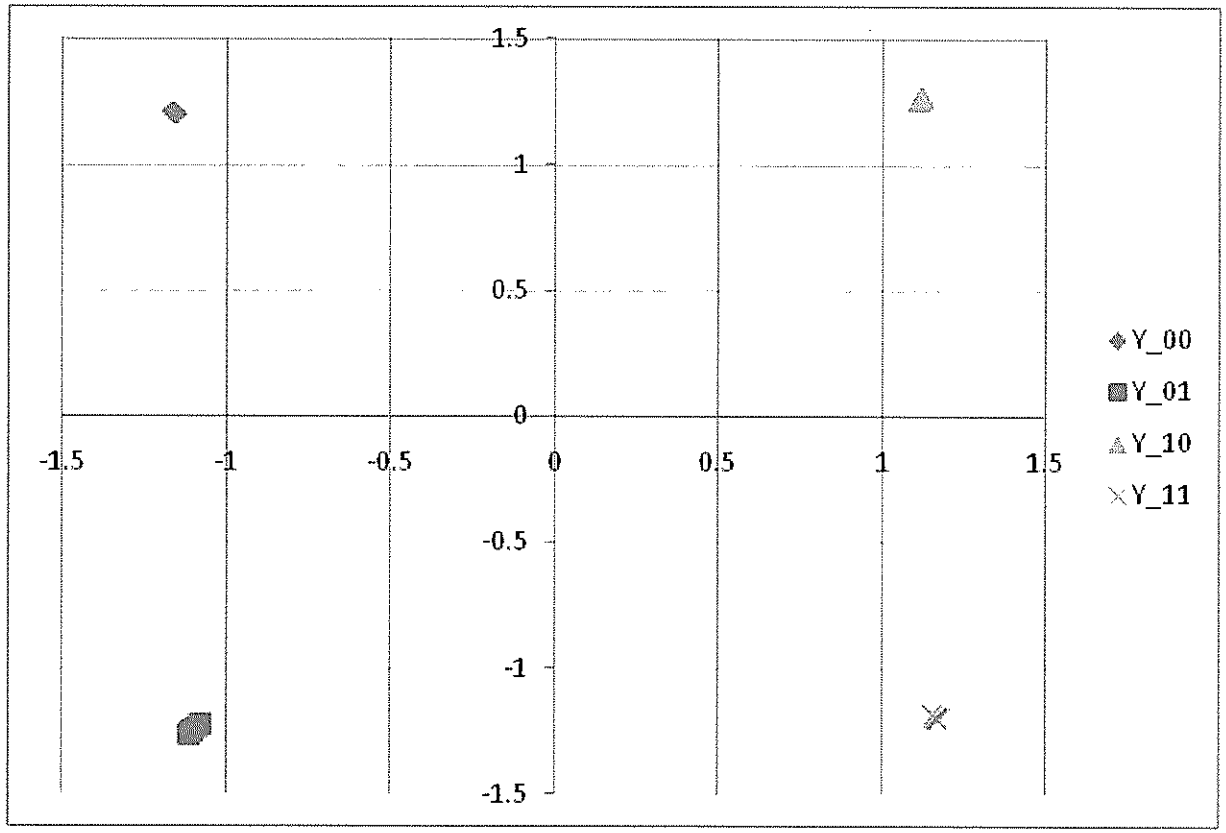



**Fig. 7**