WHAT IS CLAIMED IS:

1. An operating method for a non-volatile memory device, the method comprising:

performing a read operation on adjacent memory cells connected to an adjacent word line proximate to a target word line to determine adjacent data;

classifying target memory cells connected to the target word line into groups according to the adjacent data;

setting a read voltage level for each of the groups by searching for a read voltage level for the target memory cells in at least one of the groups; and

performing a read operation on the target memory cells using the read voltage level set for each of the groups,

wherein the setting the read voltage level for each of the groups comprises:

counting a number of memory cells of a first group, among the groups, corresponding to a number of peripheral voltage levels around a preset read voltage level; and

setting one of the peripheral voltage levels as a first read voltage level for the first group based on the counted number of memory cells.

2. The method of claim 1, wherein the classifying of the target memory cells into groups comprises:

classifying the adjacent memory cells into groups based on the adjacent data; and

classifying the target memory cells into groups corresponding to a group to which respective adjacent memory cells belong.

3. The method of claim 1, wherein the classifying of the target memory cells into groups comprises:

storing the adjacent data read from adjacent memory cells connected to at least one bit line; and

determining to which group, among the groups, a target memory cell sharing a bit line with an adjacent memory cell belongs based on the adjacent data.

4. The method of claim 1, wherein the classifying of the target memory cells into groups comprises:

classifying the target memory cells into the groups by matching a logical high state ("high") or a logical low state ("low") of adjacent data read from an adjacent memory cell with data stored in a target memory cell.

5. The method of claim 4, wherein the classifying of the target memory cells into groups comprises:

when a program state of the adjacent memory cell is high, multiplying the program state of the adjacent memory cell by the program state of the target memory cell.

6. The method of any one of the previous claims, wherein the non-volatile memory device comprises a memory cell array, and the method further comprises:

setting the read voltage level for the target word line as a read voltage level for a plurality of word lines of the memory cell array.

7. The method of any one of the previous claims, further comprising:

determining whether errors in data read from the target memory cells are correctable using an error checking and correction (ECC) operation; and

performing the read operation on the adjacent memory cells upon determining that the errors are uncorrectable.

8. A non-volatile memory device comprising:

a memory cell array including memory cells respectively connected to bit lines and word lines; and

control logic configured to

perform a read operation on the memory cells connected to a target word line among the word lines and an adjacent word line proximate to the target word line,

set a read voltage level for each one of a plurality of groups by classifying target memory cells connected to the target word line into the plurality of groups according to adjacent data read from adjacent memory cells connected to the adjacent word line,

search for a read voltage level for the target memory cells included in at least one group among the plurality of groups by counting a number of memory cells of the at least one group, among the plurality of groups, corresponding to a number of peripheral voltage levels

around a preset read voltage level and setting one of the peripheral voltage levels as the read voltage level for the at least one group based on the counted number of memory cells, and

perform the read operation directed to the target memory cells using the read voltage level set for a group to which the target memory cells belong.

9. A non-volatile memory system comprising:

a memory cell array including memory cells respectively connected to bit lines and word lines; and control logic configured to

perform a read operation directed to target memory cells connected to a target word line among the word lines,

perform a read operation directed to adjacent memory cells storing adjacent data and connected to an adjacent word line proximate the target word line,

set a read voltage level for each group among a plurality of groups by classifying target memory cells into a group among the plurality of groups based on the adjacent data,

search for a read voltage level for the target memory cells included in the group among the plurality of groups by counting a number of memory cells of the group, among the plurality of groups, corresponding to a number of peripheral voltage levels around a preset read voltage level and setting one of the peripheral voltage levels as the read voltage level for the group based on the counted number of memory cells, and

perform the read operation directed to the target memory cells using the read voltage level set for the group among the plurality of groups to which the target memory cells belong.