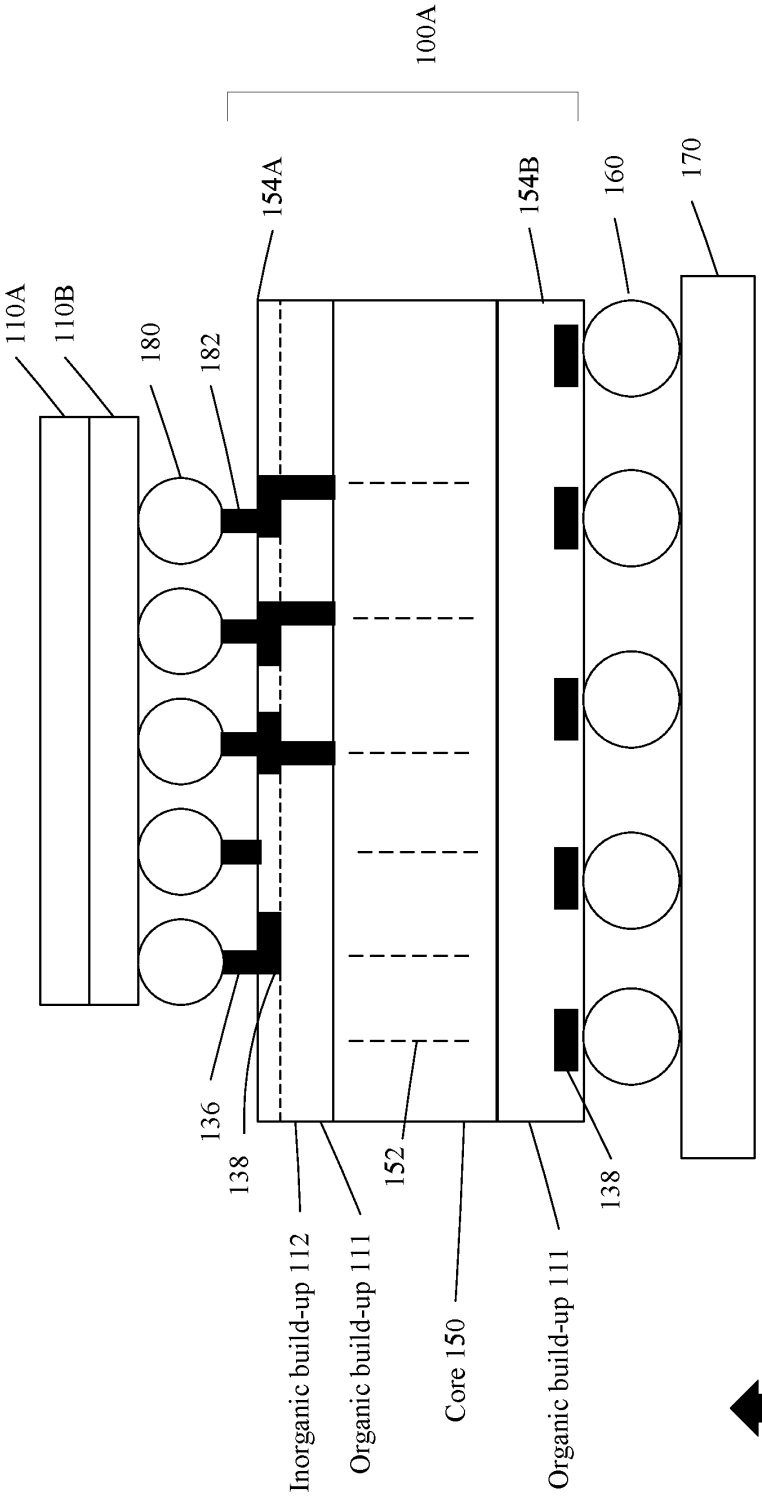

100A
110A
110B
180
182
154A
154B
160
170
136
138
Inorganic build-up 112
Organic build-up 111
152
Core 150
Organic build-up 111
138
Y
X

FIG. 1A

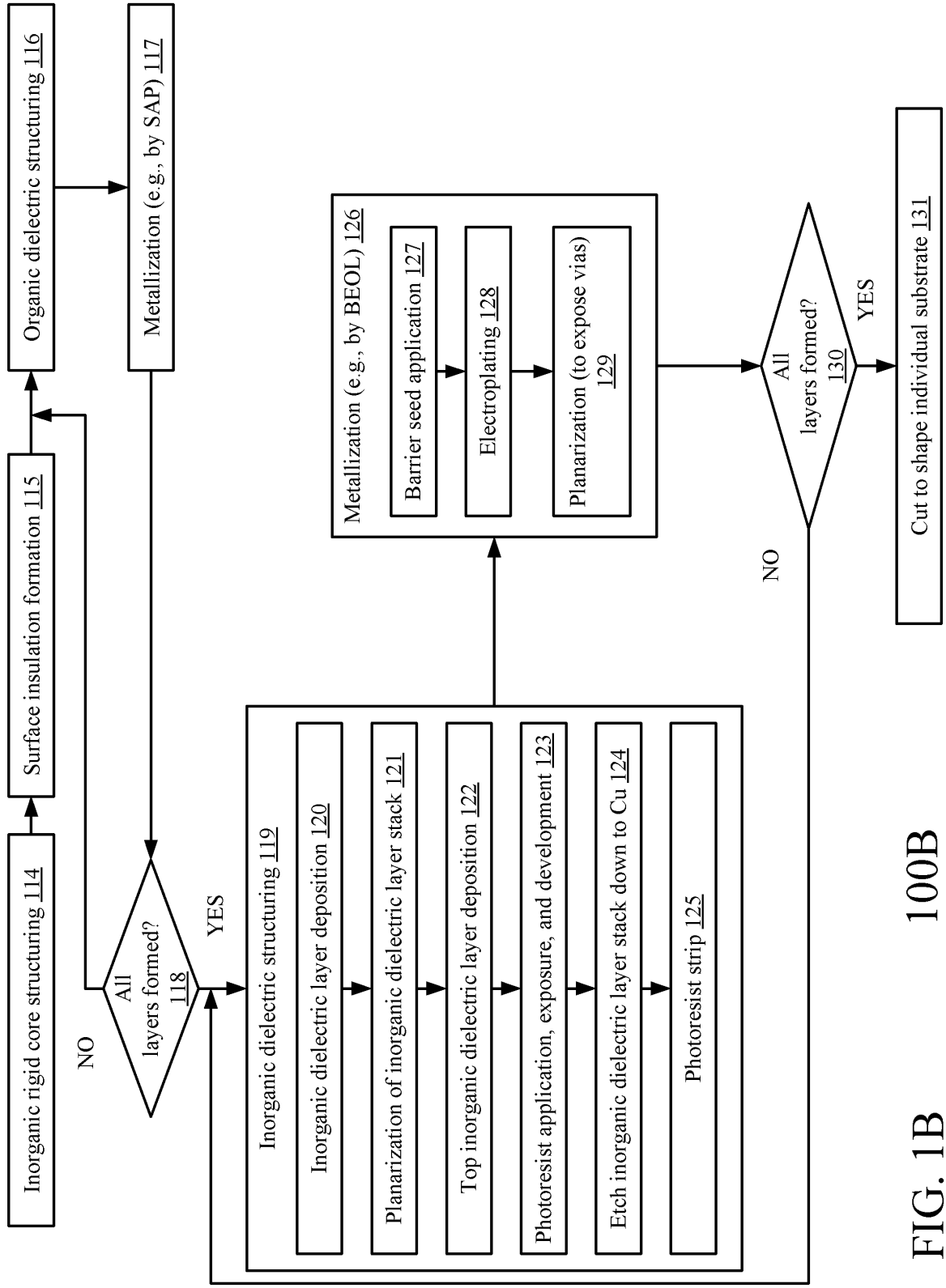

Inorganic rigid core structuring 114
Surface insulation formation 115
Organic dielectric structuring 116
Metallization (e.g., by SAP) 117
All layers formed? 118
NO
YES
Inorganic dielectric structuring 119
Inorganic dielectric layer deposition 120
Planarization of inorganic dielectric layer stack 121
Top inorganic dielectric layer deposition 122
Photoresist application, exposure, and development 123
Etch inorganic dielectric layer stack down to Cu 124
Photoresist strip 125
Metallization (e.g., by BEOL) 126
Barrier seed application 127
Electroplating 128
Planarization (to expose vias) 129
All layers formed? 130
NO
YES
Cut to shape individual substrate 131

FIG. 1B 100B

100C

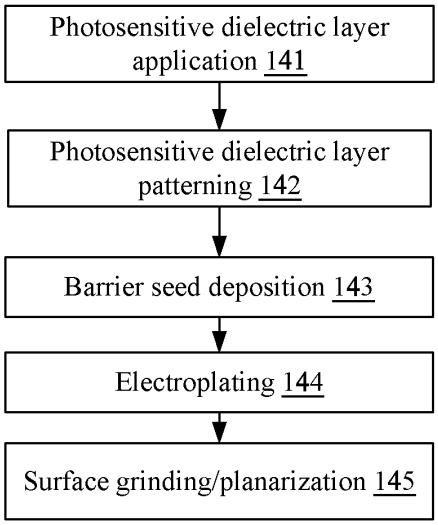


FIG. 1C

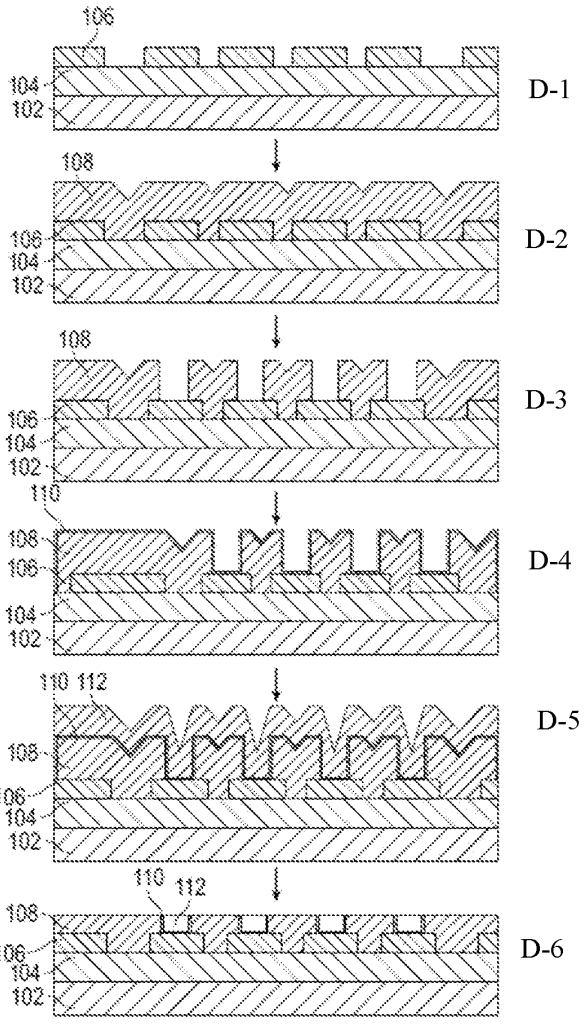


FIG. 1D

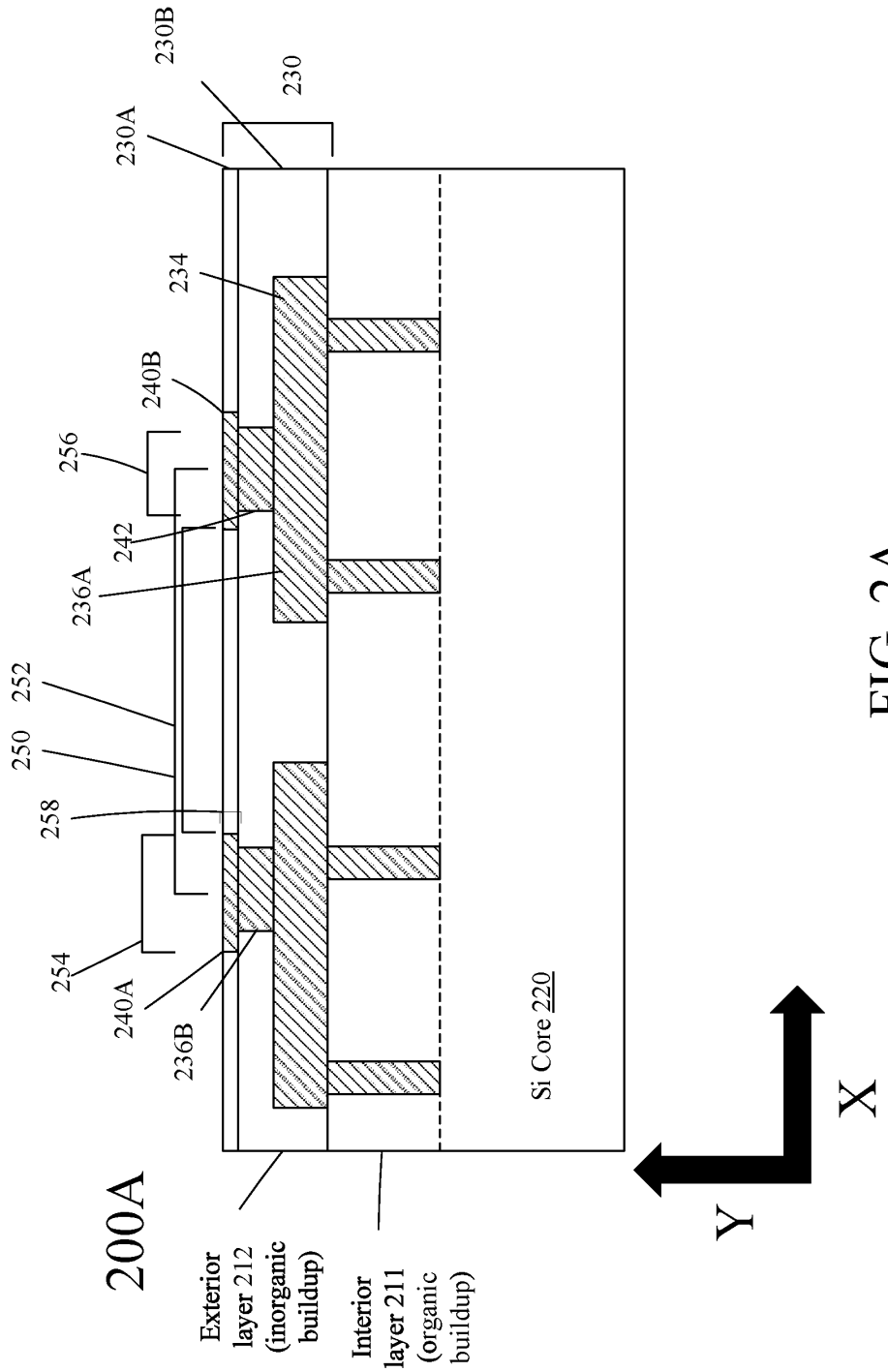

200A
Exterior layer 212 (inorganic buildup)
Interior layer 211 (organic buildup)
Si Core 220
230
230A
230B
234
240A
240B
236A
236B
242
250
252
254
256
258
Y
X

FIG. 2A

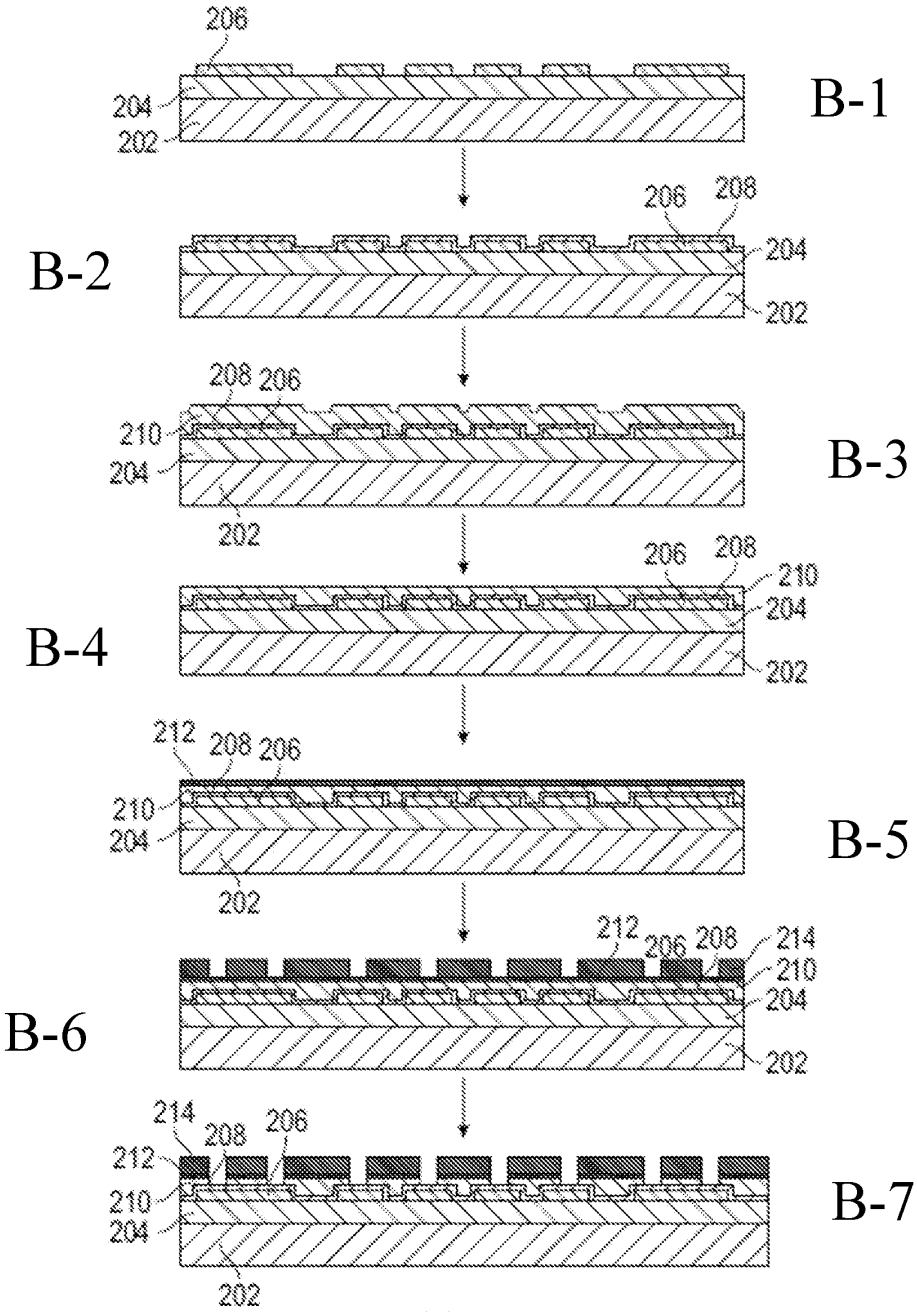

206
204
202
B-1
206
208
204
202
B-2
208
206
210
204
202
B-3
206
208
210
204
202
B-4
212
208
206
210
204
202
B-5
212
206
208
214
210
204
202
B-6
214
208
206
212
210
204
202
B-7

FIG. 2B

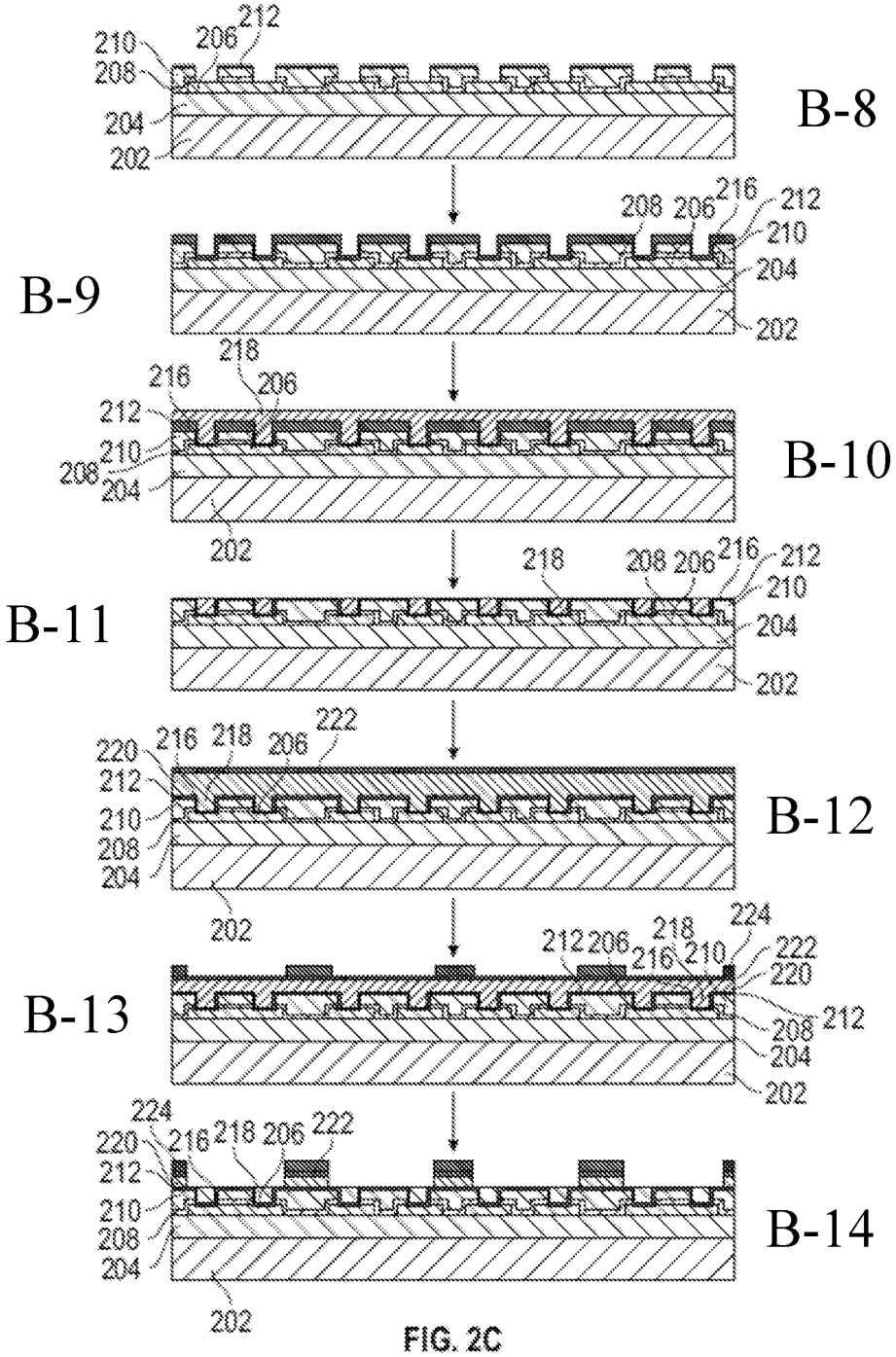


FIG. 2C

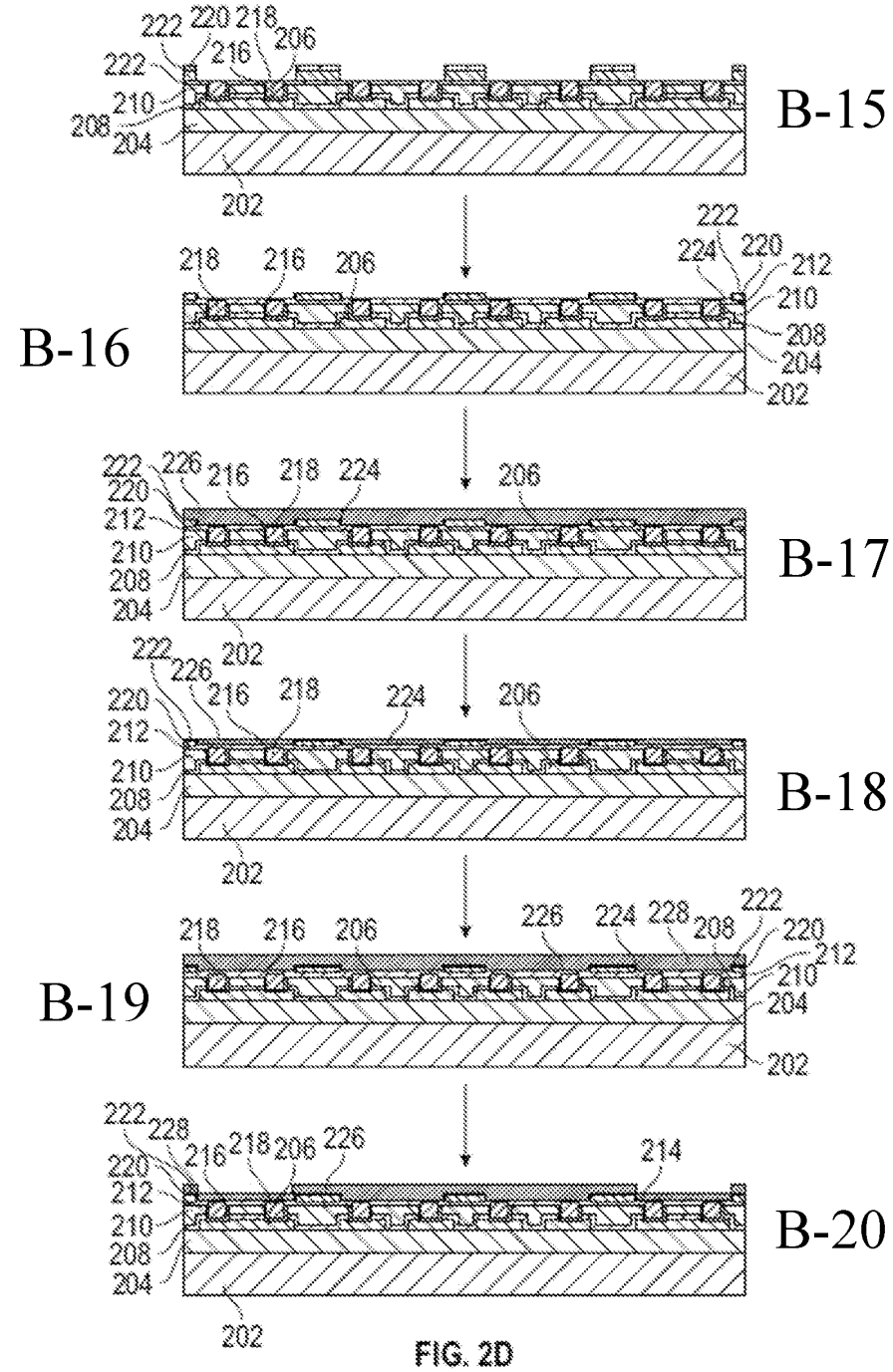


FIG. 2D

300A

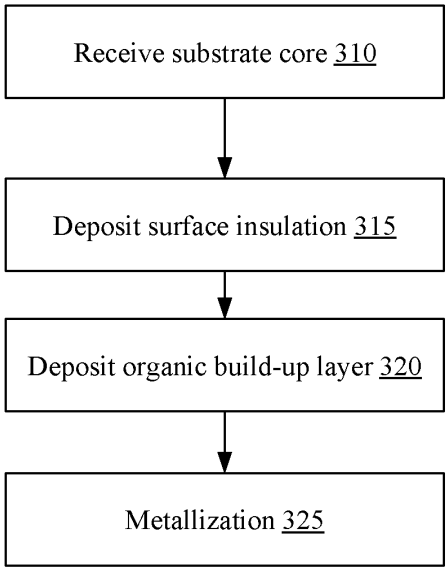


FIG. 3A

300B

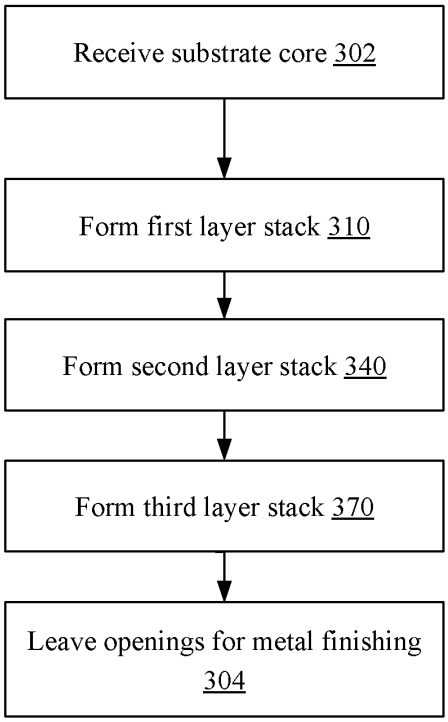


FIG. 3B

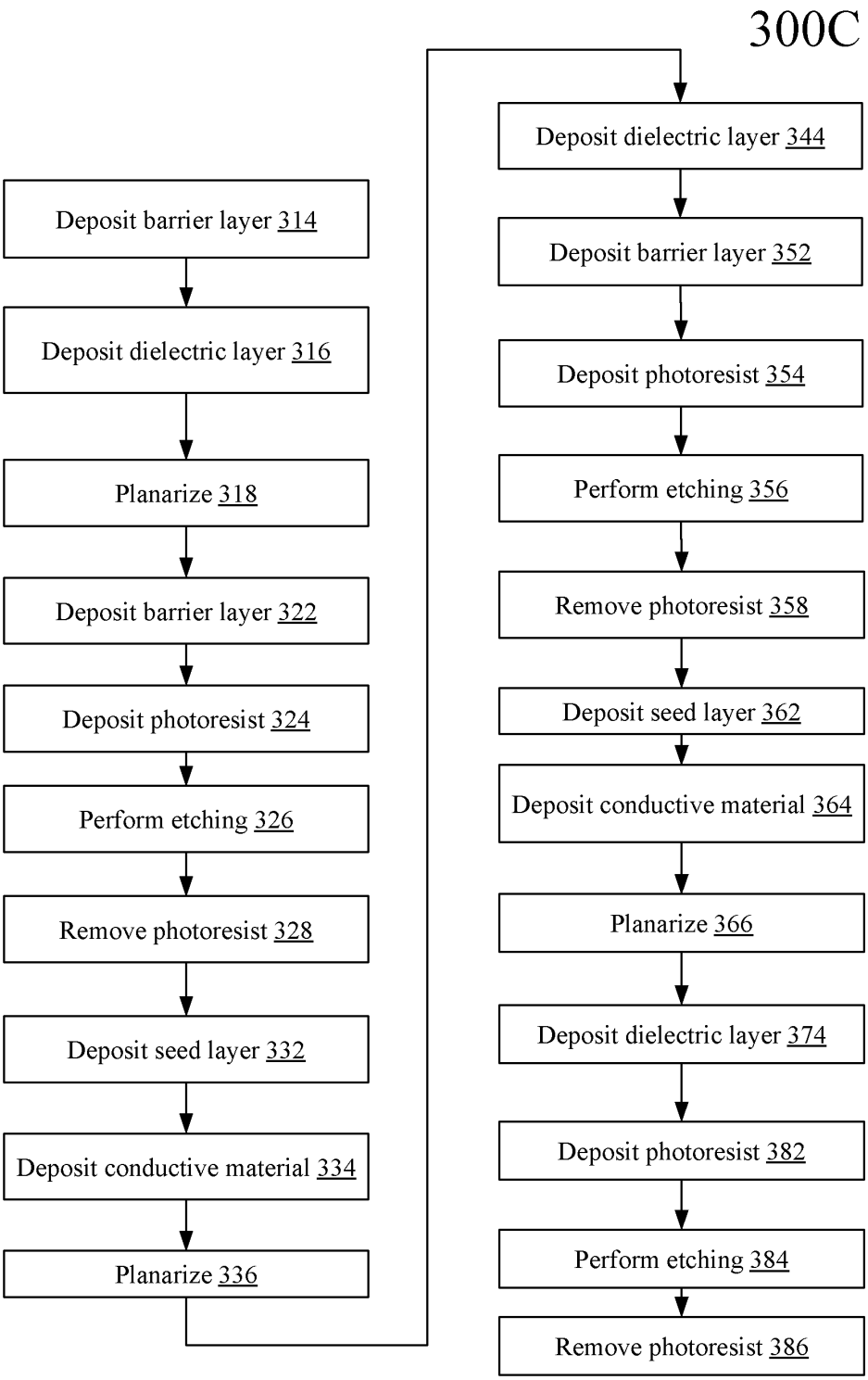

300C
Deposit barrier layer 314
Deposit dielectric layer 316
Planarize 318
Deposit barrier layer 322
Deposit photoresist 324
Perform etching 326
Remove photoresist 328
Deposit seed layer 332
Deposit conductive material 334
Planarize 336
Deposit dielectric layer 344
Deposit barrier layer 352
Deposit photoresist 354
Perform etching 356
Remove photoresist 358
Deposit seed layer 362
Deposit conductive material 364
Planarize 366
Deposit dielectric layer 374
Deposit photoresist 382
Perform etching 384
Remove photoresist 386

FIG. 3C

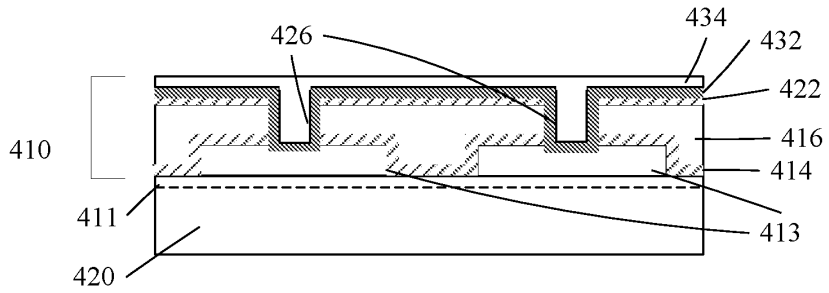


FIG. 4A

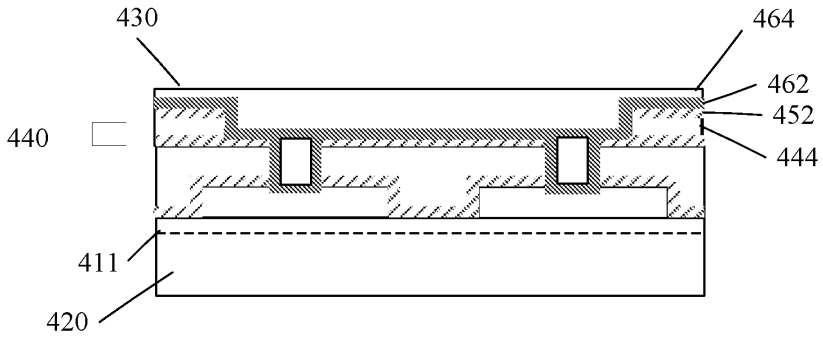


FIG. 4B

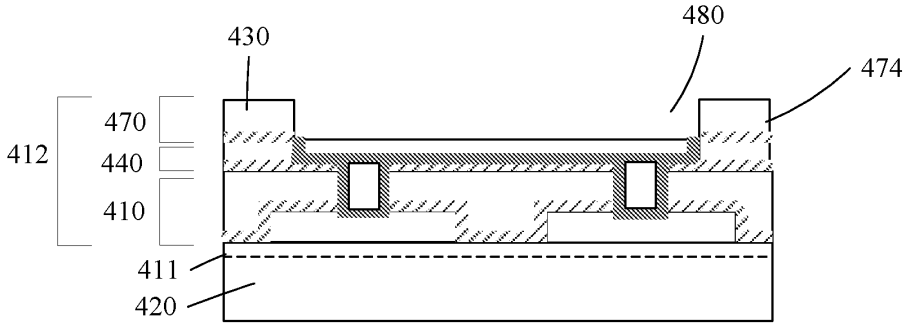


FIG. 4C

