

"RECEIVER HAVING A SEARCH TUNING CIRCUIT"

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The invention relates to a receiver having a search tuning circuit for tuning the receiver to a tuning datum selected from a group of tuning data stored in a memory circuit, which search tuning circuit, under the influence of a starting signal which depends on the field strength of a received transmitter, can start a search action when the field strength of the received transmitter becomes too weak.

A receiver of the above-mentioned type is known from Netherlands Patent Application 7,413,161. A search action of this receiver is started when the field strength of a transmitter to which the receiver has been tuned decreases to below a certain value. Particularly when such a receiver is used in a vehicle it appeared that in certain circumstances it may happen that a search action is started too frequently.

It is an object of the invention to prevent this.

According to the present invention there is provided a receiver comprising a search tuning circuit for tuning the receiver to a tuning datum selected from a group of tuning data stored in a memory circuit, which search tuning circuit in response to the influence of a starting signal which depends on the field strength of a received transmitter can start a search action when the field strength decreases to below a certain value, and a field strength behaviour-dependent starting-signal delay circuit for producing a delay in the occurrence of the starting signal with respect to the occurrence of a decrease of the field strength which delay depends on the behaviour of the field strength signal.

By providing such a delay circuit in the receiver made in accordance with the invention a search action is not immediately started at a decrease of the field strength but with a delay, which

depends on the behaviour of the field strength, such as, for example, the duration of a decrease of the field strength or the frequency with which field strength decreases occur, or both the duration and the frequency thereof. This limits the number of search actions, resulting in a more agreeable sound reproduction of a received transmitter.

The invention will now be further explained, by way of example, with reference to the accompanying drawings. In the drawings:

Figure 1 is a block schematic circuit diagram of a receiver made in accordance with the invention, and

Figure 2 is a block schematic circuit diagram showing in greater detail a circuit by means of which a signal delay which depends on the behaviour of the field strength can be obtained.

Details which are not important for an understanding of the invention have not been included in the drawing.

In Figure 1 a signal derived by an aerial is applied to an input 1 of a high-frequency and mixing section 3 of the receiver and a signal originating from an oscillator 7 is applied to an input 5 thereof. An intermediate frequency signal, which is applied to an intermediate frequency amplifier 11 is obtained from an output 9 of the high-frequency and mixing section 3.

The oscillator 7 forms part of a frequency synthesizing circuit which is tuned by applying to an input combination 13 of a frequency divider 15 a tuning datum in the form of a digital code with which the number is adjusted by which the divider 15 divides the frequency of a signal which originates from the oscillator 7 and which is applied to an input 17. A signal whose frequency is determined by the oscillator frequency and the number by which the divider 15 divides is obtained from an output 19 of the frequency divider 15. In a phase detector 21 this signal is compared with a reference signal received from a reference oscillator 23 and the frequency and the phase of these signals are made equal to one another by a control signal which is

obtained from a control signal output 25 of the phase detector 21 and is applied to a control signal input 27 of the oscillator 7. This causes the receiver to be tuned to a frequency determined by the tuning datum.

5 The tuning datum applied to the input combination 13 of the frequency divider 15 is received from an output combination 29 or 31 of a memory circuit 33, which can be connected to the input combination 13 of the frequency divider 15 via a gate circuit 35 or 37.

10 The memory circuit 33 comprises two circulating memories 39, 41, each containing a group of tuning data and which in response to a clock pulse to be applied to an input 42 can each time offer a different tuning datum to each of the output combinations 29, 31. The tuning data in a group have, for example, 15 been chosen so that they can tune the receiver to transmitters of the same character, such as, for example, transmitters transmitting the same program.

By means of the gate circuits 35, 37 it is possible to select from which circulating memories and consequently from 20 which group the tuning data are applied to the frequency divider 15. This is done by means of a switching signal coming from a switch 43 or 45 of a control device 47 when the relevant switch is closed. An OR-gate 48 then ensures that an AND-gate 49 is supplied with a signal, so that clock pulses produced by a clock 25 signal generator 51 are applied to the input 42 of the memory circuit 33 via this AND gate 49 when a reception condition signal which corresponds to logic one is applied to a third input of the AND-gate 49. This signal is produced by an AND-gate 53 having inverting inputs. A search action is started by 30 the closure of one of the switches 43 or 45, causing the tuning data from a group to tune the receiver consecutively to frequencies which correspond with those tuning data. The search action is stopped when the reception condition signal coming from the AND-gate 53 becomes logic zero.

35 There now follows a description of how the reception

condition signal at the output of the AND-gate 53 is produced. On receipt of a transmitter signal, the intermediate frequency section 11 applies an intermediate frequency signal to an amplitude detector 54 and to a frequency detector 55. The
5 amplitude detector 54 has an output 57, which applies a rectified intermediate frequency signal to an input 59 of a field strength behaviour-dependent delay circuit 61. This delay circuit 61 delays descending edges in the signal at the output 57 of the amplitude detector 54 but does not delay ascending
10 edges. The delay in the descending edges depends on the behaviour of the field strength and will be further explained hereinafter with reference to Figure 2.

A logic signal, which will be denoted by a is produced at an output 63 of the delay circuit 61. The signal a has a value
15 logic one when the received transmitter has a sufficient field strength and is located within the bandwidth of the intermediate frequency amplifier 11. When the receiver is a FM-broadcast receiver that bandwidth is large and the signal a becomes very rapidly logic one when such a transmitter is received.

20 The signal a at the output 63 of the delay circuit 61 is further applied to an input 71 of a limiter 73 via an integrating circuit formed by a resistor 67 and a capacitor 69. At an output 75 this limiter 73 supplies a logic signal which will be denoted b and which is applied to an inverting input of an AND-gate 77.
25 This signal b is, in its totality, delayed with respect to the signal a.

The AND-gate 77 now produces a signal ab' which, because of the inversion at the input of the AND-gate 53 renders this
30 AND-gate 53 non-conductive for a short period of time immediately after each occurrence of a positive edge in the a-signal which causes the AND-gate 49 to be rendered non-conductive and a search action of the receiver to be stopped during that short period of time.

35 The frequency detector 55 has two outputs 81, 83 at which signals appear from which unwanted alternating current components

have been removed. Compared with a reference level, these signals are of the opposite polarity and have the known S-shape as a function of the frequency. Via two diodes 85, 87 these signals are applied to a limiter 91, which produces at an output 93 a logic signal which will be denoted by c and which is logic one outside the pass region of the intermediate frequency amplifier 11 and in a very small frequency range around the intermediate frequency. This signal c and also the signal a are applied to an AND-gate 94.

The AND-gate 94 produces a logic signal ac which is applied to a further inverting input of the AND-gate 53 and to a switch 95 in a low frequency signal path of the receiver, which leads from an output 96 of the frequency detector 55 to a reproduction device 97.

The logic signal ac produced by the AND-gate 94 becomes logic one when a transmitter which is received during the search action which was temporarily stopped by the signal ab', has the proper frequency and it forms a definite stop signal as then the AND-gate 53 and, consequently, the AND-gate 49 remain non-conductive. The sound channel is then through-connected by the switch 95. When the received transmitter does not have the proper frequency then the signal ac remains logic zero and the search action is immediately restarted after the signal ab' has become logic zero.

The AND-gate 53 produces a logic signal $(\underline{ac})' \cdot (\underline{ab}')' = \underline{a}' + \underline{bc}'$, which is the reception condition signal which causes a search tuning action to be stopped at a received transmitter of a sufficient field strength and a proper frequency as described in the foregoing. So this is initiated by the undelayed, positively going edge of the a signal.

Restarting a search action when the field strength decreases to below a certain value is caused by a negatively going edge of the a signal, which passes from logic one to logic zero. The output signal $\underline{a}' + \underline{bc}'$ of the AND-gate 53 then becomes one and, as one of the switches 43, 45 is still closed, clock pulses which cause a search action to be performed are passed via the AND gate

49. As mentioned in the foregoing, the descending edges in the a signal are delayed with respect to the instants at which the field strength of the received transmitter decreases to below a certain value. This can be realised by means of the circuit 61, which will be described hereinafter.

It will be clear that the receiver, if so desired, may further also be suitable for tuning to tuning data other than those obtained from the memory circuit 33. This is indicated in the Figure by means of broken lines.

Although the receiver of the embodiment has been provided with a frequency synthesizing circuit having a variable divider, a different type of frequency synthesizing circuit may of course alternatively be used.

Several functions in the receiver which can be carried out simultaneously in the given example may of course also be carried out sequentially, for example when the receiver includes a microprocessor.

Although the described search tuning circuit is particularly suitable for FM radio-broadcast receivers and in particular for vehicle receivers, the field of application need not be limited thereto; also in aircraft receivers, for example, an improvement may be obtained with this search tuning circuit.

It will further be obvious that several other combinations of gates, detection circuits and limiters are possible to perform the functions desired. The reception condition signal or the composite portions thereof may, for example, alternatively be combined with the other signals which are applied to the AND-gate 49 and to the OR-gate 48.

Any type of detector which can determine a frequency datum accurately without bandwidth limiting means may be used as the frequency detector.

If so desired, the memory circuit of the receiver may contain one or more groups of tuning data.

For the use of the field strength behaviour-depending delay in the starting signal, the described temporary stopping action

and restarting on receipt of a transmitter having an unwanted frequency are not a requirement and may be omitted, in which case only an inverse of the signal a may, if so desired, be used as the reception condition signal.

5 It is further possible to process the descending and ascending edges in the a signal in separate circuits and to apply them as individual starting and stopping signals to a start-stop memory which can produce the reception condition signal.

10 In Figure 2 corresponding elements have been given the same reference numerals as in Figure 1. The field strength-dependent signal, which is converted by a limiter 101 into a logic signal p which is logic one at a sufficient field strength for a good reception and logic zero when the field strength is insufficient, is applied to the input 59 of the delay circuit 61.

15 Via an inverter 102 the logic signal p is applied to a command input 103 of a first counter 105 and directly to a setting input 107 of a flipflop 109 and to a resetting input 113 of the first counter 105. Clock pulses produced by a clock signal generator 117 are applied to an input 115 of the first counter 105, which has four outputs 119, 121, 123, 125.

20 When the logic signal p is one, the first counter 105 is kept in the reset condition via the input 113 and the inverted p signal blocks a counting operation at the command input 103. Each one of the outputs 119, 121, 123, 125 is then zero. These outputs are connected to an input of AND-gates 127, 129, 131 and 133, respectively, the outputs of which are connected to inputs of an OR-gate 135 whose output is connected to a reset input 137 of the flip-flop 109. So this reset input 137 is also zero and from an output 139 of the flip-flop 109 a signal is obtained which is one and is applied to the output 63 from which the signal a which is then consequently logic one, is obtained. Another output 140 of the flip-flop 109 is then zero.

35 When the signal p becomes zero as the result of a decrease in field strength, the first counter 105 starts counting as it is

no longer blocked by the signal at the input 103, which is now one, and as the reset signal at the input 113 has become zero. When the signal p has been zero for a sufficiently long period of time, the outputs 119, 121, 123, 125 of the first counter 105 become one one after the other after a period of time τ , 4τ , 16τ , 64τ , respectively in which τ may be selected to be a value between substantially 100 msec and 400 msec, typically 200 msec, which may correspond to, for example, four clock pulses.

The AND-gates 127, 129, 131, 133 are operated by a second counter 141, which may assume a position minus one, zero, one or two. In the position minus one outputs 143 and 145 of this counter are logic one, while an output 147 is logic zero. When this counter is in the zero position the outputs 143, 145, 147 are logic zero; in the one position the output 145 is one and the outputs 143 and 147 are zero and in the two position the outputs 145 and 147 are one and the output 143 is zero.

The output 143 of the second counter 141 is connected to a further input of the AND-gate 127 and to inverting inputs of the AND-gates 129, 131 and 133. The outputs 145 and 147 of the second counter 141 are connected to a first and a second input, respectively, of an AND-gate 149 the output of which is connected to a further input of the AND-gate 133, to a first input and to a second inverting input of an AND-gate 151 the output of which is connected to a further input of the AND-gate 131, and to an inverting first input and an inverting second input of an AND-gate 153 the output of which is connected to a further input of the AND-gate 129.

As a result thereof the output of the AND-gate 127 becomes one when the position of the second counter 141 is minus one and the output 119 of the first counter 105 is one. The output of the AND-gate 129 becomes one when the position of the second counter 141 is zero and the output 121 of the first counter 105 is one. The output of the AND-gate 131 becomes one when the position of the second counter 141 is one and the output 123 of the first counter is one, and the output of the AND-gate 133 becomes one when the position of the second counter 141 is two and the output 125 of the

first counter 105 is one. This is the case a period of time τ and 4τ , 16τ , 64τ , respectively, after the p -signal has become zero.

As a result thereof the output of the OR-gate 135 becomes one a period of time τ , 4τ , 16τ , or 64τ , respectively, depending on the position of the second counter 141, after the p -signal has become zero. The input 107 of the flip-flop 109 had already become zero because of the fact that the p -signal has become zero, so that the output 139 of the flip-flop 109 becomes zero a period of time τ , 4τ , 16τ or 64τ after the p -signal has become zero. So the start of a search action is delayed for a period of time which depends on the position of the second counter 141.

When now the signal p becomes one again, the first counter 105 is stopped via its input 103 and reset to zero via its input 113, so that the input 137 of the flip-flop 109 becomes zero and the input 107 becomes one. The output 139 immediately becomes zero when the p -signal becomes one and the search action can be stopped without any delay.

When the p -signal remains zero for a period of time shorter than $X\tau$, in which X is determined by the position of the second counter 141, then the a -signal at the output 139 of the flip-flop 109 remains one and the search action is not started.

Now the influence of the behaviour of the p -signal and, consequently, that of the field strength of a received transmitter on the position of the second counter 141, which, as described hereinbefore, determines the delay in a start of a search action, will be considered.

The second counter 141 has an up-counting input 157, which is connected to an output of an AND-gate 159 an input of which is connected to the output 140 of the flip-flop 109, and a down-counting input 161, which is connected to an output of an AND-gate 163. The output of the AND-gate 159 cannot become logic one and the counting position can therefore not further increase when an inverting input of the AND-gate 159, which is connected to the output of the AND-gate 149, is logic one, that is to say when

the highest counting position, two in this case, has been reached. The output of the AND-gate 161 cannot become logic one when the lowest counting position, which in this case is minus one and which causes the output 143 of the counter 141 to be logic one, has been reached, so that the counting position cannot further decrease.

The fact whether the second counter 141 counts upwards or downwards is further determined by a signal coming from an output 165 of a time switch 167 and input 169 of which is connected to the output 139 of the flip-flop 109 via a capacitor 171 and, via a capacitor 173 and a delay circuit 175, to a switch 176 whose other side is connected to a positive voltage source. The input 169 is further connected to ground via a resistor 174. The switch 176 is an on/off switch for the supply voltage of the receiver. The output 165 of the time switch 167 is connected directly to an input of the AND-gate 159 and via an inverter 177 to an input of the AND-gate 163.

The time switch 167 keeps its output 165 in the logic one state for a period of time which may be between one and four minutes, typically two minutes, after a positive edge has occurred at its input 169, so after the a-signal has last become one and the p-signal consequently showed a field strength decrease of a duration longer than $X\tau$.

The second counter 141 is reset to zero by a signal at a reset input 179 thereof. This signal occurs when a positive voltage is applied briefly to the reset input 179 of the second counter 141 via the switch 176, which is closed as soon as the receiver is switched on, via the delay circuit 175 and via a differentiating network having a capacitor 183 and a resistor 185.

Each time the signal at the output 140 of the flip-flop 109 changes from zero to one within two minutes after the time switch 167 started in response to a previous search action, that it to say each new search action carried out within that period of time after a previous search action, so every time the field strength within those two minutes was insufficient for a period of time longer than

24
X_T, causes the position of the counter 141 to increase by one and the delay in starting a search action may consequently increase. So the delay in starting a search action depends on the duration of the decrease in field strength and on the frequency with which the decreases in the field strength occur.

When no new decrease causing a search action occurs within two minutes after a decrease of the field strength which caused a previous search action, then the output 165 of the time switch 167 becomes logic zero and the AND-gate 163, which controls the count-down action may become operative via the inverter 177.

Via a differentiating network comprising a capacitor 186 and a resistor 187, a signal coming from an inverter 188, which makes a negative pulse from a positive output pulse of a monostable multivibrator 189, is applied to a further input of the AND-gate 163. The monostable multivibrator 189 is started by a descending edge of an output signal of a second time switch 191. The time switch 191 receives an output signal from an OR-gate 193 an input of which is connected to the output of the inverter 177 via a differentiating network having a capacitor 195 and a resistor 197, another input of this OR-gate 193 being connected to an output of an AND-gate 199 an input of which is connected to the output of the inverter 177 and a further input to the output of the differentiating network connected to the inverter 188.

The second time switch 191 is started by a positive edge at the output of the differentiating network 195, 197. This positive edge is produced when the signal from the output of the inverter 177 becomes positive. Via the OR-gate 193 this edge is applied to the second time switch 191 the output of which then remains logic one for one to ten minutes, typically three minutes, and which thereafter, when the output becomes logic zero, starts the monostable multivibrator 189 which produces a positive pulse which is converted by means of the inverter 188 into a negative pulse the positive trailing edge of which reduces the position of the second counter 141 by one and restarts the second time switch 191 via the AND-gate 199 and the OR-gate 193, so that this

second time switch applies after every three minutes a pulse to the count-down input 161 of the second counter 141 for the time no interruption occurs in the field strength and the first time switch 167 consequently produces an output signal zero which keeps the relevant inputs of the AND-gates 163 and 199 logic one via the inverter 177. As a result of this the position of the second counter 141 may decrease to its lowest position but one, causing the AND-gate 163 to be rendered non-conductive again by the signal received from the output 143 of the second counter 141.

When a field strength behaviour-dependent delay circuit as described above is used in a car radio the search properties thereof automatically adapt themselves in an advantageous manner to the speed of the car. Namely, it appears that the decreases in field strength have a duration which are substantially inversely proportional to that speed. At a high speed the circuit adjusts itself automatically to a shorter starting-delay time than when the car travels at a low speed.

In the described embodiment only those decreases of the field strength which result in a search action, that is decreases in the field strength which have a duration longer than an adjusted start-delay time $X\tau$, influence that start-delay time. This start-delay time is increased when the field strength decreases more than once every two minutes and is reduced when the field strength does not decrease more than approximately once every five, eight and eleven minutes, respectively. It will be obvious that although an advantageous version for a car radio is obtained by taking the duration as well as the frequency of field strength decreases into consideration in the above described manner, each of these two criteria may alternatively be used individually to adapt the search properties of a receiver to the circumstances in which it is used. Alternatively, if so desired, that adaptation may be obtained with a combination of the rate of occurrence and the duration of the field strength decreases measured independently from one another.

(76)

Although the above-described circuit for recognizing the behaviour of the field strength signal utilizes the same elements as for delaying the starting signal, this is not an absolute requirement and these two actions may, if so desired, be carried out in separate circuits.



CLAIMS:

1. A receiver comprising a search tuning circuit for tuning the receiver to a tuning datum selected from a group of tuning data stored in a memory circuit, which search tuning circuit in response to the influence of a starting signal which depends on the field strength of a received transmitter can start a search action when the field strength decreases to below a certain value, and a field strength behaviour-dependent starting-signal delay circuit for producing a delay in the occurrence of the starting signal with respect to the occurrence of a decrease of the field strength which delay depends on the behaviour of the field strength signal.
2. A receiver as claimed in Claim 1, wherein the field strength behaviour-depending starting-signal delay circuit is a starting-signal delay circuit which depends on the duration of the decrease in the field strength.
3. A receiver as claimed in Claim 1, wherein the field strength behaviour-dependent starting-signal delay circuit is a starting-signal delay circuit which depends on the frequency of occurrence of the decreases of the field strength.
4. A receiver as claimed in Claim 1, wherein the field strength behaviour-dependent starting-signal delay circuit is a starting-signal delay circuit which depends on the duration and the rate of occurrence of decreases in the field strength.
5. A receiver as claimed in Claim 4, wherein the starting-signal delay depends on the frequency of occurrence of decreases in the field strength which are of a longer duration than the starting-signal delay.
6. A receiver as claimed in Claim 1 or 5, wherein the delay in the starting signal is substantially 200 msec. or a multiple thereof.



7. A receiver as claimed in Claim 5 or Claim 6, wherein the delay in the starting signal is increased when the field strength decreases more than substantially once per two minutes.

8. A receiver as claimed in Claim 1, 5, 6 or 7, wherein the delay of the starting signal is reduced when the field strength decreases less than substantially once per five minutes.

9. A receiver as claimed in Claim 8, wherein the delay of the starting signal is reduced once again when the field strength decreases less than substantially once per eight minutes.

10. A receiver as claimed in any one of the Claims 6 to 9, further comprising a circuit which on switch-on of the receiver adjusts the delay of the starting signal to a value of substantially four times a minimum delay value.

11. A receiver as claimed in Claim 10, wherein the starting signal delay is adjustable to one of four values which comprise the minimum delay value and four, sixteen or sixty-four times, respectively, that minimum delay value.

12. A receiver having a search tuning circuit, substantially as hereinbefore described with reference to the accompanying drawings.

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29

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