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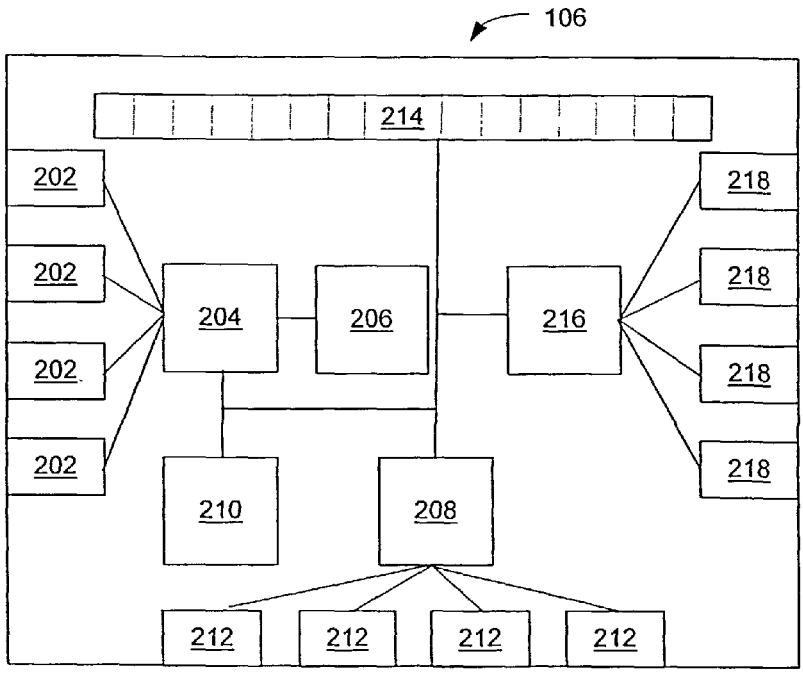
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(54) Title: SCHEDULER FOR A DATA MEMORY ACCESS HAVING MULTIPLE CHANNELS



(57) Abstract: A scheduler configured to schedule multiple channels of a Data Memory Access (DMA) includes a shift structure having entries corresponding to the multiple channels to be scheduled. Each entry in the shift structure includes multiple fields. Each entry also includes a weight that is determined based on these multiple fields. The scheduler also includes a comparison-logic circuit that is configured to then sort the entries based on their respective weights.

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