CLAIMS

What is claimed is:

1. A logic circuit comprising:

a first ferromagnetic element having a first ferromagnetic layer;

a second ferromagnetic element having a second ferromagnetic layer; and

a first transistor coupled to the first ferromagnetic element, wherein the first transistor is configured to allow a first current to flow through the first ferromagnetic element, the first current influencing a magnetization direction of the first ferromagnetic layer, the magnetization direction of the first ferromagnetic layer influencing a magnetization direction of the second ferromagnetic layer.

2. The logic circuit of claim 1, further comprising a second transistor coupled to the second ferromagnetic element, wherein the second transistor is configured to allow a second current to flow through the second ferromagnetic element.

3. The logic circuit of claim 2, wherein a magnitude of the second current is influenced by the magnetization direction of the second ferromagnetic layer.

4. The logic circuit of claim 1, wherein:

the first ferromagnetic element comprises:

a first pinned layer having a first fixed magnetization direction; and

a first insulating layer disposed between the first pinned layer and the first ferromagnetic layer; and

the second ferromagnetic element comprises:

a second pinned layer having a second fixed magnetization direction; and

a second insulating layer disposed between the second pinned layer and the second ferromagnetic layer.

5. The logic circuit of claim 4, wherein:

the first fixed magnetization direction is aligned with a longitudinal axis of the first ferromagnetic element;

the second fixed magnetization direction is aligned with a longitudinal axis of the second ferromagnetic element; and

the longitudinal axis of the first ferromagnetic element and the longitudinal axis of the second ferromagnetic element are substantially parallel.

6. The logic circuit of claim 5, wherein when a direction of the first current results in the first current flowing from the first ferromagnetic layer to the first pinned layer:

the magnetization direction of the first ferromagnetic layer is opposite the first fixed magnetization direction; and

the magnetization direction of the second ferromagnetic layer is equal to the second fixed magnetization direction in response to the magnetization direction of the first ferromagnetic layer being opposite the first fixed magnetization direction.

7. The logic circuit of claim 5, wherein when a direction of the first current results in the first current flowing to the first ferromagnetic layer from the first pinned layer:

the magnetization direction of the first ferromagnetic layer is equal to the first fixed magnetization direction; and

the magnetization direction of the second ferromagnetic layer is opposite the second fixed magnetization direction in response to the magnetization direction of the first ferromagnetic layer being equal to the first fixed magnetization direction.

8. The logic circuit of claim 4, wherein:

the magnetization direction of the first ferromagnetic layer is opposite the first fixed magnetization direction in response to the first current flowing from the first ferromagnetic layer to the first pinned layer; and

the magnetization direction of the first ferromagnetic layer is equal to the first fixed magnetization direction in response to the first current flowing to the first ferromagnetic layer from the first pinned layer.

9. The logic circuit of claim 8, further comprising a second transistor coupled to the second ferromagnetic element, the second transistor being configured to allow a second current to flow through the second ferromagnetic element, wherein a magnitude of the second current is influenced by the magnetization direction of the second ferromagnetic layer.

10. The logic circuit of claim 1, further comprising

a third ferromagnetic element having a third ferromagnetic layer; and

a second transistor coupled to the third ferromagnetic element, wherein:

the second transistor is configured to allow a second current to flow through the third ferromagnetic element, the second current influencing a magnetization direction of the third ferromagnetic layer; and

the magnetization direction of the second ferromagnetic layer is influenced by the magnetization direction of the first ferromagnetic layer and the third ferromagnetic layer.

11. The logic circuit of claim 10, further comprising:

a fourth ferromagnetic element having a fourth ferromagnetic layer; and

a third transistor coupled to the fourth ferromagnetic element, wherein:

the first current is indicative of a first digital input value;

the second current is indicative of a second digital input value;

the third transistor is configured to allow a third current to flow through the fourth ferromagnetic element, the third current being indicative of a third digital input value and influencing a magnetization direction of the fourth ferromagnetic layer; and

the magnetization direction of the second ferromagnetic layer is indicative of a majority of the first digital input value, the second digital input value, and the third digital input value.

12. The logic circuit of claim 1, further comprising a sensing arrangement configured to identify a digital output value based on the magnetization direction of the second ferromagnetic layer.

13. A method for operating a logic circuit including an input ferromagnetic element and an output ferromagnetic element having a magnetization direction influenced by a magnetization direction of the input ferromagnetic element, the method comprising:

activating an input transistor coupled to the input ferromagnetic element to allow an input current to flow through the input ferromagnetic element, the input current influencing the magnetization direction of the input ferromagnetic element;

activating an output transistor coupled to the output ferromagnetic element to allow an output current to flow through the output ferromagnetic element, wherein a magnitude of the output current is influenced by the magnetization direction of the output ferromagnetic element; and

determining the magnetization direction of the output ferromagnetic element in response to the output current; and

determining a digital output value for the logic circuit based on the magnetization direction of the output ferromagnetic element.

14. The method of claim 13, further comprising operating an input current arrangement coupled to the input transistor to provide the input current in a direction corresponding to a digital input value.

15. The method of claim 14, the input ferromagnetic element including a first pinned layer and a first free layer and the output ferromagnetic element including a second pinned layer and a second free layer, a magnetization direction of the second free layer being influenced by a magnetization direction of the first free layer, wherein operating the input current arrangement comprises:

operating the input current arrangement to provide the input current flowing from the first free layer to the first pinned layer in response to the digital input value corresponding to a first digital value, the input current flowing from the first free layer to the first pinned layer resulting in the magnetization direction of the first free layer being opposite a magnetization direction of the first pinned layer; and

operating the input current arrangement to provide the input current flowing to the first free layer from the first pinned layer in response to the digital input value corresponding to a second digital value, the input current flowing to the first free layer from the first pinned layer resulting in the magnetization direction of the first free layer being equal to a magnetization direction of the first pinned layer.

16. The method of claim 13, wherein determining the magnetization direction comprises:

obtaining a voltage across the output ferromagnetic element in response to the output current; and

determining the magnetization direction based on the voltage across the output ferromagnetic element.

17. The method of claim 16, wherein determining the magnetization direction based on the voltage across the output ferromagnetic element comprises:

identifying a first digital value as the digital output value when the voltage across the output ferromagnetic element is greater than a threshold voltage; and

identifying a second digital value as the digital output value when the voltage across the output ferromagnetic element is less than the threshold voltage.

18. A method for fabricating a logic circuit, the method comprising:

forming a first ferromagnetic element having a first ferromagnetic layer;

forming a second ferromagnetic element having a second ferromagnetic layer, wherein the second ferromagnetic element is arranged with respect to the first ferromagnetic element such that a magnetization direction of the first ferromagnetic layer influences a magnetization direction of the second ferromagnetic layer;

forming a first transistor coupled to the first ferromagnetic element, wherein the first transistor is configured to allow a first current to flow through the first ferromagnetic element, the first current influencing the magnetization direction of the first ferromagnetic layer; and

forming a second transistor coupled to the second ferromagnetic element, wherein the second transistor is configured to allow a second current to flow through the second ferromagnetic element.

19. The method of claim 18, wherein forming the first ferromagnetic element comprises forming the first ferromagnetic element overlying the first transistor.

20. The method of claim 19, further comprising:

forming a layer of dielectric material overlying the first transistor; and

forming a via in the layer of dielectric material, the via overlying a terminal region of the first transistor, wherein forming the first ferromagnetic element comprises:

forming a third ferromagnetic layer overlying the layer of dielectric material, the third ferromagnetic layer being electrically connected to the via;

forming an insulating layer overlying the third ferromagnetic layer; and

forming the first ferromagnetic layer overlying the insulating layer, wherein the first current flows between the third ferromagnetic layer and the first ferromagnetic layer.

What is claimed is:

1. A logic circuit comprising: a first ferromagnetic element having a first ferromagnetic layer; a second ferromagnetic element having a second ferromagnetic layer; and a first transistor coupled to the first ferromagnetic element, wherein the first transistor is configured to allow a first current to flow through the first ferromagnetic element, the first current influencing a magnetization direction of the first ferromagnetic layer, the magnetization direction of the first ferromagnetic layer influencing a magnetization direction of the second ferromagnetic layer.

2. The logic circuit of claim 1, further comprising a second transistor coupled to the second ferromagnetic element, wherein the second transistor is configured to allow a second current to flow through the second ferromagnetic element.

3. The logic circuit of claim 2, wherein a magnitude of the second current is influenced by the magnetization direction of the second ferromagnetic layer.

4. The logic circuit of claim 1, wherein: the first ferromagnetic element comprises: a first pinned layer having a first fixed magnetization direction; and a first insulating layer disposed between the first pinned layer and the first ferromagnetic layer; and the second ferromagnetic element comprises: a second pinned layer having a second fixed magnetization direction; and a second insulating layer disposed between the second pinned layer and the second ferromagnetic layer.

5. The logic circuit of claim 4, wherein: the first fixed magnetization direction is aligned with a longitudinal axis of the first ferromagnetic element; the second fixed magnetization direction is aligned with a longitudinal axis of the second ferromagnetic element; and the longitudinal axis of the first ferromagnetic element and the longitudinal axis of the second ferromagnetic element are substantially parallel.

6. The logic circuit of claim 5, wherein when a direction of the first current results in the first current flowing from the first ferromagnetic layer to the first pinned layer: the magnetization direction of the first ferromagnetic layer is opposite the first fixed magnetization direction; and the magnetization direction of the second ferromagnetic layer is equal to the second fixed magnetization direction in response to the magnetization direction of the first ferromagnetic layer being opposite the first fixed magnetization direction.

7. The logic circuit of claim 5, wherein when a direction of the first current results in the first current flowing to the first ferromagnetic layer from the first pinned layer: the magnetization direction of the first ferromagnetic layer is equal to the first fixed magnetization direction; and the magnetization direction of the second ferromagnetic layer is opposite the second fixed magnetization direction in response to the magnetization direction of the first ferromagnetic layer being equal to the first fixed magnetization direction.

8. The logic circuit of claim 4, wherein: the magnetization direction of the first ferromagnetic layer is opposite the first fixed magnetization direction in response to the first current flowing from the first ferromagnetic layer to the first pinned layer; and the magnetization direction of the first ferromagnetic layer is equal to the first fixed magnetization direction in response to the first current flowing to the first ferromagnetic layer from the first pinned layer.

9. The logic circuit of claim 8, further comprising a second transistor coupled to the second ferromagnetic element, the second transistor being configured to allow a second current to flow through the second ferromagnetic element, wherein a magnitude of the second current is influenced by the magnetization direction of the second ferromagnetic layer.

10. The logic circuit of claim 1, further comprising a third ferromagnetic element having a third ferromagnetic layer; and a second transistor coupled to the third ferromagnetic element, wherein: the second transistor is configured to allow a second current to flow through the third ferromagnetic element, the second current influencing a magnetization direction of the third ferromagnetic layer; and the magnetization direction of the second ferromagnetic layer is influenced by the magnetization direction of the first ferromagnetic layer and the third ferromagnetic layer.

11. The logic circuit of claim 10, further comprising: a fourth ferromagnetic element having a fourth ferromagnetic layer; and a third transistor coupled to the fourth ferromagnetic element, wherein: the first current is indicative of a first digital input value; the second current is indicative of a second digital input value; the third transistor is configured to allow a third current to flow through the fourth ferromagnetic element, the third current being indicative of a third digital input value and influencing a magnetization direction of the fourth ferromagnetic layer; and the magnetization direction of the second ferromagnetic layer is indicative of a majority of the first digital input value, the second digital input value, and the third digital input value.

12. The logic circuit of claim 1, further comprising a sensing arrangement configured to identify a digital output value based on the magnetization direction of the second ferromagnetic layer.

13. A method for operating a logic circuit including an input ferromagnetic element and an output ferromagnetic element having a magnetization direction influenced by a magnetization direction of the input ferromagnetic element, the method comprising: activating an input transistor coupled to the input ferromagnetic element to allow an input current to flow through the input ferromagnetic element, the input current influencing the magnetization direction of the input ferromagnetic element; activating an output transistor coupled to the output ferromagnetic element to allow an output current to flow through the output ferromagnetic element, wherein a magnitude of the output current is influenced by the magnetization direction of the output ferromagnetic element; and determining the magnetization direction of the output ferromagnetic element in response to the output current; and determining a digital output value for the logic circuit based on the magnetization direction of the output ferromagnetic element.

14. The method of claim 13, further comprising operating an input current arrangement coupled to the input transistor to provide the input current in a direction corresponding to a digital input value.

15. The method of claim 14, the input ferromagnetic element including a first pinned layer and a first free layer and the output ferromagnetic element including a second pinned layer and a second free layer, a magnetization direction of the second free layer being influenced by a magnetization direction of the first free layer, wherein operating the input current arrangement comprises: operating the input current arrangement to provide the input current flowing from the first free layer to the first pinned layer in response to the digital input value corresponding to a

first digital value, the input current flowing from the first free layer to the first pinned layer resulting in the magnetization direction of the first free layer being opposite a magnetization direction of the first pinned layer; and operating the input current arrangement to provide the input current flowing to the first free layer from the first pinned layer in response to the digital input value corresponding to a second digital value, the input current flowing to the first free layer from the first pinned layer resulting in the magnetization direction of the first free layer being equal to a magnetization direction of the first pinned layer.

16. The method of claim 13, wherein determining the magnetization direction comprises: obtaining a voltage across the output ferromagnetic element in response to the output current; and determining the magnetization direction based on the voltage across the output ferromagnetic element.

17. The method of claim 16, wherein determining the magnetization direction based on the voltage across the output ferromagnetic element comprises: identifying a first digital value as the digital output value when the voltage across the output ferromagnetic element is greater than a threshold voltage; and identifying a second digital value as the digital output value when the voltage across the output ferromagnetic element is less than the threshold voltage.

18. A method for fabricating a logic circuit, the method comprising: forming a first ferromagnetic element having a first ferromagnetic layer; forming a second ferromagnetic element having a second ferromagnetic layer, wherein the second ferromagnetic element is arranged with respect to the first ferromagnetic element such that a magnetization direction of the first ferromagnetic layer influences a magnetization direction of the second ferromagnetic layer; forming a first transistor coupled to the first ferromagnetic element, wherein the first transistor is configured to allow a first current to flow through the first ferromagnetic element, the first current influencing the magnetization direction of the first ferromagnetic layer; and forming a second transistor coupled to the second ferromagnetic element, wherein the second transistor is configured to allow a second current to flow through the second ferromagnetic element.

19. The method of claim 18, wherein forming the first ferromagnetic element comprises forming the first ferromagnetic element overlying the first transistor.

20. The method of claim 19, further comprising: forming a layer of dielectric material overlying the first transistor; and forming a via in the layer of dielectric material, the via overlying a terminal region of the first transistor, wherein forming the first ferromagnetic element comprises: forming a third ferromagnetic layer overlying the layer of dielectric material, the third ferromagnetic layer being electrically connected to the via; forming an insulating layer overlying the third ferromagnetic layer; and forming the first ferromagnetic layer overlying the insulating layer, wherein the first current flows between the third ferromagnetic layer and the first ferromagnetic layer.

21. A logic circuit fabricated in accordance with any one of the claims 18-20.