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CLAIMS

What is claimed is:

- 5 1. A microelectronic device, comprising:
a stack structure having tiers each comprising a conductive structure and an insulating
 structure vertically neighboring the conductive structure;
a stadium structure within the stack structure and comprising:
 a forward staircase structure and having steps comprising edges of the tiers;
10 a reverse staircase structure opposing the forward staircase structure and having
 additional steps comprising additional edges of the tiers; and
 a central region horizontally interposed between the forward staircase structure and
 the reverse staircase structure;
a source tier underlying the stack structure and comprising discrete conductive structures
15 within horizontal boundaries of the central region of the stadium structure, the
 discrete conductive structures horizontally separated from one another by dielectric
 material; and
a masking structure confined within the horizontal boundaries of the central region of the
 stadium structure and vertically interposed between the discrete conductive
20 structures of the source tier and the central region of the stadium structure, the
 masking structure comprising segments horizontally covering portions of the
 dielectric material horizontally interposed between the discrete conductive
 structures.
- 25 2. The microelectronic device of claim 1, wherein the source tier comprises:
rows of the discrete conductive structures extending in a first horizontal direction; and
columns of the discrete conductive structures extending in a second horizontal direction
 orthogonal to the first horizontal direction.
- 30 3. The microelectronic device of claim 1, wherein the discrete conductive
structures of the source tier comprise conductively doped polycrystalline silicon.

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4. The microelectronic device of claim 1, wherein outermost horizontal boundaries of the masking structure are smaller than horizontal boundaries of the central region of the stadium structure.
- 5 5. The microelectronic device of claim 1, wherein some of the segments of the masking structure partially horizontally overlap some of the discrete conductive structures.
6. The microelectronic device of any one of claims 1 through 5, further comprising openings vertically extending through the masking structure and horizontally
10 positioned between the segments of the masking structure.
7. The microelectronic device of claim 6, wherein the openings within the masking structure are confined within horizontal boundaries of some of the discrete conductive structures.
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8. The microelectronic device of claim 6, wherein the openings within the masking structure are filled with dielectric fill material.
9. The microelectronic device of any one of claims 1 through 5, wherein the
20 masking structure comprises an electrically conductive material.
10. The microelectronic device of claim 9, wherein the electrically conductive material comprises elemental tungsten.

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11. A microelectronic device, comprising:
a stack structure comprising tiers each comprising an electrically conductive structure and a dielectric structure vertically neighboring the electrically conductive structure;
a stadium structure within the stack structure and comprising:
5 opposing staircase structures mirroring one another and each having steps
 comprising edges of at least some of the tiers; and
 a central region horizontally interposed between the opposing staircase structures;
 and
a source tier vertically below the stack structure and comprising:
10 discrete conductive structures within horizontal boundaries of the opposing
 staircase structures of the stadium structure; and
 an additional discrete conductive structure within horizontal boundaries of the
 central region of the stadium structure and having relatively larger
 horizontal dimensions than one or more of the discrete conductive
15 structures.

12. The microelectronic device of claim 11, wherein the additional discrete conductive structure of the source tier extends continuously in a first horizontal direction across the central region of the stadium structure from a vertically lowermost step of a first
20 of the opposing staircase structures of the stadium structure to a vertically lowermost step
of a second of the opposing staircase structures of the stadium structure.

13. The microelectronic device of claim 11, wherein the additional discrete conductive structure of the source tier horizontally extends across substantially all of a
25 horizontal area of the central region of the stadium structure.

14. The microelectronic device of any one of claims 11 through 13, wherein the additional discrete conductive structure of the source tier has substantially the same vertical position and substantially the same material composition as the discrete conductive
30 structures of the source tier.

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15. A memory device, comprising:
a stack structure comprising a vertically alternating sequence of conductive structures and
insulative structures arranged in tiers, each of the tiers individually comprising at
least one of the conductive structures and at least one of the insulative structures;
5 a stadium structure within the stack structure and comprising:
opposing staircase structures individually having steps comprising horizontal ends
of at least some the tiers; and
a central region horizontally intervening between the opposing staircase structures;
discrete conductive structures underlying the stack structure, a group of the discrete
10 conductive structures located within horizontal boundaries of the central region of
the stadium structure;
a conductive masking structure interposed between the discrete conductive structures and
the central region of stadium structure; and
strings of memory cells vertically extending through the stack structure.

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16. The memory device of claim 15, further comprising:
digit lines overlying the stack structure and electrically coupled to the strings of memory
cells;
a source structure underlying the stack structure and electrically coupled to the strings of
20 memory cells;
conductive contact structures on at least some of the steps of the opposing staircase
structures of the stadium structure;
conductive routing structures electrically coupled to the conductive contact structures; and
a control device electrically coupled to the source structure, the digit lines, and the
25 conductive routing structures.

17. The memory device of claim 16, wherein the source structure and the
discrete conductive structures are located at substantially the same vertical position as one
another.

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18. The memory device of any one of claims 15 through 17, wherein the
conductive masking structure is substantially confined within horizontal boundaries of the
central region of the stadium structure, the conductive masking structure horizontally
extending over less than all of the group of the discrete conductive structures located within
5 the horizontal boundaries of the central region of the stadium structure.

19. The memory device of claim 18, wherein a horizontal center of conductive
masking structure is substantially aligned with a horizontal center of the central region of
the stadium structure.

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20. The memory device of claim 18, wherein the conductive masking structure
further comprises openings vertically extending therethrough, horizontal centers the
openings substantially aligned with horizontal centers of some of the discrete conductive
structures of the group of the discrete conductive structures.

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21. The memory device of claim 20, further comprising a dielectric material
horizontally interposed between horizontally neighboring discrete conductive structures of
the group of the discrete conductive structures, vertically interposed between the group of
the discrete conductive structures and the conductive masking structure, and filling the
20 openings within the conductive masking structure.

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22. A 3D NAND Flash memory device, comprising:
a stack structure comprising vertically alternating conductive structures and insulating structures arranged in tiers, the stack structure comprising:
a distributed stadium region comprising stadium structures located at different
5 vertical positions than one another within stack structure, the stadium structures each individually comprising:
a forward staircase structure comprising edges of a portion of the tiers;
a reverse staircase structure mirroring the forward staircase structure and comprising additional edges of the portion of the tiers; and
10 a central region horizontally interposed between the forward staircase structure and the reverse staircase structure; and
a memory array region horizontally neighboring the distributed stadium region;
a source tier vertically underlying the stack structure and comprising:
a source structure within horizontal boundaries of the memory array region of the
15 stack structure; and
discrete conductive structures within horizontal boundaries of the distributed stadium region of the stack structure;
a masking structure vertically interposed between the discrete conductive structures and the stack structure, and substantially horizontally confined within horizontal boundaries
20 of the central region of one of the stadium structures positioned at a relatively lower vertical position within the stack structure; and
semiconductive pillar structures within horizontal boundaries of the memory array region of the stack structure and vertically extending through the stack structure.
23. The 3D NAND Flash memory device of claim 22, further comprising:
digit lines vertically overlying and within horizontal boundaries of the memory array region of the stack structure, the semiconductive pillar structures in electrical communication with the digit lines and the source structure; and
a control device vertically overlying and within horizontal boundaries of the memory array
30 region, the control device comprising CMOS circuitry in electrical communication with the source structure, the digit lines, and the conductive structures of the tiers of the stack structure.

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24. The 3D NAND Flash memory device of claim 22, wherein the discrete conductive structures of the source tier are electrically isolated from another and the source structure by at least one dielectric material.

5 25. The 3D NAND Flash memory device of any one of claims 22 through 24, wherein the masking structure comprises an electrically conductive material horizontally extending between and partially horizontally overlapping some of the discrete conductive structures horizontally neighboring one another within the horizontal boundaries of the central region of the one of the stadium structures.

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26. The 3D NAND Flash memory device of claim 25, wherein the masking structure further comprises filled openings vertically extending through the electrically conductive material and horizontally overlapping the some of the discrete conductive structures, the filled openings having dielectric material therein.

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27. The 3D NAND Flash memory device of any one of claims 22 through 24, further comprising a dielectric liner material substantially covering and surrounding horizontal boundaries and lower vertical boundaries of the masking structure.

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28. An electronic system, comprising:
- an input device;
- an output device;
- a processor device operably coupled to the input device and the output device; and
- 5 a memory device operably coupled to the processor device and comprising at least one microelectronic device structure comprising:
- a stack structure comprising tiers each comprising an electrically conductive structure and a dielectric structure vertically neighboring the electrically conductive structure;
- 10 a stadium structure within the stack structure and exhibiting steps comprising edges of at least some of the tiers;
- a source tier vertically below the stack structure and comprising discrete conductive structures within horizontal boundaries of the stadium structure; and
- a masking structure substantially confined within horizontal boundaries of a
- 15 horizontally central region of the stadium structure free of the steps, the masking structure comprising at least one masking material horizontally extending between and partially horizontally overlapping some of the discrete conductive structures of the source tier within the horizontal boundaries of the horizontally central region of the stadium structure.
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29. The electronic system of claim 28, wherein the memory device comprises a 3D NAND Flash memory device.