

The invention relates to a circuit arrangement for reversing a magnetic field.

Circuit arrangements of this type are used in magneto-optic recording and reproduction devices for example, in order to reverse the direction of magnetisation in the magnetic layer of a magneto-optic recording medium.

A known magneto-optic recording medium is the magneto-optic disc in which a magneto-optic layer, in which items of data are recordable and from which items of data are readable, is located behind a transparent layer. It will now be explained how the items of data are written onto a magneto-optic disc.

The magneto-optic layer is heated up to a temperature which is close to the Curie temperature by means of a laser beam that is focused onto the disc. Usually however, it is only necessary to heat up the magneto-optic layer to the compensation temperature which lies somewhat under the Curie temperature. An electromagnet, which magnetises the region heated by the laser beam in the one or other direction of magnetisation, is arranged behind the focal point on the disc. Because, after switching off the laser beam, the heated spot cools once more below the compensation temperature, the direction of magnetisation determined by the electromagnet is maintained. It is, so to speak, frozen-in. The individual bits are stored in this manner in domains having different directions of magnetisation. Thereby, the one direction of magnetisation of a domain corresponds, for example, to a logical one, while the opposite direction of magnetisation represents a logical zero.

One makes use of the Kerr effect for reading the items of data. The plane of polarisation of a linearly polarised light beam is rotated through a measurable angle in the course of the reflection at a magnetised mirror. In dependence upon the direction in which the mirror is magnetised, the plane of polarisation of the reflected light beam is rotated to the right or to the left. However, because the individual domains on the disc act like magnetised mirrors, the plane of polarisation of a scanning light beam is rotated through a measurable angle to the left or to the right in dependence upon the direction of magnetisation of the currently scanned domain.

The optical scanning device recognises which bit is present, a logical one or a logical zero, from the rotation of the plane of polarisation of the light beam reflected from the disc.

A circuit arrangement acting as an electromagnet having a coil behind the magneto-optic disc provides one known solution for magnetising the magneto-optic layer in the one or the other direction. The coil has to be dimensioned such that it is capable of reversing the magnetisation of the whole area which is covered by the optical scanning device. This area is, for example, a radial or arc-like strip, which runs from the edge of the disc to the centre of the disc, in dependence on the type of recording and reproduction device. The cross-section and thus the inductance of the coil are relatively large because the field strength in the whole strip must reach a minimum value in order to be able to reverse the magnetisation of the strip.

In another known solution, the coil is attached to the optical scanning device. The coil may, for example, be wrapped around the objective lens of the optical scanning device. Because the coil together with the optical scanning device is guided along the data tracks on the magneto-optic disc by means of a tracking control loop in this solution, a smaller cross-section and thus a smaller inductance are sufficient to generate the same minimum field strength since it is not a radial or arc-like strip but rather, a small, for example, circular region in the magneto-optic layer having the virtually point-like laser spot as the centre point which has its magnetisation reversed.

In the article "A simple digital tape head driver" by Robert S. Olla which appeared in Electronic Engineer, Vol 31, No 2, February 1972, Radnor US at page DC-9, the author described a magnetic head driver for a digital tape recording device.

A series circuit consisting of the collector-emitter paths of two transistors, which serve as electronic switches, is located in parallel with an oscillatory circuit. The two transistors are alternately opened and closed by a respective control signal on the bases in order to reverse the direction of the current through the coil in the oscillatory circuit. The direction of the magnetic field in the coil is thereby reversed.

A further switching arrangement for reversing a magnetic field is known from the US-PS 3 400 304.

A capacitance is connected to each terminal of a coil. Energy is initially supplied to the coil and one of the two capacitances from a first voltage source by means of four transistors, which are provided as electronic switches. In the next step, the coil and this capacitance are disconnected from the voltage source in order to produce resonance in the oscillatory circuit formed by the coil and the one capacitance. The resonance in the

oscillatory circuit is interrupted by switching over the transistors, which are serving as electronic switches, whereby an induced voltage is generated in the coil.

Finally, energy is supplied to the coil and to the other capacitance from a second voltage source. The coil and the other capacitance are disconnected from the second voltage source so that resonance is now caused in the oscillatory circuit consisting of the coil and the other capacitance. The resonance in the oscillatory circuit is inhibited by switching over the switches in order to generate an induced voltage in the coil. The starting state, in which the first voltage source again supplies energy to the coil and the one capacitance, is now restored.

The object of the invention is now, to produce a circuit arrangement including a coil such that an assured and rapid reversal of the magnetic field is achieved.

The invention achieves this object by the features given in claim 1. A second solution of the invention is specified in claim 2.

There is shown in

Figures 1 to 9 a first embodiment of the invention in different switching states

Figure 10 a diagram in which the switching states of the controllable switches as well as the current and voltage waveform for the first embodiment are plotted with respect to time

Figure 11 a second embodiment of the invention

Figure 12 a diagram in which the switching states of the controllable switches as well as the current and voltage waveforms for the second embodiment are plotted with respect to time

Figure 13 a first embodiment of a control circuit for controlling the controllable switches

Figure 14 a diagram in which the control signals for the controllable switches as well as the current and voltage waveforms are plotted with respect to time

Figure 15 a second embodiment of a control circuit for controlling the controllable switches

Figure 16 a diagram in which the control signals for the controllable switches as well as the current and voltage waveforms are plotted with respect to time

Figure 17 a third embodiment of the invention .

The first embodiment of the invention will be now be described and thereafter explained with the help of the Figures 1 to 9.

In Figure 1, a series circuit consisting of two oppositely poled diodes D1 and D2 is located in parallel with an oscillatory circuit consisting of a coil L and a capacitance C. The diode D1 can be shunted by means of a controllable switch S1 and the diode D2 by means of a controllable switch S2. The one terminal A of the oscillatory circuit is connected via a series circuit consisting of a resistance R1 and a controllable switch S3 to the one pole of a voltage source +U whose other pole is connected to the common connection point of the two diodes D1 and D2. The other terminal B of the oscillatory circuit is likewise connected via a series circuit consisting of a resistance R3 and a controllable switch S4 to the one pole of the voltage source +U.

A control circuit S, whose outputs A1 to A4 are connected to the control inputs of the controllable switches S1 to S4, open and close the controllable switches S1 to S4 in a cyclical sequence which will now be explained with the help of the Figures 1 to 10.

In Figure 1, the controllable switches S1 and S2 are closed whereas the controllable switches S3 and S4 are open. For the sake of simplicity and for an easier understanding of the invention, it will be assumed that the coil L is a lossless inductance in which magnetic energy is already stored. Consequently, a current I flows, in the direction indicated by the arrow, in the current circuit which the coil L and the two controllable switches S1 and S2 form. The manner of operation of the voltage source +U, of the controllable switches S3 and S4 as well as of the resistances R1 and R2 will be gone into later on.

In order to reverse the direction of the magnetic field, the control circuit S opens the controllable switch S1. Then, because the current flow through the branch consisting of the two controllable switches S1 and S2 which runs parallel to the coil L is interrupted, the current I now flows via the

capacitance C which is thereby charged, as is shown in Figure 2. However, during the charging process, the current I through the coil falls until it finally becomes zero when the voltage U_c on the capacitance C is at its greatest. This state is illustrated in Figure 3. Because the capacitance C now begins to discharge, the current I then flows through the coil L in the other direction as is indicated by the current arrow in Figure 4. However, as soon as the voltage U_c on the capacitance C has fallen to zero, the diode $D1$ begins to conduct. The current I continues to flow in the same direction through the coil L of course, however, it is now no longer via the capacitance C but rather, via the controllable switch $S2$ and the diode $D1$. This state is shown in Figure 5.

In Figure 6, the control circuit S opens the controllable switch $S2$ while it simultaneously closes the controllable switch $S1$. The capacitance is now charged up in the opposite direction until the voltage U_c on the capacitance C adopts the largest negative value. The current I through the coil L is then zero as is shown in Figure 7.

The current flow through the coil L reverses because the capacitance C now discharges again. This is illustrated in Figure 8.

The diode $D2$ begins to conduct as soon as the voltage U_c on the capacitance C is zero. The current I flows in the loop which is formed by the coil L , the diode $D2$ and the controllable switch $S1$ as is shown in Figure 9. The control circuit S now closes the controllable switch $S2$; consequently, the starting state illustrated in Figure 1 is reached once more.

However, because the coil L , the capacitance C , the two diodes $D1$ and $D2$ as well as the two controllable switches $S1$ and $S2$ are not lossless components but rather components having ohmic losses, energy has to be supplied to the oscillatory circuit. Consequently, the control circuit S closes the controllable switch $S3$ when it opens the controllable switch $S1$. Due to this measure, the oscillatory circuit is connected to the voltage source $+U$ as is shown in Figure 2. Likewise, the control circuit S closes the controllable switch $S4$ when it closes the controllable switch $S1$ and opens the controllable switch $S2$. The oscillatory circuit is now likewise connected to the voltage source $+U$. This connection state is apparent from Figure 6.

The current I through the coil L , the voltage U_c on the capacitance C and the switching states of the controllable switches $S1$ to $S4$ in dependence on the time t are shown in

Figure 10. At the time point $t = 0$, the controllable switches S3 and S4 are open while the controllable switches S1 and S2 are closed. The controllable switch S2 can however also be open because the diode D2 is conducting.

As already explained, the controllable switch S1 is opened and the controllable switch S3 is simultaneously closed for the reversal of the magnetic field. The current I through the coil L falls whilst the voltage U_c on the capacitance C simultaneously rises. The voltage U_c adopts its maximum, when the current I through the coil L becomes zero. At this time point t_1 , the controllable switch S3 is re-opened; the controllable switch S2 must be closed, at the latest, at the time point t_1 . The current I is now negative whilst the voltage U_c simultaneously falls to the value zero. The current I now has its greatest negative value. The controllable switch S1 may be closed, at the earliest, at this time point t_2 . At the time point t_3 , the control circuit S opens the controllable switch S2 whilst it simultaneously closes the controllable switch S4. The current I falls to zero; the voltage U_c on the capacitance C simultaneously becomes negative. The greatest negative voltage U_c is present on the capacitance C when the current I is zero. At this time point t_4 , the controllable switch S4 is re-opened; the controllable switch S1 must be closed, at the latest, at the time point t_4 . The current I continues to rise to its greatest positive value whilst the voltage U_c simultaneously falls to the value zero. At this time point t_5 , the controllable switch S2 may already be closed. The position of the switches S1 to S4 is arbitrary in the hatched regions. The resistances R_1 and R_2 serve for limiting the current through the oscillatory circuit.

A second embodiment of the invention will now be described and explained with the aid of Figures 11 and 12.

The second embodiment shown in Figure 11 differs from the first by virtue of another way of supplying energy. The parallel circuit consisting of the oscillatory circuit, the diodes D1 and D2 and the controllable switches S1 to S4 is constructed in exactly the same way as in the first embodiment. However, the one terminal A of the oscillatory circuit is connected to the one electrode of a diode D3 whose other electrode is connected via a controllable switch S3 to the one pole of a voltage supply $-U$ and via a series circuit consisting of an inductance L_2 and a resistance R_1 to the other pole of the voltage supply $-U$. The other terminal B of the oscillatory circuit is connected in the same way to the one electrode of a diode D4 whose other electrode is connected via a controllable switch S4 to the one pole of the voltage supply $-U$ and via a series circuit

consisting of an inductance L_3 and a resistance R_2 to the other pole of the voltage supply $-U$.

The current I through the coil, the voltage U_c on the capacitance C and the position of the controllable switches S_1 to S_4 are plotted with respect to time t in Figure 12.

The current waveform and the voltage waveform as well as the position of the controllable switches S_1 and S_2 coincides with those of Figure 10. The supplying of energy does not occur by direct application of the voltage of a supply voltage source but rather, by application of an induced voltage. Consequently, the controllable switches S_3 and S_4 are briefly opened each time that the capacitance C is charged - positively or negatively. The diodes D_3 and D_4 are poled such that current flows through the inductances L_2 and L_3 but not in the oscillatory circuit when the controllable switches S_3 and S_4 are closed.

In Figure 12, the controllable switch S_3 is now opened at the time point t_1 when the capacitance C is positively charged. An induced voltage, which is supplied to the capacitance C , arises in the inductance L_2 due to the opening of the controllable switch S_3 . The controllable switch S_2 may be re-closed, at the earliest, at the time point t_2 when U_c is a maximum and I is zero. The controllable switch S_4 is opened at the time point t_3 when the capacitance C is negatively charged. The induced voltage occurring on the inductance L_3 now balances out the energy loss in the oscillatory circuit. The controllable switch S_4 may be re-closed, at the earliest, at the time point t_4 when the voltage U_c adopts the greatest negative value. The position of the switches S_1 to S_4 is arbitrary in the hatched regions. The resistances R_1 and R_2 are effective, as in the first embodiment, as current limiters. As opposed to the first embodiment, the second has the advantage that the high voltage for balancing out the energy loss in the oscillatory circuit is not produced by a mains unit but, in a simple manner, in an inductance. Thus, the voltage $-U$ in the second embodiment can be selected to be a factor of ten smaller than the voltage $+U$ in the first embodiment.

The third embodiment of the invention depicted in Figure 17 differs from the second embodiment of Figure 11 in that two further diodes D_5 and D_6 are provided. The one additional diode, the diode D_5 , which is oppositely poled to the diode D_3 , is located between the controllable switch S_3 and the common connection point of the diode D_3 and the inductance L_2 . The other additional diode, the diode D_6 , which is oppositely poled

to the diode D4, is connected between the controllable switch S4 and the common terminal of the diode D4 and the inductance L3.

If transistors are provided for the controllable switches S3 and S4, the diodes D5 and D6 cause a more rapid discharging of the parasitic capacitance in the inductances L2 and L3 as will now be explained on the basis of the example of the diode D5 and the inductance L2.

When the controllable switch S3 is closed - i.e. the transistor provided therefor is conductive, the voltage $-U$ is present on the inductance L2 whilst the current through the inductance L2 climbs linearly. As soon as the controllable switch S3 is opened, i.e. the transistor is blocked, the potential on the one terminal of the inductance L2, which is connected to the diodes D3 and D5, quickly climbs to a maximum value because of the induced voltage, whilst the current through the inductance L2 falls to the value zero. Thereafter, however, the potential on the one terminal of the inductance L2 falls back again. When it has dropped to the value zero, the current reaches a minimum. The potential continues to fall whilst the current through the inductance L2 simultaneously climbs up again from the minimum to the value zero. However, without the diode D5, it cannot become negative with respect to the negative pole of the voltage supply source $-U$ because the diode of the transistor serving as a controllable switch is then switched through. Consequently, without the diode D5, the parasitic capacitance of the inductance L2 can only be slowly discharged. Therefore, when the controllable switch S3 is re-closed, the parasitic capacitance is not completely discharged and consequently the inductance L2 is not yet free of current. The diode D5 is provided in order to avoid this disadvantage, since the potential at the one terminal of the inductance L2 cannot become negative with respect to the negative pole of the voltage supply source $-U$ because it blocks this node from the negative pole of the voltage supply source $-U$. The parasitic capacitance of the inductance L2 is thereby more quickly discharged and, as a result thereof, the inductance L2 becomes free of current more quickly.

By appropriate dimensioning of the inductance L2 and suitable choice of the enabling time points of the controllable switch S3, one can even cause a residual current to flow in the inductance L2 in the same direction as the current caused by the voltage supply source $-U$ upon the enablement of the controllable switch S3. Consequently, due to this residual current, the current in the inductance L2 rises more quickly to the maximum value than would be the case for an inductance L2 that is free

of current at the time point when the controllable switch S3 is enabled.

As already mentioned, the invention is suitable for reversing the magnetisation of the magnetic layer of a magneto-optic recording medium.

The items of data are stored on magneto-optic CD discs in accordance with the eight-to-fourteen modulation-code, abbreviated EFM.

A first embodiment of a control circuit for controlling the controllable switches S1 to S4, to which the items of data that are to be recorded are supplied for example, is shown in Figure 13.

The clock pulses T of a clock pulse generator G and a digital signal DS, which would be an EFM signal in a CD player for example, are supplied to a shift register SR. The digital signal DS is present on the first output T1 of the shift register SR which is connected to the non-inverting input of a NAND gate N1 and N2 as well as to the inverting input of a NAND gate N3 and N4. The digital signal DS1, which is delayed by one clock pulse, is derived from the second output T2 of the shift register SR which is connected to the inverting input of the NAND gate N1 and N4. The third output T3 of the shift register SR, at which the digital signal DS2 which is delayed by two clock pulses is emitted, is connected to the inverting input of the NAND gate N2 and N3. The control signal for the controllable switch S3 is derivable from the output of the NAND gate N1, the control signal for the controllable switch S2 is derivable from the output of the NAND gate N2, the control signal for the controllable switch S1 is derivable from the output of the NAND gate N3 and the control signal for the controllable switch S4 is derivable from the output of the NAND gate N4.

The digital signal DS, the digital signal DS1 which is delayed by one clock pulse, the digital signal DS2 which is delayed by two clock pulses, the current I through the coil L, the voltage U_c on the capacitance C as well as the control signals for the controllable switches S1 to S4 are plotted with respect to time t in Figure 14. The digital signal may be a data signal constructed in accordance with the EFM code for example.

A second embodiment of a control circuit for controlling the controllable switches S1 to S4 is shown in Figure 15.

The data signal DS is likewise supplied to a shift register SR which is clocked by the clock pulses T from a clock pulse generator G. The output T1 of the shift register SR, at which the data signal DS1 that is delayed by one clock pulse is emitted, is connected to the inverting input of a NAND gate N1 and to the non-inverting input of a NAND gate N4. The output T2 of the shift register SR, which delivers the data signal DS2 that is delayed by two clock pulses, is connected to the non-inverting input of the NAND gate N1 and to the inverting input of the NAND gate N4. The output T4, from which the data signal DS4 that is delayed by four clock pulses is derivable, is connected to the inverting input of a NAND gate N2 and to the inverting input of a NAND gate N3. The output T5, which emits the data signal DS5 that is delayed by five clock pulses, is connected to the non-inverting input of the NAND gate N2 and to the inverting input of a NAND gate N5. The output T6, which delivers the data signal DS6 that is delayed by six clock pulses, is connected to the non-inverting input of the NAND gate N3 and to the inverting input of the NAND gate N6. The control signal for the controllable switch S3 is derivable from the Q-output of an RS flip-flop FF1 whose set input is connected to the output of the NAND gate N1 and whose reset input is connected to the output of the NAND gate N2. The control signal for the controllable switch S4 is derivable from the Q-output of an RS flip-flop FF2 whose set input is connected to the output of the NAND gate N4 and whose reset input is connected to the output of the NAND gate N5. The control signal for the controllable switch S1 is present at the output of the NAND gate N3 while the output of the NAND gate N6 delivers the control signal for the controllable switch S2. AND gates for example, may be used instead of NAND gates if the flip-flops react to rising edges.

The clock pulses T, the data signal DS, the signals DS1 - DS5 at the outputs T1, T2, T4, T5 and T6 of the shift register SR, the signal SN1 at the output of the NAND gate N1, the signal SN2 at the output of the NAND gate N2, the signal SN4 at the output of the NAND gate N4, the signal SN5 at the output of the NAND gate N5, the signals S1 - S4 for controlling the controllable switches S1 - S4, the current I2 through the inductance L2, the current I3 through the inductance L3, the current I through the coil L and the voltage U_c are plotted with respect to time t in Figure 16. A further explanation of the pulse diagrams shown in the Figure 16 will be dispensed with because the manner of operation of a NAND gate and of a flip-flop are known to the skilled person.

For magneto-optic recording and reproduction devices, the invention offers the advantage that data already recorded on the magneto-optic disc can be directly over-written. In contrast, in known magneto-optic recording and reproduction devices, the old items of data have to be erased before new items of data are recorded.

To this end, the magneto-optic layer is heated up to the compensation temperature by the laser at the positions where the new items of data are intended to be stored. These positions are thereby magnetised in the one direction. The disc is initialised, as is the technical expression for this process. Thereafter, the direction of the magnetic field produced in the coil is then reversed.

For recording the new items of data, the laser power is switched between a small and a large value in dependence on the bit which is to be stored. If, for example, a logical zero is stored at the previously erased location, then the laser operates at low power so that the compensation temperature is not reached. For recording a logical one on the other hand, the laser heats up the location which is to be newly written to the compensation temperature so that this location can be reverse magnetised by the coil. Items of data on the magneto-optic disc are first erased in this laborious manner before the new items of data are subsequently recorded.

The invention is not only suitable for magneto-optic devices but is also suitable for other magnetic recording devices.



Claims

1. Circuit arrangement for reversing a magnetic field, wherein a series circuit consisting of a first and a second diode (D1, D2) which are oppositely poled is connected in parallel with an oscillatory circuit consisting of a coil (L) and a capacitance (C), wherein the first diode (D1) can be shunted by a first controllable switch (S1) and the second diode (D2) by a second controllable switch (S2), wherein the first controllable switch (S1) is opened for reversing the magnetic field, wherein the second controllable switch (S2) is closed, at the latest, when the voltage (Uc) on the capacitance (C) has risen to the one extreme value, wherein the first controllable switch (S1) is closed, at the soonest, when the voltage (Uc) on the capacitance has fallen again from the one extreme value to zero, wherein the second controllable switch (S2) is opened for a renewed reversal of the magnetic field but not before the voltage (Uc) on the capacitance (C) has fallen from the one extreme value to zero, wherein the first controllable switch (S1) is closed, at the latest, when the voltage (Uc) on the capacitance (C) has risen to the other extreme value, that the second controllable switch (S2) is closed, at the soonest, when the voltage (Uc) on the capacitance (C) has fallen again from the other extreme value to zero, wherein the one terminal (A) of the oscillatory circuit is connected via a third controllable switch (S3) to the one pole of a voltage source (+U) and the other terminal (B) of the oscillatory circuit is connected via a fourth controllable switch (S4) to the one pole of a voltage source (+U) whose other pole is connected to the common connection point of the two diodes (D1, D2), wherein the control circuit (S) closes the third controllable switch (S3) when the first controllable switch (S1) is opened whereas the second controllable switch (S2) is closed, wherein the control circuit (S) re-opens the third controllable switch (S3) when the capacitance (C) has charged, wherein the control circuit (S) closes the fourth controllable switch (S4) when the second controllable switch (S2) is opened whereas the first controllable switch (S1) is closed and wherein the control circuit (S) re-opens the fourth controllable switch (S4) when the capacitance (C) has charged.

2. Circuit arrangement for reversing a magnetic field, wherein a series circuit consisting of a first and a second diode (D1, D2) which are oppositely poled is connected in parallel with an oscillatory circuit consisting of a coil (L) and a capacitance (C), wherein the first diode (D1) can be shunted by a first controllable switch (S1) and the second diode (D2) by a second controllable switch (S2), wherein the first controllable switch (S1) is opened for reversing the magnetic field, wherein the



second controllable switch (S2) is closed, at the latest, when the voltage (U_c) on the capacitance (C) has risen to the one extreme value, wherein the first controllable switch (S1) is closed, at the soonest, when the voltage (U_c) on the capacitance (C) has fallen again from the one extreme value to zero, wherein the second controllable switch (S2) is opened for a renewed reversal of the magnetic field but not before the voltage (U_c) on the capacitance (C) has fallen from the one extreme value to zero, wherein the first controllable switch (S1) is closed, at the latest, when the voltage (U_c) on the capacitance (C) has risen to the other extreme value, wherein the second controllable switch (S2) is closed, at the soonest, when the voltage (U_c) on the capacitance (C) has fallen again from the other extreme value to zero, wherein the one terminal (A) of the oscillatory circuit is connected to the one electrode of a third diode (D3) whose other electrode is connected via a third controllable switch (S3) to the one pole of a voltage source ($-U$) and via a second inductance (L2) to the other pole of the voltage source ($-U$), wherein the other terminal (B) of the oscillatory circuit is connected to the one electrode of a fourth diode (D4) whose other electrode is connected via a fourth controllable switch (S4) to the one pole of the voltage source ($-U$) and via a third inductance (L3) to the other pole of the voltage source ($-U$), wherein the control circuit (S) closes the third controllable switch (S3) a predetermined period of time before the opening of the first controllable switch (S1) and opens it simultaneously with the first controllable switch (S1) and wherein the control circuit (S) closes the fourth controllable switch (S4) a predetermined period of time before the opening of the second controllable switch (S2) and opens it simultaneously with the second controllable switch (S2).

3. Circuit arrangement in accordance with Claim 1, wherein a first resistance (R1) is in series with the third controllable switch (S3) and a second resistance (R2) is in series with the fourth controllable switch (S4).

4. Circuit arrangement in accordance with Claim 2, wherein a fifth diode (D5) which is oppositely poled to the third diode (D3) is located between the third controllable switch (S3) and the common connection point of the third diode (D3) and the second inductance (L2) and wherein a sixth diode (D6) which is oppositely poled to the fourth diode (D4) is located between the fourth controllable switch (S4) and the common connection point of the fourth diode (D4) and the third inductance (L3).



5. Circuit arrangement in accordance with Claim 1, 2, 3 or 4, wherein a control circuit (S) cyclically repeats the switching sequences of the first and second controllable switches (S1, S2).

6. Circuit arrangement in accordance with Claim 2 or 4, wherein a digital signal (DS) is present on the input of a shift register (SR) which is clocked by a clock pulse generator (G), wherein the signals (DS1, DS2, DS3, DS4, DS5) at the outputs (T1, T2, T3, T4, T5, T6) of the shift register (SR) are logically combined in a logic circuit (N1, N2, N3, N4, N5, N6) and wherein the control signals for the controllable switches (S1, S2, S3, S4) are derivable from the outputs of the logic circuit (N1, N2, N3, N4, N5, N6).

7. Circuit arrangement in accordance with Claim 6, wherein four outputs of the logic circuit (N1, N2, N3, N4, N5, N6) are connected to the inputs of two RS flip-flop (FF1, FF2) from whose outputs the control signals for two controllable switches (S3, S4) are derivable.