IMPROVEMENTS IN OR RELATING TO INTEGRATED LIGHT DETECTING OR GENERATING MEANS AND AMPLIFYING MEANS

This invention relates to integrated light detection or generating means and amplifying means and more particularly to light sources such as light emitting diodes, or light detectors such as photodiodes integrated with amplifiers such as field effect transistors, resistors and capacitors in various group III-V multilayer structures to form a monolithic structure.

The term "light" used herein includes invisible light such as infra-red and ultra violet.

Several such integrated systems are known in which an amplifier comprising a junction F.E.T. is formed in a localised diffusion step through a window in an oxide mask. The disadvantages of this method are that low doped layers are deteriorated during the diffusion drive in step and spreading during diffusion tends to lengthen the gate and so reduce the mutual conductance achievable.

It is an object of the present invention therefore to provide integrated light detection or generation means and amplifying means which will overcome these disadvantages.

According to the present invention there is provided integrated light detecting or generating means

and amplifying means comprising a field effect transistor comprising a semi-insulating substrate on which are formed source and drain layers separated by a groove, a first layer and a second layer on top of the first layer formed in said groove forming a gate bridging the source and drain layers, and light detecting or generating means formed of the same layers as the gate to form a monolithic structure.

The light detecting or generating means which are formed from the same layers which form the gate maybe directly formed on a semi-insulating substrate but are preferably formed to be one and the same as the gate.

The layers forming the light detecting or generating means preferably define a light detector such as a photo-diode.

Alternatively the above mentioned layers may define a light source such as a light emitting diode.

Preferably when the above mentioned layers form a light detector it comprises a p-n photo-diode consisting of p-type layers which also form part of the gate.

The source and drain layers preferably each comprise a buffer layer, high conductivity source and drain layers and a high resistance cover layer.

Preferably the groove between the source and drain layer is V shaped and the gate and the light detecting

or generating means are formed in the groove.

A method of making integrated light detecting or generating means and amplifying means comprising the steps of forming a field effect transistor high conductivity soure/drain layer on a semi-insulating substrate, forming a groove to divide the layer into two parts to separate the source and drain, producing an field effect transistor first and second layers in the groove to produce a gate to bridge the drain and source and producing light detecting or generating means formed of said first and second layers.

The FET high conductivity source/drain layer is preferably formed by a first epitaxial growth step, and the FET gate and the light detecting or generating means are preferably formed by a second epitaxial growth step.

The groove is preferably V shaped and formed by etching.

Embodiments of the invention will now be described by way of example only with reference to the accompanying drawings in which,

Figures 1 to 3 illustrate sequentially the steps of producing an integrated photodiode and FET amplifier according to the invention,

Figure 4 is a perspective view of a completed FET integrated with a separate detector diode and,

Figure 5 is a perspective view of a completed FET integrated with a detector diode formed on top of the FET.

A method of making simultaneously a photodiode and a short gate junction FET on a semi-insulating InP substrate 16 is illustrated in Figures 1 to 3.

An FET buffer layer 10, a high conductivity n^+ source/drain layer 12 and a high resistance n type cover layer 14 are grown in a single expitaxial growth step. The layer sequence is shown in Figure 1.

The layer 14 is then covered by a layer of photoresist 18 and slot 20 of lum is opened in the layer 18. The layers 10, 12 and 14 are then etched using a crystal orientation dependent etch to produce a V groove 22 to a depth such that the apex of the V groove divides the high conductivity n^+ source/drain contact layer 12. See Figure 2.

The remainder of the photoresist layer is then removed and in a second epitaxial growth step the following layers are deposited:- an n type GaInAs layer 24, a p type GaInAs layer 26 and a p type InP layer 28. These are deposited conformally so that the GaInAs layer 24 bridges the gap in the n^+ layer 12.

Precision depth etching through photoresist patterns is performed to define a groove 12 and hence to define the boundaries of a source 30, a drain 32

and a gate 34 and in some embodiments to define a separate p-n/diode 36 which can either be detached from the FET as shown in Figure 4 or on top of the FET and connected directly to the gate as shown in Figure 5.

An insulating layer e.g. SiO_2 (not shown) is deposited, windows opened by photoengraving and n and p type metallisations applied using engraving and float-off techniques. The oxide is needed to isolate inter-connections and these are taken over appropriate mesa edges to preserve electrical continuity.

The scheme shown does not easily allow the inclusion of high value resistors so a resistor deposition stage is needed for most useful integration.

The 'V' groove infilled gate FET has short (submicron) gate lengths so that high mutual conductance result.

The thin n FET layer 24 is controllably infilled so that the high conductivity materials necessary for high gm may be utilised.

The infilled FET layer 24 is GaInAs which has excellent transport properties for FET's.

The important gate/drain and gate/source capacitances which are likely to be higher than that of a MESFET may be reduced because of the high resistance layer 14 grown onto the source/drain n^+ LAYER 12.

The gate junction infill 34 forms a detector in itself whose geometry can be tailored to that required for good optical coupling.

Detection out to 1.6um can be achieved in the heterostructure detection layer.

Both photofets and integrated diode-FETs are realisable using this method.

Infilling by liquid phase epitaxy produces thicker layers on concave regions of the surface. This means that to fully pinch off the FET in the apex of the 'V' sufficient negative bias is needed to significantly deplete the layer 14 so reducing the source/drain to gate capacitance.

The detector diode structure is ppnin$^+$ which behaves as a p-i-n- structure once the central n and i layers 12, 14 have been fully depleted.

Figure 4 illustrates a junction FET 38 integrated with a separate detector diode 40, the detector being connected to the gate of the FET by a metallic conductor 42. Metallic contact pads 44, 46, 48, 50 are provided for the input and output to the diode and the source and drain of the FET.

Figure 5 illustrates a junction FET 52 integrated with a photodiode 54 which is mounted directly on the gate 56 of the FET. Again contact pads 58, 60 are

provided for the source and drain, and a further contact pad 62 is provided which is connected to the gate of the FET.

Whilst an integrated FET and a photodiode has been described the invention is equally applicable to an integrated FET and a light source, such as an LED.

CLAIMS

1. Integrated light detecting or generating means and amplifying means comprising a field effect transistor comprising a semi-insulating substrate on which are formed source and drain layers separated by a groove, a first layer and a second layer on top of the first layer formed in said groove forming a gate bridging the source and drain layers, and light detecting or generating means formed of the same layers as the gate to form a monolithic structure.

2. Integrated means as claimed in claim 1 which said light detecting generating means are directly formed on a semi-insulating substrate and are connected to the layers forming the gate via connector means.

3. Integrated means as claimed in claim 1 in which said light detecting or generating means and the gate are one and the same.

4. Integrated means as claimed in claim 1 in which said light detecting or generating means are formed on top of the source or drain layers and is connected directly to the layers forming the gate in the groove.

5. Integrated means as claimed in any preceding claim in which said light detecting means comprising a p-n photodiode consisting of p-type layers which also form part of the gate.

6. Integrated means as claimed in any preceding claim in which said source and drain layers each comprises a buffer layer, high conductivity source and drain layers and a high resistance cover layer.

7. Integrated means as claimed in any preceding claim in which said groove between the source and drain layers is V shaped.

8. A method of making integrated light detecting or generating means and amplifying means comprising the steps of forming a field effect transistor high conductivity source/drain layer on a semi-insulating substrate, forming a groove to divide the layer into two parts to separate the source and drain, producing an field effect transistor first and second layers in the groove to produce a gate to bridge the drain and source and producing light detecting or generating means formed of said first and second layers.

9. A method as claimed in claim 8 in which said field effect transistor high conductivity source/drain layer is formed by a first epitaxial growth step and the field effect transistor first and second layers and the light detecting or generating means are formed by a second epitaxial growth step.

10. Integrated light detecting or generating means and amplifying means constructed and adapted to operate

as hereinbefore described with reference to Figures 1 to 5, 4 or 5 of the accompanying drawings.

11. A method of making integrated light detecting or generating means substantially as hereinbefore described with reference to Figures 1 to 3, 4 or 5 ofthe accompanying drawings.