

Description

Title of Invention: COMMUNICATION DEVICE AND COMMUNICATION SYSTEM

Technical Field

[0001] The present disclosure relates to a communication apparatus, a communication method, a program, and a communication system, and more specifically relates to a communication apparatus, a communication method, a program, and a communication system which are capable of performing communication more reliably.

[0002] <CROSS REFERENCE TO RELATED APPLICATIONS>

This application claims the benefit of Japanese Priority Patent Application JP 2016-099930 filed on May 18, 2016, the entire contents of which are incorporated herein by reference.

Background Art

[0003] As a bus interface (IF) used for communication between a plurality of devices through a bus in a board mounting the devices, for example, an Inter-Integrated Circuit (I2C) has been widely used.

[0004] Furthermore, it has been desired to increase the speed of the I2C recently, and an Improved Inter Integrated Circuit (I3C) has been defining as a standard for the next-generation. In the I3C, a master and a slave can perform communication bidirectionally using two signal lines, and, for example, data transfer from the master to the slave (write transfer) and data transfer from the slave to the master (read transfer) are performed.

[0005] For example, Patent Literature 1 discloses a digital data processing system in which a host processor and a subsystem controller are interconnected by an I2C. Furthermore, Patent Literature 2 discloses a method for implementing a communication protocol arranged in layers on the standard I2C protocol.

Citation List

Patent Literature

[0006] PTL 1: JP 2000-99448 A
PTL 2: JP 2002-175269 A

Summary of Invention

Technical Problem

[0007] Incidentally, in the above described I3C, it is defined that, for example, a master and a slave perform error detection by parity, cyclic redundancy check (CRC), or the like,

but a signal for which the error detection is not prepared is also transmitted/received. Thus, when an error occurs in a signal for which the error detection is not prepared, the I3C is sometimes in a state in which both of the master and the slave do not drive a data signal line. Thus, there is a concern that it may be difficult to, for example, detect whether received data is correct, and to perform normal communication.

[0008] The present disclosure has been made in view of such a situation, and is to perform communication more reliably.

Solution to Problem

[0009] A communication apparatus of a first aspect of the present disclosure includes a transmission/reception unit which transmits/receives a signal to/from another communication apparatus, and an error detection unit which detects error occurrence by performing parity check to data received by the transmission/reception unit, in which the error detection unit performs error detection assuming one bit of 2-bit parity included in the data as even parity, and the other bit as odd parity.

[0010] A communication method or a program of the first aspect of the present disclosure includes transmitting/receiving a signal to/from another communication apparatus, detecting error occurrence by performing parity check to received data, and performing error detection assuming one bit of 2-bit parity included in the data as even parity, and the other bit as odd parity.

[0011] In the first aspect of the present disclosure, the error occurrence is detected by transmitting/receiving a signal to/from the other communication apparatus, and performing parity check to received data. Then, the error detection is performed assuming one bit of 2-bit parity included in the data as even parity, and the other bit as odd parity.

[0012] A communication system of a second aspect of the present disclosure includes a first communication apparatus which has control initiative in a bus, and a second communication apparatus which performs communication according to control by the first communication apparatus, in which the first communication apparatus and the second communication apparatus each include a transmission/reception unit which transmits/receives a signal, and an error detection unit which detects error occurrence by performing parity check to data received by the transmission/reception unit, and the error detection unit performs error detection assuming one bit of 2-bit parity included in the data as even parity, and the other bit as odd parity.

[0013] In the second aspect of the present disclosure, the error occurrence is detected by transmitting/receiving a signal, and performing parity check to received data. Then, the error detection is performed assuming one bit of 2-bit parity included in the data as even parity, and the other bit as odd parity.

Advantageous Effects of Invention

[0014] According to the first and second aspects of the present disclosure, it is possible to perform communication more reliably.

Brief Description of Drawings

[0015] [fig.1]Fig. 1 is a block diagram illustrating a configuration example of an embodiment of a bus IF to which the present technology is applied.

[fig.2]Fig. 2 is a diagram explaining an error which occurs in a preamble.

[fig.3A]Fig. 3A is a diagram explaining error detection by parity.

[fig.3B]Fig. 3B is a diagram explaining error detection by parity.

[fig.3C]Fig. 3C is a diagram explaining error detection by parity.

[fig.4A]Fig. 4A is a diagram explaining error detection by parity.

[fig.4B]Fig. 4B is a diagram explaining error detection by parity.

[fig.5]Fig. 5 is a diagram illustrating a first configuration example of a parity error detector.

[fig.6]Fig. 6 is a flowchart explaining communication processing in a DDR mode of a master.

[fig.7A]Fig. 7A is a diagram explaining error detection by parity.

[fig.7B]Fig. 7B is a diagram explaining error detection by parity.

[fig.8]Fig. 8 is a diagram illustrating a second configuration example of a parity error detector.

[fig.9]Fig. 9 is a block diagram illustrating a configuration example of an embodiment of a computer to which the present technology is applied.

Description of Embodiments

[0016] Hereinafter, a specific embodiment to which the present technology is applied is described in detail with reference to the drawings.

[0017] <Configuration example of Bus IF>

[0018] Fig. 1 is a block diagram illustrating a configuration example of an embodiment of a bus IF to which the present technology is applied.

[0019] A bus IF 11 illustrated in Fig. 1 is configured by connecting a master 12 with three slaves 13-1 to 13-3 through a data signal line 14-1 and a clock signal line 14-2.

[0020] The master 12 has the control initiative in the bus IF 11, and can communicate with the slaves 13-1 to 13-3 through the data signal line 14-1 and the clock signal line 14-2.

[0021] The slaves 13-1 to 13-3 can communicate with the master 12 through the data signal line 14-1 and the clock signal line 14-2 according to the control by the master 12. Note that, the slaves 13-1 to 13-3 are configured similarly to each other, and are, hereinafter, simply referred to as the slave 13 unless they need to be distinguished, and which is similarly apply to each block included in the slave 13.

- [0022] The data signal line 14-1 and the clock signal line 14-2 are used to transmit a signal between the master 12 and the slave 13. For example, in the bus IF 11, serial data (SDA) is sequentially transmitted bit by bit through the data signal line 14-1, and a serial clock (SCL) having a predetermined frequency is transmitted through the clock signal line 14-2.
- [0023] Furthermore, in the bus IF 11, a plurality of transmission systems having different communication speed is defined in compliance with the I3C standard, and the master 12 can switch these transmission systems. For example, in the bus IF 11, a Standard Data Rate (SDR) mode in which data communication is performed at a normal transfer rate, and a High Data Rate (HDR) mode in which data communication is performed at a transfer rate higher than the SDR mode are defined according to a transfer rate of data. Furthermore, in the HDR mode, three modes of a Double Data Rate (DDR) mode, a Ternary Symbol Pure-Bus (TSP) mode, and a Ternary Symbol Legacy-inclusive-Bus (TSL) mode are defined in the standard. Note that, in the bus IF 11, when communication is started, it is defined that the communication is performed in the SDR mode.
- [0024] The master 12 includes a transmission/reception unit 21, an error detection unit 22, a confirmation signal detection unit 23, and a conflict avoidance unit 24.
- [0025] The transmission/reception unit 21 transmits/receives a signal to/from the slave 13 through the data signal line 14-1 and the clock signal line 14-2. For example, the transmission/reception unit 21 transmits a signal to the slave 13 by driving the data signal line 14-1 (switching electric potential to an H level or an L level) according to the timing of the serial clock transmitted by driving the clock signal line 14-2. Furthermore, the transmission/reception unit 21 receives a signal transmitted from the slave 13 by driving the data signal line 14-1 according to the timing of the serial clock of the clock signal line 14-2 by the slave 13. Note that, the master 12 drives the clock signal line 14-2 at all times. Moreover, the transmission/reception unit 21 adds parity to be described later to data to be transmitted to the slave 13, and performs the transmission.
- [0026] The error detection unit 22 detects an error occurring in the signal received by the transmission/reception unit 21. For example, the error detection unit 22 can detect the error by performing parity check or cyclic redundancy check (CRC) to the signal received by the transmission/reception unit 21, or checking a token issued when a transmission right is changed from the slave 13 to the master 12. Then, when detecting that an error occurs in the signal received by the transmission/reception unit 21, the error detection unit 22 can instruct, for example, the transmission/reception unit 21 to restart the communication with the slave 13.
- [0027] The confirmation signal detection unit 23 confirms whether the slave 13 has

succeeded in receiving a command, data, or the like by detecting an acknowledgement signal (ACK) or a negative acknowledgement signal (NACK) transmitted from the slave 13 which has received the signal transmitted from the transmission/reception unit 21. For example, in the bus IF 11, it is defined that the slave 13 transmits the ACK to the master 12 when the slave 13 has succeeded in receiving a command, data, or the like with no error in the signal. Furthermore, in the bus IF 11, it is defined that the slave 13 transmits the NACK to the master 12 when an error occurs in the signal and the slave 13 has failed to receive a command, data, or the like.

[0028] Accordingly, the confirmation signal detection unit 23 can confirm that the slave 13 has succeeded in receiving a command, data, or the like transmitted from the master 12 when detecting the ACK transmitted from the slave 13. On the other hand, the confirmation signal detection unit 23 can confirm that the slave 13 has failed to receive a command, data, or the like transmitted from the master 12 when detecting the NACK transmitted from the slave 13.

[0029] When, for example, the NACK is detected by the confirmation signal detection unit 23, the conflict avoidance unit 24 instructs the transmission/reception unit 21 to transmit an abort signal for instructing that the communication be interrupted halfway after the predetermined number of bits following the NACK is ignored. The conflict avoidance unit 24 can thereby avoid a conflict from occurring by, for example, the read data transmitted from the slave 13 and an HDR end command transmitted from the master 12. Note that, in order to perform master abort reliably, the master 12 drives the second bit of a preamble to be transmitted/received after the read data at all times.

[0030] Moreover, when a preamble for instructing that a CRC word be transmitted is received by the transmission/reception unit 21 and a token error or a CRC error is detected in the signal received following the preamble by the error detection unit 22, the conflict avoidance unit 24 instructs the transmission/reception unit 21 to transmit an abort signal for instructing that the communication be interrupted halfway after transmitting a clock according to the number of bits corresponding to the difference between the CRC word and the read data following the preamble. The conflict avoidance unit 24 can thereby avoid a conflict from occurring by, for example, the read data transmitted from the slave 13 and an HDR end command transmitted from the master 12.

[0031] The slave 13 includes a transmission/reception unit 31 and an error detection unit 32.

[0032] The transmission/reception unit 31 transmits/receives a signal to/from the master 12 through the data signal line 14-1 and the clock signal line 14-2. For example, the transmission/reception unit 31 receives a signal transmitted from the master 12 by driving the data signal line 14-1 according to the timing of a serial clock of the clock signal line 14-2 by the master 12. Furthermore, the transmission/reception unit 31

transmits a signal to the master 12 by driving the data signal line 14-1 according to the timing of the serial clock of the clock signal line 14-2. Moreover, the transmission/reception unit 31 adds parity to be described later to data to be transmitted to the master 12, and performs the transmission.

[0033] The error detection unit 32 detects, similarly to the error detection unit 22 of the master 12, an error occurring in the signal received by the transmission/reception unit 31. Then, when no error occurs in the signal received by the transmission/reception unit 31, the error detection unit 32 transmits an ACK informing that the reception of a command, data, or the like transmitted by the signal has succeeded from the transmission/reception unit 31 to the master 12. On the other hand, when an error occurs in the signal received by the transmission/reception unit 31, the error detection unit 32 transmits a NACK informing that the reception of a command, data, or the like transmitted by the signal has failed from the transmission/reception unit 31 to the master 12.

[0034] Moreover, when, for example, an error occurs in the signal received by the transmission/reception unit 31 and it is difficult to perform normal communication, the error detection unit 32 ignores all the communication thereafter, stops the response to the master 12, and causes the slave 13 to be in a standby state.

[0035] The bus IF 11 is configured as described above, and the master 12 and the slave 13 can transmit/receive a signal through the data signal line 14-1 and the clock signal line 14-2.

[0036] Incidentally, in the bus IF 11, it is defined that a type of the data to be transmitted next is specified using a 2-bit signal called a preamble in the DDR mode. However, since the error detection by the parity or the CRC for the preamble is not prepared, when an error occurs in the preamble, it is difficult to detect the error.

[0037] For example, when the master 12 transmits a read command to the slave 13, the first bit of the preamble transmitted following the read command is driven by the master 12, and the second bit is driven by the slave 13. For example, the master 12 specifies, by the first bit, that data is to be transmitted following the read command, and the slave 13 can transmit, by the second bit, whether the reception of the read command has succeeded. For example, the slave 13 transmits the ACK indicating that the reception of the read command has succeeded by driving the second bit of the preamble following the read command to 0, and transmits the NACK indicating that the reception of the read command has failed by driving the second bit to 1.

[0038] However, when a 1-bit error in which a 1-bit value is inverted occurs at the second bit of the preamble, it is difficult for the master 12 to detect error occurrence. Accordingly, when the slave 13 transmits the NACK indicating that the reception of the read command has failed and the 1-bit error occurs in the NACK, the master 12 er-

roneously recognizes that the ACK has been transmitted from the slave 13. In this case, although the master 12 becomes a standby state for waiting for the read data to be transmitted from the slave 13, the slave 13 has failed to receive the read command, and does not transmit the read data.

- [0039] Thus, as illustrated in Fig. 2, when the 1-bit error occurs at the second bit of the preamble following the read command, both of the master 12 and the slave 13 become a state for not driving the data signal line 14-1.
- [0040] Here, as described above, the error detection unit 22 of the master 12 can detect, by using a parity bit included in read data transmitted from the slave 13, an error which occurs in the read data. For example, as illustrated in Fig. 3A, the error detection unit 22 can detect whether an error occurs in data on the basis of a parity bit P1 calculated from odd bits of the data and a parity bit P0 calculated from even bits of the data. For example, normally, the parity bit P1 is set so as to take 0 when the logical disjunction of the odd bits of the data is even, and the parity bit P0 is set so as to take 0 when the logical disjunction of the even bits of the data is even.
- [0041] Accordingly, as illustrated in Fig. 3B, when all bits of the read data are 0, both of the parity bits P1 and P0 are to be 0. Thus, when neither the master 12 nor the slave 13 drives the data signal line 14-1 while the data signal line 14-1 is not being kept at the H level (that is, while the data signal line 14-1 is being at the L level), all bits of the read data are to be 0. Accordingly, it is difficult to distinguish this case from the case in which the data all bits of which are actually 0 is transmitted.
- [0042] Similarly, as illustrated in Fig. 3C, when all bits of the read data are 1, both of the parity bits P1 and P0 are to be 1. Thus, when neither the master 12 nor the slave 13 drives the data signal line 14-1 while the data signal line 14-1 is being kept at the H level, all bits of the read data are to be 1. Accordingly, it is difficult to distinguish this case from the case in which the data all bits of which are actually 1 is transmitted.
- [0043] Thus, the error detection unit 22 of the master 12 is set so that the parity bit P1 is to be the even parity which takes 0 when the logical disjunction of the odd bits of the data is even, and the parity bit P0 is to be the odd parity which takes 0 when the logical disjunction of the even bits of the data is odd. Note that, although the configuration of the error detection unit 22 of the master 12 is described below, the error detection unit 32 of the slave 13 is configured similarly. Then, the data is transmitted after parity to be described below is attached by the transmission/reception unit 21 and the transmission/reception unit 31.
- [0044] Thus, when, for example, all bits of the read data are 0 as illustrated in Fig. 4A, the parity bit P1 is to be 0, and the parity bit P0 is to be 1. Similarly, when, for example, all bits of the read data are 1 as illustrated in Fig. 4B, the parity bit P1 is to be 0, and the parity bit P0 is to be 1. Thus, when neither the master 12 nor the slave 13 drives the

data signal line 14-1, the error detection unit 22 can detect that the received data is not correct and an error has occurred from the fact that the parity bits are not matched.

[0045] <First configuration example of Parity error detector>

[0046] The error detection unit 22 of the master 12 includes a parity error detector 41 illustrated in Fig. 5.

[0047] As illustrated in Fig. 5, the parity error detector 41 includes an input terminal 42, XOR gates 43 and 44, a one-bit addition unit 45, and output terminals 46 and 47.

[0048] To the input terminal 42 of the parity error detector 41, serial data supplied through the data signal line 14-1 is input. Then, the input terminal 42 is connected to the XOR gates 43 and 44 so that the odd bits of the serial data are supplied to the XOR gate 43, and the even bits of the serial data are supplied to the XOR gate 44.

[0049] Then, in the parity error detector 41, 1 bit of value 1 is added to the XOR gate 44 from the one-bit addition unit 45. Accordingly, the parity error detector 41 is configured so that the parity bit P1 output from the output terminal 46 is to take 0 when the logical disjunction of the odd bits of the data is even, and the parity bit P0 output from the output terminal 47 is to take 0 when the logical disjunction of the odd bits of the data is odd.

[0050] The parity error detector 41 configured in this manner can detect that the data has not been received correctly when, for example, neither the master 12 nor the slave 13 drives the data signal line 14-1 while the data signal line 14-1 is not being kept at the H level (that is, while the data signal line 14-1 is being at the L level). In other words, although all the received signals are to be 0 in this case, since the parity bit P1 is to be 0 and the parity bit P0 is to be 1, an error can be detected from the fact that the parity bits are not matched (see Fig. 4A).

[0051] Similarly, the parity error detector 41 can detect that the data has not been received correctly when, for example, neither the master 12 nor the slave 13 drives the data signal line 14-1 while the data signal line 14-1 is being kept at the H level. In other words, although all the received signals are to be 1 in this case, since the parity bit P1 is to be 0 and the parity bit P0 is to be 1, an error can be detected from the fact that the parity bits are not matched (see Fig. 4B).

[0052] Furthermore, by assuming the parity bit P1 as the even parity and the parity bit P0 as the odd parity, the parity error detector 41 can detect an error early considering the case in which, for example, the master 12 continues to keep the data signal line 14-1 at the H level. In other words, when the master 12 continues to keep the data signal line 14-1 at the H level, all bits of the data are to be 1, and it is possible to detect an error early from the fact that the parity bit P1 is to be 0.

[0053] <Communication method for performing Parity check normally>

[0054] Fig. 6 is a flowchart explaining communication processing in which the master 12

reads data from the slave 13 in the DDR mode which is one of the HDR mode (DDR Read).

- [0055] In step S11, the master 12 performs processing to switch communication from the SDR mode to the HDR mode. Specifically, in the master 12, the transmission/reception unit 21 drives the data signal line 14-1 and the clock signal line 14-2, and transmits a broadcast command (0x7E+R/W=0) for informing that a command is to be transmitted to all of the slaves 13 included in the bus IF 11 in the SDR mode. Thereafter, in the master 12, when the ACK transmitted from the slave 13 is received to confirm that the reception of the broadcast command has succeeded, the transmission/reception unit 21 transmits a common command code (ENTHDR CCC (0x20)) for entering the HDR mode.
- [0056] In step S12, the transmission/reception unit 21 of the master 12 drives the data signal line 14-1 and the clock signal line 14-2, and transmits the read command.
- [0057] In step S13, the transmission/reception unit 21 detects the value of the second bit of the preamble after the read command is transmitted, and determines whether the slave 13 has transmitted the ACK or the NACK. In other words, when detecting that the second bit of the preamble after the read command is transmitted is 0, the transmission/reception unit 21 determines that the slave 13 has transmitted the ACK. On the other hand, when detecting that the second bit of the preamble after the read command is transmitted is 1, the transmission/reception unit 21 determines that the slave 13 has transmitted the NACK.
- [0058] When the transmission/reception unit 21 determines that the slave 13 has transmitted the ACK in step S13, the processing proceeds to step S14.
- [0059] In step S14, the transmission/reception unit 21 receives the read data transmitted from the slave 13.
- [0060] In step S15, the error detection unit 22 performs the parity check to the data received by the transmission/reception unit 21 in step S14, and determines whether an error occurs in the data. At this time, as described above with reference to Figs. 4A and 4B, the parity bit P1 takes 0 when the logical disjunction of the odd-numbered bits of the data is even, and the parity bit P1 takes 0 when the logical disjunction of the even-numbered bits of the data is odd.
- [0061] When the error detection unit 22 determines that no error occurs in the data, that is, that the data is normal in step S15, the processing proceeds to step S16, and the transmission/reception unit 21 receives the preamble following the data.
- [0062] In step S17, the transmission/reception unit 21 determines whether the preamble received in step S16 specifies the data or the CRC word to be transmitted next.
- [0063] When the transmission/reception unit 21 determines that the data is to be transmitted next in step S17, the processing proceeds to step S18. Then, after the transmission/

reception unit 21 receives the read data, the processing returns back to step S15, and similar processing is repeated thereafter.

[0064] On the other hand, when the transmission/reception unit 21 determines that the CRC word is to be transmitted next in step S17, the processing proceeds to step S19, and the transmission/reception unit 21 receives the CRC word.

[0065] After the processing in step S19, the processing proceeds to step S22. Alternatively, when it is determined that the result of the parity check is error in step S15, the processing proceeds to step S20. Then, after the abort signal for instructing the slave 13 to suspend the processing is transmitted, the processing proceeds to step S22. Furthermore, when it is determined that the NACK has been transmitted in step S13, the processing proceeds to step S21. Then, after a conflict preventing clock period of the predetermined number of bits passes, the transmission/reception unit 21 transmits the abort signal for instructing the slave 13 to suspend the processing, and the processing proceeds to step S22.

[0066] In step S22, the transmission/reception unit 21 transmits an HDR end command, and communication processing in which the master 12 reads the data from the slave 13 in the DDR mode (DDR Read) is thereby terminated.

[0067] As described above, in the bus IF 11, when, for example, the master 12 determines that an ACK is received, it is possible to detect that the received data is not correct by performing the parity check by the error detection unit 22 although the ACK is a 1-bit error of a NACK and the data signal line 14-1 is not being driven. The master 12 thereby accurately determines whether the received data is correct or whether the data signal line 14-1 is not being driven, and can reliably perform communication.

[0068] <Second configuration example of Parity error detector>

[0069] With reference to Figs. 7A, 7B, and 8, a second configuration example of the parity error detector 41 is described.

[0070] The parity error detector 41 described above with reference to Figs. 4A, 4B and 5 is configured so that the parity bit P1 takes 0 when the logical disjunction of the odd bits of the data is even and the parity bit P0 takes 0 when the logical disjunction of the even bits of the data is odd.

[0071] In contrast to the parity error detector 41 in Fig. 5, as illustrated in Figs. 7A, 7B, and 8, a parity error detector 41A is configured so that the parity bit P1 takes 1 when the logical disjunction of the odd bits of the data is even and the parity bit P0 takes 1 when the logical disjunction of the even bits of the data is odd.

[0072] The parity error detector 41A configured in this manner can detect that the data has not been received correctly when, for example, neither the master 12 nor the slave 13 drives the data signal line 14-1 while the data signal line 14-1 is not being kept at the H level (that is, while the data signal line 14-1 is being at the L level). In other words, as

illustrated in Fig. 7A, although all bits of the read data are to be 0 in this case, since the parity bit P1 is to be 1 and the parity bit P0 is to be 0, an error can be detected from the fact that the parity bits are not matched.

- [0073] Similarly, the parity error detector 41A can detect that the data has not been received correctly when, for example, neither the master 12 nor the slave 13 drives the data signal line 14-1 while the data signal line 14-1 is being kept at the H level. In other words, as illustrated in Fig. 7B, although all bits of the read data are to be 1 in this case, since the parity bit P1 is to be 1 and the parity bit P0 is to be 0, an error can be detected from the fact that the parity bits are not matched.
- [0074] Note that, the present technology is not limited to the bus IF 11 in compliance with the I3C standard, and can be applied to the bus IF 11 in compliance with other standards. Furthermore, although the bus IF 11 has been connected with the slaves 13-1 to 13-3 in the configuration example illustrated in Fig. 1, the number of the slaves 13 may be, for example, one, two, or three.
- [0075] Note that, each processing described above with reference to the flowchart is not necessarily performed in the order described as the flowchart in time series, and processing performed in parallel or independently (for example, parallel processing or a processing object) is included. Furthermore, the program may be executed by one CPU or a plurality of CPUs.
- [0076] Furthermore, in the present specification, a system means an entire apparatus including a plurality of apparatuses.
- [0077] Furthermore, the above described series of processing may be performed by hardware or software. When the series of processing is performed by software, a program constituting the software is installed, from a program recording medium recording the program, in a computer embedded in dedicated hardware or a general-purpose personal computer capable of performing various functions by installing various programs.
- [0078] <Hardware configuration example>
- [0079] Fig. 9 is a block diagram illustrating a hardware configuration example of a computer which performs the above described series of processing by a program.
- [0080] In the computer, a central processing unit (CPU) 101, a read-only memory (ROM) 102, a random-access memory (RAM) 103, and an electronically erasable and programmable read only memory (EEPROM) 104 are connected with each other by a bus 105. The bus 105 is further connected with an input/output interface 106, and the input/output interface 106 is connected externally (for example, to the data signal line 14-1 and the clock signal line 14-2 of Fig. 1).
- [0081] In the computer configured in the above manner, the CPU 101 loads and executes the program stored in, for example, the ROM 102 or the EEPROM 104 into the RAM 103

through the bus 105, and the above described series of processing is thereby performed. Furthermore, the program to be executed by the computer (CPU 101) can be not only written in the ROM 102 in advance, but also installed in the EEPROM 104 through the input/output interface 106 or updated externally.

[0082] Note that, the present technology may have the following configurations.

(1)

A communication apparatus includes:

a transmission/reception unit which transmits/receives a signal to/from another communication apparatus; and

an error detection unit which detects error occurrence by performing parity check to data received by the transmission/reception unit,

in which the error detection unit performs error detection assuming one bit of 2-bit parity included in the data as even parity, and the other bit as odd parity.

(2)

The communication apparatus according to (1), in which the error detection unit assumes parity calculated from odd-numbered bits of the data received by the transmission/reception unit as even parity, and parity calculated from even-numbered bits as odd parity.

(3)

The communication apparatus according to (1), in which the error detection unit assumes parity calculated from odd-numbered bits of the data received by the transmission/reception unit as odd parity, and parity calculated from even-numbered bits as even parity.

(4)

The communication apparatus according to any of (1) to (3), in which the transmission/reception unit assumes one bit of 2-bit parity to be added to data to be transmitted to the other communication apparatus as even parity, and the other bit as odd parity.

(5)

The communication apparatus according to any of (1) to (4),
in which the communication apparatus has control initiative in a bus, and
the other communication apparatus performs communication according to control by the communication apparatus.

(6)

The communication apparatus according to any of (1) to (5), in which the communication apparatus performs communication according to control by the other communication apparatus having control initiative in a bus.

(7)

The communication apparatus according to any of (1) to (6) further includes:
an error detection unit which detects error occurrence by receiving, by the transmission/reception unit, a preamble specifying a type of data to be transmitted next and comparing a bit sequence of a signal received following the preamble with a bit sequence to be transmitted in the transmission type specified by the preamble; and
a conflict avoidance unit which instructs, when the error detection unit detects the error occurrence, the transmission/reception unit to transmit an abort signal for instructing that communication be interrupted halfway after a clock according to the predetermined number of bits is transmitted following the preamble.

(8)

The communication apparatus according to any of (1) to (7) further includes:
a confirmation signal detection unit which detects either of an acknowledgement signal or a negative acknowledgement signal to be transmitted from the other communication apparatus which has received the signal transmitted from the transmission/reception unit; and
a conflict avoidance unit which instructs, when the confirmation signal detection unit detects the negative acknowledgement signal, the transmission/reception unit to transmit an abort signal for instructing that communication be interrupted halfway after the predetermined number of bits following the negative acknowledgement signal is ignored.

(9)

The communication apparatus according to any of (1) to (8), in which the transmission/reception unit receives read data read from the other communication apparatus, and drives a second bit of a preamble to be transmitted/received after the read data at all times.

(10)

The communication apparatus according to any of (1) to (9), in which the transmission/reception unit is capable of transmitting/receiving a signal in a standard data rate (SDR) mode in which data communication is performed at a normal transfer rate, and in a high data rate (HDR) mode in which data communication is performed at a higher transfer rate than the SDR mode.

(11)

The communication apparatus according to any of (1) to (10), in which the transmission/reception unit performs communication through two signal lines of a data signal line which sequentially transmits serial data bit by bit and a clock signal line which transmits a serial clock having a predetermined frequency.

(12)

The communication apparatus according to any of (1) to (11), in which the

transmission/reception unit performs communication in compliance with an Improved Inter Integrated Circuit (I3C) standard.

(13)

A communication method includes:

transmitting/receiving a signal to/from another communication apparatus;
detecting error occurrence by performing parity check to received data; and
performing error detection assuming one bit of 2-bit parity included in the data as even parity and the other bit as odd parity.

(14)

A program causes a computer to perform communication processing including:

transmitting/receiving a signal to/from another communication apparatus;
detecting error occurrence by performing parity check to received data; and
performing error detection assuming one bit of 2-bit parity included in the data as even parity and the other bit as odd parity.

(15)

A communication system includes:

a first communication apparatus which has control initiative in a bus; and
a second communication apparatus which performs communication according to control by the first communication apparatus,
in which the first communication apparatus and the second communication apparatus each include
a transmission/reception unit which transmits/receives a signal, and
an error detection unit which detects error occurrence by performing parity check to data received by the transmission/reception unit, and
the error detection unit performs error detection assuming one bit of 2-bit parity included in the data as even parity, and the other bit as odd parity.

[0083] Note that, the present embodiment is not limited to the above described embodiment, and can be variously modified without departing from the scope of the present disclosure.

Reference Signs List

[0084] 11 Bus IF
12 Master
13 Slave
14-1 Data signal line
14-2 Clock signal line
21 Transmission/reception unit
22 Error detection unit

- 23 Confirmation signal detection unit
- 24 Conflict avoidance unit
- 31 Transmission/reception unit
- 32 Error detection unit
- 41 Parity error detector
- 42 Input terminal
- 43, 44 XOR gate
- 45 One-bit addition unit
- 46, 47 Output terminal

Claims

[Claim 1]

A communication device comprising:

transmission and reception circuitry configured to
5 communicate with an external communication device via a
data signal line and a clock signal line, the
communication including transmitting and receiving data
via the data signal line, the data including an expected
parity and a payload, the expected parity including a
10 first expected parity bit and a second expected parity
bit; and

control circuitry configured to perform a parity
check to received data by calculating a first calculated
parity bit and a second calculated parity bit and
15 comparing the first expected parity bit to the first
calculated parity bit and the second expected parity bit
to the second calculated parity bit,

wherein one of the first calculated parity bit or
the second calculated parity bit are calculated based on
20 the data using an XOR function on one of all odd payload
bits or all even payload bits, and the other one of the
first calculated parity bit or the second calculated
parity bit are calculated using an XOR function of the
other of all odd payload bits or all even payload bits
25 adding 1,

wherein, in a case where the control circuitry determines
that an error has occurred, the control circuitry causes
the transmission and reception circuitry to transmit a
negative acknowledgement signal to the external
30 communication device and the control circuitry causes the
transmission and reception circuitry to interrupt the

communication.

[Claim 2]

The communication device according to claim 1,
5 wherein the control circuitry is configured to calculate
the first calculated parity bit using the XOR function of
all odd payload bits, and to calculate the second
calculated parity bit using the XOR function of all even
payload bits adding 1.

10

[Claim 3]

The communication device according to claim 1,
wherein the control circuitry is configured to calculate
the first calculated parity bit using the XOR function of
15 all odd payload bits adding 1, and to calculate the
second calculated parity bit using the XOR function of
all even payload bits.

[Claim 4]

The communication device according to claim 1,
20 wherein the control circuitry is configured to determine
that an error has occurred when the first expected parity
bit does not match the first calculated parity bit,
and/or the second expected parity bit does not match the
second calculated parity bit.

25 [Claim 5]

The communication device according to claim 4,
wherein, in a case where the control circuitry determines
that the error has occurred, the control circuitry causes
the transmission and reception circuitry to restart
30 communication with the external communication device.

[Claim 6]

The communication device according to claim 4,
wherein, in the case where the control circuitry
determines that the error has occurred, the control
circuitry causes the transmission and reception circuitry
5 not to transmit an acknowledgement signal to the external
communication device.

[Claim 7]

The communication device according to claim 1,
wherein the transmission and reception circuitry is
10 configured to communicate in an SDR mode and an HDR mode,
data communication being performed at a first transfer
rate in the SDR mode, the data communication being
performed at a second transfer rate higher than the first
transfer rate in the HDR mode.

15 [Claim 8]

The communication device according to claim 7,
wherein the control circuitry is configured to perform
the parity check to the received data in the HDR mode.

[Claim 9]

20 A communication device comprising:

transmission and reception circuitry configured to
communicate with an external communication device via a
data signal line and a clock signal line, the
communication including transmitting and receiving data
25 via the data signal line, the data including a parity and
a payload, the parity including a first parity bit and a
second parity bit; and

control circuitry configured to calculate the
parity for the data to be transmitted by the transmission
30 and reception circuitry by calculating the first parity
bit and the second parity bit, and to append the parity

to the payload,

wherein one of the first parity bit or the second parity bit are calculated based on the data using an XOR function on one of all odd payload bits or all even payload bits, and the other one of the first parity bit or the second parity bit are calculated using an XOR function of the other of all odd payload bits or all even payload bits adding 1,

wherein the control circuitry is configured to determine that an error has occurred by receiving a negative acknowledgement signal from the external communication device and the control circuitry causes the transmission and reception circuitry to interrupt the communication.
[Claim 10]

The communication device according to claim 9, wherein the control circuitry is configured to calculate the first parity bit using the XOR function of all odd payload bits, and to calculate the second parity bit using the XOR function of all even payload bits adding 1.
[Claim 11]

The communication device according to claim 9, wherein the control circuitry is configured to calculate the first parity bit using the XOR function of all odd payload bits adding 1, and to calculate the second parity bit using the XOR function of all even payload bits.
[Claim 12]

The communication device according to claim 9, wherein the control circuitry is configured to determine whether an error has occurred and, in a case where the control circuitry determines that the error has occurred, the control circuitry causes the transmission and

reception circuitry to restart communication with the external communication device.

[Claim 13]

The communication device according to claim 9,
5 wherein the transmission and reception circuitry is configured to communicate in an SDR mode and an HDR mode, data communication being performed at a first transfer rate in the SDR mode, the data communication being performed at a second transfer rate higher than the first
10 transfer rate in the HDR mode.

[Claim 14]

The communication device according to claim 13, wherein the control circuitry is configured to calculate the parity in the HDR mode.

15 [Claim 15]

A communication system, comprising:

a first communication device, including:

first transmission and reception circuitry configured to communicate via a data signal line and a
20 clock signal line, the communication including transmitting and receiving data via the data signal line, the data including an expected parity and a payload, the expected parity including a first expected parity bit and a second expected parity bit, and

25 first control circuitry configured to calculate the expected parity for the data to be transmitted by the first transmission and reception circuitry, and to add the expected parity to the payload; and

30 a second communication device, including:

second transmission and reception circuitry

configured to communicate with the first communication device via the data signal line and the clock signal line, the communication including transmitting and receiving the data via the data signal line,

5 second control circuitry configured to perform a parity check to the data received by the second transmission and reception circuitry by calculating a first calculated parity bit and a second calculated parity bit and comparing the first expected parity bit to
10 the first calculated parity bit and the second expected parity bit to the second calculated parity bit,

 wherein one of the first expected parity bit or the second expected parity bit are calculated based on the data using an XOR function on one of all odd payload
15 bits or all even payload bits, and the other one of the first expected parity bit or the second expected parity bit are calculated using an XOR function of the other of all odd payload bits or all even payload bits adding 1, wherein the first control circuitry is configured to
20 determine that an error has occurred by receiving a negative acknowledgement signal from the second communication device and the first control circuitry causes the first transmission and reception circuitry to interrupt the communication.

25 and

 wherein one of the first calculated parity bit or the second calculated parity bit are calculated based on the data using an XOR function on one of all odd payload bits or all even payload bits, and the other one of the
30 first calculated parity bit or the second calculated parity bit are calculated using an XOR function of the

other of all odd payload bits or all even payload bits
adding 1,

wherein, in a case where the second control circuitry
determines that the error has occurred, the second

5 control circuitry causes the second transmission and
reception circuitry to transmit the negative
acknowledgement signal to the first communication device
and the second control circuitry causes the second
transmission and reception circuitry to interrupt the
10 communication.

[Claim 16]

The communication system according to claim 15,
wherein the second control circuitry is configured to
calculate the first calculated parity bit using the XOR
15 function of all odd payload bits, and to calculate the
second calculated parity bit using the XOR function of
all even payload bits adding 1.

[Claim 17]

The communication system according to claim 15,
20 wherein the second control circuitry is configured to
calculate the first calculated parity bit using the XOR
function of all odd payload bits adding 1, and to
calculate the second calculated parity bit using the XOR
function of all even payload bits.

25 [Claim 18]

The communication system according to claim 15,
wherein:

the second control circuitry is configured to
determine that an error has occurred when the first
30 expected parity bit does not match the first calculated
parity bit, and/or the second expected parity bit does

not match the second calculated parity bit, and

in a case where the second control circuitry
determines that the error has occurred, the control
circuitry causes the first communication device to
5 restart communication with the second communication
device.