

Digital Signal Processing System

The invention concerns a digital signal processing system for signals coded in segments (batch-bulk).

The packing density (of information) is often subjected to temporal fluctuations with the transmission and/or recording and reproduction of digital signals. This can apply to untreated signals as well as, for example, to such video signals which were treated with a source coder for irrelevancy and redundancy reduction. To design the transmission route or the recording medium for the maximum packing density is technically expensive and uneconomic. With a limitation of the transmission or recording capacity to an average packing density through temporal compression and subsequent expansion, that is by giving the data segments various word lengths depending on the packing density, there is the problem of recognizing the data segments of differing lengths for the blocks after the transmission or recording and to allocate the correct position for the blocks in the output picture. This recognition is then particularly difficult if interference removes the recognition criteria. Moreover, the case can occur that even after the interference has died out, a correct evaluation of the following data segments is not possible.

A similar problem exists if, for example, in a digital video recorder in the operating mode "search", the data can only be read piece by piece in short segments. It is supposed to be possible to reconstruct a picture with sufficient quality from the relatively short data segments read even in the "search" operating mode.

It is the object of the invention to improve a method of digital signal recording and reproduction so that the signal, for example, a picture, can also be decoded with sufficient quality even with reproduction of batch-bulk coded signals at higher speed (search).

This task is solved by the feature given in patent claim 1. Further advantageous developments are described in the sub-claims.

It is known from the Patent Specification DE-A-37 02 490 (EP-A-0276753) to (batch-bulk) record in segments digital signals which have been received in segments and to fill up blocks whose data segments have a smaller than average word length with parts of the data segments of blocks which have a larger than average word length.

The data to be recorded can, for example, consist of coefficients of a DCT transformation. DCT stands for: discrete cosine transformation. For example, for every $n \times m$ picture element block, for example, $n = 8$ and $m = 8$, the D.C. component and one or several important A.C. components and a terminating end-of-block characteristic is firstly recorded for each block. If the data segment length of the coded block is smaller than an average block data segment length then the remaining available space is filled up with A.C. components of a block which requires a larger than average data segment length and, if it fits, filled up with the respective end-of-block characteristic.

If reading errors occur during the reproduction, the starts of the blocks which are located at equal intervals can be found again with this method.

In the "search" operating mode, the reading heads move, for example, with a conventional helical-scan recording system (oblique track), at an angle different from that in the normal reproduction operation over the recorded tracks. Hereby, the tracks can only be batch-bulk read even with a certain reading head follow-up adjustment, for example, by actuators. The question is then which spatial position in the entire decoded signal the particular segment of blocks read should have.

The solution is to insert location information into the signal to be recorded at particular points and to arrange the signal components belonging to these parts in the decoded signal corresponding with the location information. The end-of-block characteristic appears to be most suitable for that purpose. However, if location information is added to every end-of-block characteristic then the amount of data to be recorded can markedly increase.

A further possibility is to combine several blocks, for example, eight, into a larger block, hereinafter called 'superblock', and to provide this at the start or end with an address for the location within the picture. The data rate is only negligibly increased by the recording of an address only for each superblock and the total coder efficiency is increased. The output signal is then assembled from the almost equally spaced (in time) decoded superblocks. The signal is segmented according to the size of the superblocks and can have an unchanged spatial resolution.

A further possibility is to modify the recording sequence of the direct and alternating components of the transformation coefficients known from DE-A-37 02 490.

Firstly, the direct components of all the blocks of one track are recorded at the start of a track, after that the track addresses of the important A.C. components of the associated blocks, then the corresponding A.C. components, following that the track addresses of the less important A.C. components and these A.C. components themselves. Less important A.C. components are, for example, transformation coefficients with small amplitudes. Such a track section of the signal can represent, for example, one segment or two segments, i.e. in the case of a picture signal, a picture can consist of, for example, two segments or only one segment.

First of all, corresponding to an increasing search speed

- D.C. components, important A.C. components and their track addresses
and partly the less important A.C. components and their track addresses
or
 - D.C. components, important A.C. components and their track addresses
or
 - D.C. components
- can be read and decoded.

Correspondingly, a relatively high signal quality with, for example, a full temporal and somewhat reduced spatial resolution, results from a lower search speed; and less high signal quality with, for example, full temporal and significantly reduced spatial resolution, results from a higher search speed. This conforms with the expectation of the viewer.

It is also possible to combine two or several of the above mentioned recording options.

In the following, an exemplary embodiment of the invention is explained with the help of the drawings. These show:

- Fig.1 a block diagram of a video signal processing system,
- Fig.2 tracks of digitally coded video signals on a magnetic tape with helical-scan recording with a scanning path of the video heads in "search" operating mode,
- Fig.3 a known recording method of block-wise coded video signals,
- Fig.4 a superblock recorded on one track of a magnetic tape according

to the recording system of the invention,

Fig.5 the location of such superblocks within the picture,

Fig.6 the locations within the picture of several or all of the blocks respectively of one track in a further recording method according to the invention,

Fig.7 the arrangement of the signal components of this method on one track of a magnetic tape,

Fig.8 a block diagram for a circuit which uses the method according to Fig. 4 and 5,

Fig.9 a block diagram for a circuit which uses the method according to Fig. 6 and 7.

Fig.1 shows a video signal processing system, for example, the video signal section of a digital video recorder, with a circuit 11 which separates the incoming analog CSCC signal into a luminance component and a chrominance component.

The luminance signal is fed to the analog-to-digital converter 12, then, for example, two-dimensionally DCT transformed in a circuit 13, modulated with a channel coding in a circuit 14, stored in a memory 15, for example, a magnetic tape, demodulated in a circuit 16 according to the channel coding, two-dimensionally inversely-DCT transformed, for example, in a circuit 17 and, via a digital-to-analog converter 18, re-assembled with the corresponding chrominance signal from the digital-to-analog converter 181 to form an analog CSCC signal in a circuit 19.

The chrominance signal is processed in the circuits 121 to 181 in a way corresponding with the luminance signal in the respective circuits 12 to 18.

For a digital audio signal processor, for example, the circuits 12 to 18 can be used for a sound channel and the circuits 11,19 and 121 to 181 can be left out.

Fig.2 shows a magnetic tape 20 with recorded helical tracks 21. The general direction of a video head motion on the magnetic tape 20 in the search mode is indicated by the dotted line 22.

The video heads, which are not illustrated here are arranged, for example, on actuators; therefore, they can follow a track 21 piece by piece 23 and read digital data. Between these data segments 23, the video heads jump 24 to the respective next or also a more distant track 21.

Fig.3 shows the arrangement of components of video signals coded in block form on tracks of a magnetic tape. A magnetic tape track section 31 with three blocks of data A, B, C, of equal length with the respective end-of-block characteristic A4, B4, C4 is shown.

Further, a track section 32 with three blocks of data a, b, c, of differing lengths is shown. The respective lengths correspond to the amount of data which, for example, a DCT coder delivers for each of the blocks a, b, c, a1, b1, and c1 are D.C. components, a2, b2 and c2 are important A.C. components, a3, b3 and c3 are less important A.C. components, a4, b4 and c4 are end-of-block markings.

A data recording as on track section 32 leads to an inconsistent block length which hinders the finding of the beginning of the block due to the

appearance of reading errors on reproduction.

A consistent block length as on track section 31 is advantageous. For this purpose, a part of the less important A.C. components c3F from a block c with an amount of data b larger than average is attached to a block a with an amount of data b smaller than average, if possible with the corresponding end-of-block characteristic signal c4, as shown on track section 33. This method is known (DE-A-37 02 490) but is not sufficient to supply in a "search" operating mode, whereby the helical scan tracks 21 of the magnetic tape 20 can only be partly read, information as to where the read and decoded data of the track sections 23 is to be arranged in the output picture of a video recorder, because, for example, only the first block of a complete picture is marked as such.

This information could be given by an addition of appropriate data to the end-of-block characteristics a4, b4, c4. For example, with a picture size of 540 x 576 picture elements with a block size of 8 x 8 picture elements and a coding data rate of about 1 bit/picture element then approximately 77 bit would be necessary instead of approximately 64 bit for every block.

In order to avoid this clear increase in the amount of data, one can - under the condition that the track sections 23 comprise an appropriate number of blocks, combine several, for example, eight, blocks into one "superblock" and only add one address information 401 or 402 to each superblock.

A coder must be controlled in such a way that the data for the last block within the superblock can still be stored in the storage space for this track block. Unoccupied storage space can be filled up with the value "zero".

Fig.4 shows one track of the magnetic tape with such a superblock 40 which consists of the blocks 41 to 48, which corresponds with such blocks as A,

B, C from 31 to 33, and an address 401 or 402.

Fig.5 shows the position of superblocks 51 to 54 in the output picture 50 of a video recorder in search mode. A good spatial resolution can be achieved. The picture is noticeably segmented and has therewith, a reduced temporal resolution.

Fig.6 shows less segmentation by using a further method. For example, only two segments 61 and 62 are present in the entire picture 60. The complete picture 60 can also be formed from one segment 60.

Fig.7 shows the corresponding form of storage of the coding signal components on one track of the magnetic tape.

Firstly, the D.C. components a1, b1 and n1 are written at the start of the storage space for the segment 61, 62 or 60. The addresses a5, b5 to n5 of the important A.C. components a2, b2 to n2 as well as these A.C. components themselves then follow. The addresses a6, b6 to n6 for the less important A.C. components a3, b3 to n3 and these A.C. components themselves then join on. A characteristic 701 or 702 for the location of the segment 61, 62 or 60 within the picture 60 can be inserted at the start or end of this complete track section. Further, non-illustrated corresponding components exist between the b and the n components, for example, between b1 and n1.

A coder must be controlled in such a way that the data n1 to n6 for the last block in the segment (for example, 61, 62 or 60) can still be stored in the storage space provided for the segment. Unoccupied storage space can be filled up with the value "zero".

A segment-free presentation in the search mode is then attained if, for

example, the D.C. components of all blocks of one picture or several pictures are stored in one track of the magnetic tape and the video heads can only scan an appropriate area of the track in the high speed search. It is then possible to decode a picture with reduced spatial resolution even with this high speed search.

Fig.8 shows the block diagram of a coder for the method according to Fig.3 through 5 which contains the circuits 811, 821, 823, 831, 833, 841 and 851, a transmission route or, respectively, a storage medium 86 and the block diagram for a decoder which contains the circuits 812, 822, 824, 830, 832, 842 and 852. The coder can be contained, for example, within the circuit 14 or 141, and the decoder in the circuit 16 or 161.

For example, block-wise DCT coded picture signals from the circuit 811, which contains a quantizer and which codes the signals with variable word lengths, are fed to the input 801 of the coder. Corresponding output signals a1 to a3, b1 to b3, c1 to c3 are fed to the circuit 821, which essentially contains a multiplexer in which they are split up into, for example, D.C. components a1, b1, c1, important A.C. components a2, b2, c2 and less important A.C. components a3, b3, c3.

D.C. components a1, b1, c1 are loaded into a first FIFO memory 831 and A.C. components a2, a3, b2, b3, c2, c3 into a second FIFO memory 833. FIFO stands for: first in - first out.

The state of filling of the first FIFO memory 831 or the state of filling of the second FIFO memory 833 or a combination, for example, the sum, of the two states can be advantageously used as the regulating variable for the quantizer characteristic curve of the circuit 811. The quantizer characteristic curve of the circuit 811 and the size of the FIFO memories 831 or 833 must be designed so that no overflow or underflow appears in the FIFO memories 831 or 833.

In the circuit 823, D.C. and A.C. components a1 to a3, b1 to b3, c1 to c3 from the two FIFO memories 831 and 833 are assembled in a demultiplexer according to the arrangement on the track section 33 and end-of-block markings a4, b4, c4 are added. In circuit 851, several blocks A, B, C are each combined to form one superblock 40 and provided with a superblock address information 401 or 402 and, for example, provided with a channel modulation and an error control.

The control circuit 841 receives signals from the circuit 821 which indicate the respective actual processing of signal components a1 to c1 or a2 to c2 or a3 to c3 or c3F and signals from the input 803 which indicate the location of the current block in the signal before the coding or, respectively, after the decoding. The control circuit 841 supplies the respective read and write addressing for the FIFO memories 831 and 833, controls the circuit 823 with the demultiplexer and the insertion of end-of-block markings a4, b4, c4 and controls the circuit 851 with the combination and addressing 401 or 402 of superblocks 40.

The output signal from circuit 851 is then transmitted 86 or, respectively, stored 86 and upon reproduction fed to the circuit 852 in the decoder. The channel modulation and error correction and the separation of superblock addresses 401 or 402, for example, take place there. Superblock addresses 401 or 402 are available at the output 804 of the decoder.

Direct components a1, b1, c1 or alternating components a2, a3, b2, b3, c2, c3, c3F are separated from the data stream in a circuit 824, which essentially contains a multiplexer and an end-of-block marking decoder, and loaded into a third FIFO memory 830 or a fourth FIFO memory 832.

From there, the corresponding signal components are arranged, in a form like that shown on track section 32, within a circuit 822, which essentially

contains a demultiplexer, and decoded corresponding to their variable word length in the circuit 812. Signal blocks with constant word length and their associated addresses 804 within the picture are then available again at the output 802 of the decoder, superblock-wise jumping in the "search" operating mode.

The control circuit 842 receives, for example, block addresses from circuit 852 and supplies therewith, the read and write addressing for direct components a1, b1, c1 or alternating components a2, a3, b2, b3, c2, c3, c3F in the FIFO memories 830 or 832 and, apart from that, controls the multiplexer in circuit 824 and the demultiplexer in circuit 822.

Fig.9 shows, for the method according to Fig.3, 6 and 7, the block diagram of a coder which contains the circuits 911, 921, 923, 931, 933, 935, 937, 939, 941 and 951, a transmission route or, respectively, a storage medium 96 and the block diagram of a decoder which contains the circuits 912, 922, 924, 930, 932, 934, 936, 938, 942 and 952. The coder can be contained, for example, within the circuit 14 or 141 and the decoder within the circuit 16 or 161.

For example, blockwise DCT coded picture signals from the circuit 911, which contains a quantizer and which codes the signals with variable word lengths, are fed to the input 901 of the coder. Corresponding output signals a1 to a3, b1 to b3, c1 to c3 are fed to the circuit 821, which essentially contains a multiplexer in which they are split up into, for example, D.C. components a1, b1, c1, important A.C. components a2, b2, c2 and less important A.C. components a3, b3, c3. D.C. components a1, b1 to n1 of a segment, for example, 61, or picture 60 are loaded into a first FIFO memory 931, important A.C. components a2, b2 to n2 of the segment or picture into a second FIFO memory 933 and less important A.C. components a3, b3 to n3 of the segment or picture into a third FIFO memory 935. The addresses a5, b5 to n5 of the

important A.C. components a_2, b_2 to n_2 of the segment or picture are loaded into a fourth FIFO memory 937 and the addresses a_6, b_6 to n_6 of the less important A.C. components a_3, b_3 to n_3 of the segment or picture into a fifth FIFO memory 939.

The state of filling of a FIFO memory or, respectively, the state of filling of several FIFO memories 931, 933, 935, 937, 939 or, respectively, the sum of the states can be advantageously used as the regulating variable for the quantizer characteristic curve of the circuit 911. The quantizer characteristic curve of the circuit 911 and the size of the FIFO memories 931, 933, 935, 937, 939 must be proportioned so that no overflow or underflow appears in the FIFO memories 931, 933, 935, 937, 939.

D.C. and A.C. components a_1, b_1 to n_1, a_2, b_2 to n_2, a_3, b_3 to n_3 and their addresses a_5, b_5 to n_5, a_6, b_6 to n_6 from the five FIFO memories 931, 933, 935, 937, 939 are put together in a demultiplexer in the circuit 923 according to the arrangement on the track section in Fig.7. In circuit 951, segments 61, 62 are marked with their addresses 701 or 702 within the picture 60 or, respectively, pictures 60 are marked with their picture number 701 or 702 and, for example, provided with a channel modulation and an error control.

The control circuit 941 receives signals from the circuit 921 which indicate the respective actual processing of signal components a_1, b_1 to n_1, a_2, b_2 to n_2 or a_3, b_3 to n_3 and signals from the input 903 which indicate the location of the current block in the signal before the coding or, respectively, after the decoding. The control circuit 941 supplies the respective read and write addressing for the FIFO memories 931, 933, 935, 937, 939, controls the circuit 923 with the demultiplexer and controls the circuit 951 with the addressing 701 or 702 of segments 61, 62 or, respectively, with the allocation of picture numbers 701 or 702 of pictures 60.

The output signal from the circuit 951 is then transmitted 96 or, respectively, stored 96 and upon reproduction fed to the circuit 952 in the decoder. The channel demodulation and error correction and the separation of segment addresses or picture numbers 701, 702, for example, take place there. The segment addresses or the picture numbers 701, 702 are available at the output 904 of the decoder.

D.C. components a_1, b_1 to n_1 , important A.C. components a_2, b_2 to n_2 and their addresses a_5, b_5 to n_5 , less important A.C. components a_3, b_3 to n_3 and their addresses a_6, b_6 to n_6 are separated from the data stream in a circuit 924, which essentially contains a multiplexer and an address decoder, and loaded into a sixth 930, seventh 932, ninth 936, eighth 934 or, respectively, tenth 938 FIFO memory.

From there, the corresponding signal components are arranged, in a form like that shown on track section 32, within a circuit 922, which essentially contains a demultiplexer, and decoded corresponding to their variable word length in the circuit 912. Signal blocks with constant word length and their associated addresses 904 within the picture or picture number 904 are then available again at the output 902 of the decoder, in the "search" operation mode in a segment-type or, respectively, picture-type form with less important A.C. components a_3, b_3 to n_3 , for example, filled up with zeros before the decoding.

The control circuit 942 receives, for example, block addresses from circuit 952 and supplied therewith, the read and write addresses for D.C. components a_1, b_1 to n_1 or important A.C. components a_2, b_2 to n_2 or less important A.C. components a_3, b_3 to n_3 and their addressing in the FIFO memories 930, 932, 934, 936, 938 and, apart from that, controls the multiplexer in circuit 924 and the demultiplexer in circuit 922.

If, as in Fig. 8 or 9, a device, for example, a video recorder, contains a coder and a decoder, circuits of the coder, for example, the FIFO memories 831 and 833 or, respectively, 931, 933, 935, 937, 939, can be advantageously used by the decoder and thereby, corresponding circuits of the decoder, for example, the FIFO memories 830 and 832 or 930, 932, 934, 936, 938, can be left out.

Claims

1. Signal processing system for digital signals which are coded or decoded in segments (batch-bulk), in particular picture or sound signals, whereby the coded signals have a variable word length within the segments (a,b,c in 32) which is independent on the packing density of the signals and these coded signals received in segments are firstly allocated to blocks (A,B,C in 31) of constant word length, following that the blocks (a in 32), whose segments have a smaller word length than was predetermined by these blocks (A,B,C in 31), are filled up with components (c3F in 33) from segments (c3 in 32), which have a larger word length than was given by the blocks (A,B,C in 31) and that on decoding, the segments (32) are re-assembled in their original variable word lengths from the blocks of constant word length (33), characterised in that several successive blocks (33) of a constant word length are respectively combined into a superblock (40) and this is provided with information (401 or 402) which indicates the respective location (51 to 54) of the superblock (40) to be decoded within the digital signal before the segment-type coding, the sum of the variable lengths of the segments within every single superblock (40) is smaller than or equal to the sum of the constant word lengths (41 to 48) of the combined blocks of the respective superblock (40).

2. System according to claim 1, characterised in that the information (401 or 402) about the location of every single superblock (40) is respectively arranged in the digital signal before or after the coded data of every single superblock (40).

3. System according to claim 2, characterised in that the level of occupancy of a memory or several memories (831,833), which temporarily store(s) the coded segments (33) in the signal processing system, and/or the corresponding level within the storage area for every

single superblock (40) controls a quantizer characteristic curve with the coding (811) in the coding section of the signal processing system.

4. System according to claim 2 or 3, characterised in that the decoding is designed so that stored (86) superblocks (40) are decoded from a storage medium (86) at essentially equal temporal intervals with an increased reading speed and, by means of the location information (401 or 402), can be reproduced at corresponding points of the decoded signal and that thereby, a segmented presentation of the digital signal, as it would be formed with decoding using a not increased reading speed, is rendered possible with reduced temporal resolution.

5. Signal processing system for digital signals which are coded or decoded in segments, in particular picture or sound signals, whereby the coded signals have a variable word length within the segments (32) which is dependent on the packing density of the signals and consist of a combination of several different types of components, for example, D.C. components (a1, b1 to n1 in Fig.7), important A.C. components (a2, b2 to n2 in Fig.7) and less important A.C. components (a3, b3 to n3 in Fig.7), which in each case form a data segment belonging to one of the types, characterised in that a successive number of digital signals is respectively combined into one segment (61,62) whereby, in the case of a picture signal, one segment (60) can comprise, for example, a complete picture (60) and every segment (61,62 or 60) contains the combination of the different types of components (a1, b1 to n1, a2, b2 to n2, a3, b3 to n3 in Fig.7), within every single segment (61, 62 or 60), the data sections of corresponding types of components are combined (a1, b1 to n1 or a2, b2 to n2 or a3, b3 to n3 in Fig.7), for all types (a2, b2 to n2, a3, b3 to n3 in Fig.7) of components, which follow a first type (a1, b1 to n1 in Fig.7), within every single segment



(61,62 or 60), the respective addresses of the data sections of one type (a5, b5 to n5 or a6, b6 to n6 in Fig.7) are transmitted or stored or evaluated in a combined way always before the data segments of this type, each segment (61,62 or 60) is provided with information (701 or 702) which indicates the respective location of the segments (61,62 or 60) to be decoded within the digital signal before the segment-type coding.

6. System according to claim 5, characterised in that the information (701 or 702) concerning the location of every single segment (61,62 or 60) is arranged in the digital signal respectively before or after the coded data of every single segment (61,62 or 60).

7. System according to claim 6, characterised in that the level of occupancy of a memory or several memories (931,933,935,937,939) which temporarily store(s) the data segments of the various types of components in the signal processing system (Fig.7) and/or the corresponding level within the storage area for each segment (61,62 or 60) controls a quantizer characteristic curve with the coding (911) in the coder section of the signal processing system.

8. System according to claim 6 or 7, characterised in that the decoding is designed in such a way that stored (96) segments (61,62 or 60) are decoded from a storage medium (96) at essentially equal temporal intervals with an increased reading speed and, by means of the location information (701 or 702), can be reproduced at corresponding points of the decoded signal, and that a reduced number of data segments of types of components (for example, a1,b1 to n1,a2,b2 to n2 in Fig.7) with corresponding addresses (for example, a5,b5 to n5 in Fig.7) can be reproduced from the storage medium (96) with an increased reading speed, and a further reduced number of data segments of types of components (for



example, a1,b1 to n1 in Fig.7) with or without corresponding addresses can be reproduced from the storage medium (96) with an even higher reading speed in such a way that thereby, a little-segmented or unsegmented presentation of the digital signal, as it would be formed by decoding with a not increased speed, is rendered possible with a reduced spatial resolution.

9. System according to one or more of the preceding claims, characterised in that the information (401,402 or 701,702) concerning the position (51 to 54 or 61,62 or 60) of the superblocks or, respectively, the segments are safeguarded in the signal by an error protection against errors in transmission, recording or evaluation.

10. Coder circuit for a system according to one or more of claims 1 to 4, provided with a coding circuit (811) with variable word length and controllable quantization characteristic curve, with a following multiplexer (821), which loads D.C. components into a first FIFO memory (831) and A.C. components into a second FIFO memory (833) and corresponding information therefore into a control circuit (841) which addresses the FIFO memories (831,833) and additionally receives information (803) concerning the position of superblocks (40) in the whole signal, whereby the levels of occupancy of the FIFO memories (831,832) or, respectively the superblocks (40) in the FIFO memories (831,832) can control the quantization characteristic curve, with a demultiplexer (823) which, controlled by the control circuit (841), puts together the D.C. and A.C. components from the FIFO memories (831,832) into blocks of equal word length, with a subsequent circuit (851) which, controlled by the control circuit (841), combines always several of such blocks (41 to 48) in a superblock (40), provides them with an address (401 or 402) and adds an error control or a channel modulation.

11. Decoder circuits for a system according to one or



more of claims 1 to 4, provided with a circuit (852) which carries out a channel modulation or an error control and decodes information concerning the position of signal components in the whole signal (804) and feeds information concerning the position of the D.C. and A.C. components allocated in the demultiplexer (823) of the coder section to a control circuit (42), with a subsequent multiplexer (824) which, controlled by the control circuit (842), writes the D.C components into a third FIFO memory (830) and the A.C. components into a fourth FIFO memory (832) whereby the addressing of the FIFO memories (830,832) is supplied by the control circuit (842), with a demultiplexer (822) downstream from the FIFO memories (830,832) which again arranges D.C. and A.C. components at the output of the coding circuit (811) in the coding section corresponding to the original location and which is controlled by the control circuit (842), with a downstream decoder circuit (812) which generates signals with constant word length from signals with variable word length, wherein the decoder circuit is designed so that stored (86) superblocks (40) are decoded from a storage medium (86) at essentially equal temporal intervals with an increased reading speed and, by means of the location information (804), can be reproduced at corresponding points of the decoded signal in such a way that thereby, a segmented presentation of the digital signals, as they would be formed with decoding using a not increased reading speed, is rendered possible with reduced temporal resolution.

12. Coder circuit for a system according to one or more of claims 5 to 8, provided with a coding circuit (911) with variable word length and controllable quantizer characteristic curve, with a downstream multiplexer (921) which loads, segment-wise (61,62 or 60), D.C. components (a1,b1 to n1 in Fig.7) into a first FIFO memory (931), important A.C. components (a2,b2 to n2 in Fig.7) into a second FIFO memory (933) and less important A.C. components (a3,b3 to n3 in Fig.7) into a



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third FIFO memory (935) and information corresponding to that into a control circuit (941) which addresses the FIFO memories (931,933,935,937,939) and additionally receives information (903) concerning the location of the segments (61,62 or 60) in the total signal, wherein the control circuit (941) writes the respective addresses of the important (a5,b5 to n5 in Fig.7) or less important (a6,b6 to n6 in Fig.7) A.C. components into a fourth FIFO memory (937) or fifth FIFO memory (939) and the levels of occupancy of the FIFO memories (931,933,935,937,939) can control the quantizer characteristic curve, with a demultiplexer (923), which, controlled by the control circuit (941), forms respectively, from the contents of the FIFO memories (931,933,935,937,939), segments (61,62 or 60) of the signal with a new sequence of components, specifically in the sequence: D.C. components (a1,b1 to n1 in Fig.7), addresses for important A.C. components (a5,b5 to n5 in Fig.7), corresponding importantly A.C. components (a2,b2 to n2 in Fig.7), addresses for less important A.C. components (a6,b6 to n6 in Fig.7) and corresponding less important A.C. components (a3,b3 to n3 in Fig.7), with a downstream circuit (951) which, controlled by the control circuit (941), provides a segment (61,62 or 60) each with an address (701 or 702) and adds on an error control or a channel modulation.

13. Decoder circuit for a system according to one or more of claims 5 to 8, provided with a circuit (952) which carries out a channel modulation or an error correction and decodes (904) information concerning the location of segments in the total signal and feeds information concerning the position of the D.C. important A.C. and less important A.C. components or the addresses of the important and less important A.C. components allocated in the demultiplexer (823) of the coder section to a control circuit (942), with a subsequent multiplexer (924) which, controlled by the control circuit (942), writes the D.C. components (a1,b1 to n1



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in Fig.7) into a sixth FIFO memory (930), the important A.C. components (a2,b2 to n2 in Fig.7) into a seventh FIFO memory (932), the less important A.C. components (a3,b3 to n3 in Fig.7) into an eighth FIFO memory (934), the addresses (a5,b5 to n5 in Fig.7) of the important A.C. components into a ninth FIFO memory (936) and the addresses (a6,b6 to n6 in Fig.7) of the less important A.C. components into a tenth FIFO memory (938), wherein the respective addressing of the FIFO memories (930,932,934,936,938) is supplied by the control circuit (942), with a demultiplexer (922) downstream from the FIFO memories (930,932,934,936,938) which again arranges the D.C. important A.C. and less important A.C. components at the output of the coding circuit (911) in the coder section corresponding to the original location and which is controlled by the control circuit (942), with a downstream decoding circuit (912) which generates signals with constant word length from signals with variable word length, wherein the decoder circuit is designed so that stored (96) segments (61,62 or 60) are decoded from the storage medium (96) at essentially equal temporal intervals at an increased reading speed and, by means of the location information (904), can be reproduced at corresponding points of the decoded signal and, with slightly increased reading speed, the D.C. components (a1,b1 to n1 in Fig.7), the addresses (a5,b5 to n5 in Fig.7), of the important A.C. components and the important A.C. components (a2,b2 to n2 in Fig.7) are decoded from the storage medium (96) with the less important A.C. components (a3,b3 to n3 in Fig.7) set to zero and, in case of a significantly increased reading speed, only the D.C. components (a1,b1 to n1 in Fig.7) are decoded from the storage medium (96) with the important and less important A.C. components (a2,b2 to n2 and a3,b3 to n3 in Fig.7) set to zero and that thereby, a coarser presentation of the digital signals, as they would be decoded on reproduction with a not increased reading speed, is rendered possible.

