WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor structure, comprising:

etching a semiconductor substrate to form a plurality trenches and define a plurality of fin active regions;

filling in the plurality of trenches with a dielectric material to form shallow trench isolation (STI) features;

recessing a first subset of the STI features in a first region by a first dimension;

recessing a second subset of the STI features in a second region by a second dimension less than the first dimension; and

forming a conductive feature on the STI features and the fin active regions, wherein the conductive feature covers the first subset of the STI features,

wherein recessing the first subset of the STI features in the first region by the first dimension, and recessing the second subset of the STI features in the second region comprise:

forming a patterned resist layer on the semiconductor substrate, wherein the patterned resist layer has openings exposing the first region and covering the second region;

performing a first STI etch to the first subset of the STI features in the first region through openings of the patterned resist layer;

removing the patterned resist layer; and

performing a second STI etch to the first subset of the STI features in the first region and the second subset of the STI features in the second region, resulting in the first subset of the STI features being recessed from the second subset of the STI features.

2. The method of claim 1, further comprising performing a well implantation to the semiconductor substrate after the performing the first STI etch and before the performing the second STI etch.

3. The method of claim 2, further comprising:

depositing a hard mask layer on the semiconductor substrate;

patterning the hard mask layer using a lithography process, wherein the etching the semiconductor substrate to form the plurality trenches and define the plurality of fin active

regions includes etching the semiconductor substrate through openings of the hard mask layer; and

removing the hard mask layer after the first STI etch and before the performing the well implantation.

4. The method of claim 1, further comprising:

forming a first transistor in the first region, wherein the first transistor comprises a first gate stack having a first one of the dielectric features and a first one of the conductive features overlying the first one of the dielectric features; and

forming a second transistor in the second region, wherein the second transistor comprises a second gate stack having a second one of the dielectric features and a second one of the conductive features overlying the second one of the dielectric features.

5. The method of claim 1, further comprising coupling the fin active regions, the first subset of the STI features, and the conductive features covering the first subset of the fin active regions to thereby form a capacitor.

6. The method of claim 1, further comprising coupling the fin active regions, the second subset of the STI features, and the conductive features to thereby form a field effect transistor.

7. The method of claim 1, wherein:

defining the fin active regions comprises orienting the fin active regions in a first direction; and

forming the conductive feature comprises orienting the conductive feature in a second direction perpendicular to the first direction.

8. A method for fabricating a semiconductor structure, comprising:

forming a semiconductor substrate having a first region and a second region;

forming a shallow trench isolation (STI) feature in the semiconductor substrate, wherein the STI feature is formed to comprise a first portion disposed in the first region and having a first thickness T1 and a second portion disposed in the second region and

having a second thickness T2 greater than the first thickness T1, the first portion of the STI feature being recessed from the second portion of the STI feature;

forming a plurality of fin active regions on the semiconductor substrate;

forming a plurality of conductive features on the fin active regions and the STI feature, wherein one of the conductive features covers the first portion of the STI feature in the first region and a portion of the second portion of the STI feature in the second region;

wherein the plurality of conductive features are formed to comprise:

a first conductive feature disposed in the first region and having a first width W1; and

a second conductive feature disposed in the second region and having a second width W2 less than the first width W1; and

forming a plurality of dielectric features underlying the conductive features and separating the conductive feature from the fin active regions, wherein the plurality of dielectric features comprise:

a first dielectric feature disposed in the first region, underlying the first conductive feature, and having a first dielectric material; and

a second dielectric feature disposed in the second region, underlying the second conductive feature, and having a second dielectric material different from the first dielectric material.

9. The method of claim 8, further comprising:

configuring the first conductive feature, the first dielectric feature, and a first subset of the fin active regions to form a capacitor; and

configuring the second conductive feature, the second dielectric feature, and a second subset of the fin active regions to form a fin field effect transistor.

10. The method of claim 8, further comprising:

forming the first portion of the first region to have a plurality of sides; and

forming the second portion of the second region to surround the first portion on each of the sides.

11. A method for fabricating a semiconductor structure, comprising:

forming a semiconductor substrate having a first region and a second region;

forming a single fin active region on the semiconductor substrate that extends in the first and second regions;

forming a shallow trench isolation (STI) feature in the semiconductor substrate and adjacent the fin active region, wherein the STI feature is formed to comprise:

a first portion disposed in the first region and a second portion disposed in the second region, and

the first portion of the STI feature has a first top surface and the second portion of the STI feature has a second top surface higher than the first top surface;

forming a first conductive feature on the fin active region and the STI feature, wherein the first conductive feature is disposed in the first region and covers the first portion of the STI feature, the first conductive feature further comprising a first width;

forming a second conductive feature on the fin active region and the STI feature, wherein the second conductive feature is disposed in the second region, the second conductive feature further comprising a second width less than the first width;

forming a first dielectric feature aligned with the first conductive feature and underlying the first conductive feature, the first dielectric feature further comprising a first dielectric material;

forming a second dielectric feature aligned with the second conductive feature and underlying the second conductive feature, the second dielectric feature further comprising a second dielectric material different from the first dielectric material;

wherein the fin active region, the first dielectric feature, and the first conductive feature are configured and coupled to form a capacitor; and

wherein the fin active region, the second dielectric feature, and the second conductive feature are configured and coupled to form a field effect transistor.

12. The method of claim 11, wherein:

forming the fin active region comprises orienting the fin active region in a first direction; and

forming the first and second conductive features comprises orienting the first and second conductive features in a second direction perpendicular to the first direction.

13. The method of claim 11, further comprising forming the capacitor as a de-coupling capacitor.

14. A method for fabricating a semiconductor structure, comprising:

forming a semiconductor substrate having a first region and a second region;

forming a shallow trench isolation (STI) feature in the semiconductor substrate, wherein the STI feature includes a first portion disposed in the first region and having a first thickness T1 and a second portion disposed in the second region and having a second thickness T2 greater than the first thickness T1, the first portion of the STI feature being recessed from the second portion of the STI feature;

forming a plurality of fin active regions on the semiconductor substrate;

forming a plurality of conductive features on the fin active regions and the STI feature, wherein one of the conductive features covers the first portion of the STI feature in the first region and a portion of the second portion of the STI feature in the second region;

forming a plurality of dielectric features underlying the conductive features and separating the conductive feature from the fin active regions;

forming a first transistor in the first region, wherein the first transistor comprises a first gate stack having a first one of the dielectric features and a first one of the conductive features overlying the first one of the dielectric features; and

forming a second transistor in the second region, wherein the second transistor comprises a second gate stack having a second one of the dielectric features and a second one of the conductive features overlying the second one of the dielectric features,

wherein the first one of the dielectric features has a first dielectric thickness, and the second one of the dielectric features has a second dielectric thickness different from the first dielectric thickness.

15. The method of claim 14, further comprising recessing the first portion of the STI feature is from the second portion of the STI feature such that a top surface of the first portion is lower than a top surface of the second portion by (T2-T1).

16. The method of claim 14, further comprising forming a capacitor in the first region, wherein the capacitor includes one of the fin active regions, one of the conductive

features, and one of the dielectric layer separating the one of the conductive features from the one of the fin active regions.

17. The method of claim 16, further comprising forming the capacitor as a de-coupling capacitor and the second transistor is a field effect transistor.

18. The method of claim 14, wherein forming the plurality of conductive features comprises:

forming a first conductive feature in the first region and having a first width W1; and

forming a second conductive feature in the second region and having a second width W2 less than the first width W1.

19. The method of claim 14, wherein:

forming the plurality of fin active regions comprises orienting the fin active regions in a first direction; and

forming the plurality of conductive features comprises orienting the conductive features in a second direction perpendicular to the first direction.