FOUNDRY-AGNOSTIC POST-PROCESSING METHOD FOR A WAFER

BACKGROUND

[0001] The present disclosure relates to foundry-agnostic post-processing methods for wafers and, more particularly, to foundry-agnostic post-processing methods for wafers where alternative material substrates are bonded to wafers to create customized devices with improved performance.

[0002] In electronics, a wafer is a thin slice of semiconductor material that is used for the fabrication of integrated circuits and in photovoltaics. The wafer serves as the substrate for microelectronic devices built in and over the wafer and undergoes many microfabrication process steps such as doping or ion implantation, etching, deposition of various materials and photolithographic patterning. At a final stage, individual microcircuits formed on the wafer may be separated from one another by a dicing process and packaged for shipping.

[0003] Wafers are frequently formed of silicon (Si) or silicon germanium (SiGe) and may include low resistivity (LRS) substrates, high resistivity (HRS) substrates and silicon-on-insulator (SOI) substrates with a buried oxide (BOX) layer disposed on an HRS substrate. Over time, it has been demonstrated that the higher resistivity substrates can in some cases improve certain aspects of device performance by reducing parasitic substrate losses, such as collector-substrate capacitance. However, foundries where wafers are typically processed do not have the capacity for providing wafers with substrates that are more resistive than the LRS, HRS and SOI substrates.

SUMMARY

[0004] According to a first aspect of the present invention, there is provided a foundry-agnostic post-processing method for a wafer having an active surface, a substrate, and an intermediate layer interposed between the active surface and the substrate, the foundry-agnostic post-processing method including: producing an output yield at a wafer processing foundry with the production of each wafer in the output yield comprising forming the intermediate layer thereof to include doped wells, isolated doped substrate regions and shallow trench isolation regions or to be defined between trench isolation regions; removing one of the wafers from the output yield of the wafer processing foundry; removing wafers that are similar to the removed one of the wafers from respective output yields of a plurality of wafer processing foundries; compiling the removed one of the wafers and the removed wafers that are similar to the removed one of the wafers into a wafer set in a post-processing facility; thinning the substrate of each wafer of the wafer set to the intermediate layer to expose a new surface; and bonding the new surface to an alternate material substrate which provides for enhanced device performance as compared to the substrate, wherein the thinning comprises: recognizing an existence of a via in the intermediate layer of each wafer of the wafer set; executing the thinning of the substrate at locations remote from a location of the via; and adjusting the thinning of the substrate at the location of the via in order to avoid the execution of the thinning at the location of the via, wherein: the adjusting is conducted such that the thinning forms an irregular topology with a bump of material of the substrate, which is substantially wider than the via and which protrudes from a plane of the new surface at the location of the via, and the bonding of the new surface to an alternate material substrate comprises absorbing the irregular topology in the alternate material substrate such that an outward topology of the alternate material substrate is flat at a location corresponding to the location of the via.

[0005] According to a second aspect of the present invention, there is provided a foundry-agnostic post-processing method for a wafer having an active surface, a silicon handle, and a buried oxide (BOX) layer interposed between the active surface and the silicon handle, the foundry-agnostic post-processing method including: producing an output yield at a wafer

processing foundry with the production of each wafer in the output yield comprising forming the BOX layer to include doped wells, isolated doped substrate regions and shallow trench isolation regions; removing one of the wafers from the output yield of the wafer processing foundry; removing wafers that are similar to the removed one of the wafers from respective output yields of a plurality of wafer processing foundries; compiling the removed one of the wafers and the removed wafers that are similar to the removed one of the wafers into a wafer set in a post-processing facility; thinning the silicon handle of each wafer of the wafer set to the BOX layer to expose a new surface; and bonding the new surface to an alternate material substrate which provides for enhanced device performance as compared to the silicon handle, wherein the thinning comprises: recognizing an existence of a via in the BOX layer of each wafer of the wafer set; executing the thinning of the silicon handle at locations remote from a location of the via; and adjusting the thinning of the silicon handle at the location of the via in order to avoid the execution of the thinning at the location of the via, wherein: the adjusting is conducted such that the thinning forms an irregular topology with a bump of material of the silicon handle, which is substantially wider than the via and which protrudes from a plane of the new surface at the location of the via, and the bonding of the new surface to an alternate material substrate comprises absorbing the irregular topology in the alternate material substrate such that an outward topology of the alternate material substrate is flat at a location corresponding to the location of the via.

[0006] Disclosed herein is a foundry-agnostic post-processing method for a wafer. The wafer includes an active surface, a high resistivity substrate (HRES SX) and a near sub-collector (NS) interposed between the active surface and the HRES SX. The method includes removing the wafer from an output yield of a wafer processing foundry, thinning the HRES SX to the NS or within microns of the NS to expose a new surface and bonding the new surface to an alternate material substrate which provides for enhanced device performance as compared to the HRES SX.

[0007] Additional features and advantages are realized through the techniques of the present invention. Other embodiments and aspects of the invention are described in detail herein and are considered a part of the claimed invention. For a better understanding of the invention with the advantages and the features, refer to the description and to the drawings.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0008] For a more complete understanding of this disclosure, reference is now made to the following brief description, taken in connection with the accompanying drawings and detailed description, wherein like reference numerals represent like parts:

[0009] FIG. 1 is a schematic illustration of wafer removal from an output yield of a wafer processing foundry;

[0010] FIG. 2 is an enlarged side view of an SOI wafer in accordance with embodiments;

[0011] FIG. 3 is an enlarged side view of the SOI wafer of FIG. 2 with its silicon handle removed;

[0012] FIG. 4 is an enlarged side view of an SOI wafer with a fused silica substrate;

[0013] FIG. 5 is an enlarged side view of a wafer with an HRES SX in accordance with embodiments;

[0014] FIG. 6 is an enlarged side view of the wafer of FIG. 5 with its HRES SX removed;

[0015] FIG. 7 is an enlarged side view of a wafer with a fused silica substrate;

[0016] FIG. 8 is a schematic illustration of a grinding process for a wafer;

[0017] FIG. 9 is a schematic illustration of a chemical mechanical polishing process for the wafer of FIG. 8;

CLAIMS

1. A foundry-agnostic post-processing method for a wafer having an active surface, a substrate, and an intermediate layer interposed between the active surface and the substrate, the foundry-agnostic post-processing method comprising:

producing an output yield at a wafer processing foundry with the production of each wafer in the output yield comprising forming the intermediate layer thereof to include doped wells, isolated doped substrate regions and shallow trench isolation regions or to be defined between trench isolation regions;

removing one of the wafers from the output yield of the wafer processing foundry;

removing wafers that are similar to the removed one of the wafers from respective output yields of a plurality of wafer processing foundries;

compiling the removed one of the wafers and the removed wafers that are similar to the removed one of the wafers into a wafer set in a post-processing facility;

thinning the substrate of each wafer of the wafer set to the intermediate layer to expose a new surface; and

bonding the new surface to an alternate material substrate which provides for enhanced device performance as compared to the substrate,

wherein the thinning comprises:

recognizing an existence of a via in the intermediate layer of each wafer of the wafer set;

executing the thinning of the substrate at locations remote from a location of the via; and

adjusting the thinning of the substrate at the location of the via in order to avoid the execution of the thinning at the location of the via, wherein:

the adjusting is conducted such that the thinning forms an irregular topology with a bump of material of the substrate, which is substantially wider than the via and which protrudes from a plane of the new surface at the location of the via, and

the bonding of the new surface to an alternate material substrate comprises absorbing the irregular topology in the alternate material substrate such that an outward topology of the alternate material substrate is flat at a location corresponding to the location of the via.

2. The foundry-agnostic post-processing method according to claim 1, wherein at least one of the active surface and the substrate comprises at least one of silicon (Si) and silicon germanium (SiGe) and wherein the alternate material substrate comprises a high resistivity material.

3. The foundry-agnostic post-processing method according to claim 1, wherein the alternate material substrate comprises at least one of glass and fused silica.

4. The foundry-agnostic post-processing method according to claim 1, wherein the bonding comprises oxide bonding.

5. The foundry-agnostic post-processing method according to claim 1, wherein the thinning comprises:

grinding of outer layers of the substrate; and

chemical mechanical polishing of inner layers of the substrate.

6. The foundry-agnostic post-processing method according to claim 1, further comprising:

analyzing results of respective executions of each of the thinning and bonding to each wafer of the wafer set; and

optimizing the respective executions based on results of the analyzing.

7. A foundry-agnostic post-processing method for a wafer having an active surface, a silicon handle, and a buried oxide (BOX) layer interposed between the active surface and the silicon handle, the foundry-agnostic post-processing method comprising:

producing an output yield at a wafer processing foundry with the production of each wafer in the output yield comprising forming the BOX layer to include doped wells, isolated doped substrate regions and shallow trench isolation regions;

removing one of the wafers from the output yield of the wafer processing foundry;

removing wafers that are similar to the removed one of the wafers from respective output yields of a plurality of wafer processing foundries;

compiling the removed one of the wafers and the removed wafers that are similar to the removed one of the wafers into a wafer set in a post-processing facility;

thinning the silicon handle of each wafer of the wafer set to the BOX layer to expose a new surface; and

bonding the new surface to an alternate material substrate which provides for enhanced device performance as compared to the silicon handle,

wherein the thinning comprises:

recognizing an existence of a via in the BOX layer of each wafer of the wafer set;

executing the thinning of the silicon handle at locations remote from a location of the via; and

adjusting the thinning of the silicon handle at the location of the via in order to avoid the execution of the thinning at the location of the via, wherein:

the adjusting is conducted such that the thinning forms an irregular topology with a bump of material of the silicon handle, which is substantially wider than the via and which protrudes from a plane of the new surface at the location of the via, and

the bonding of the new surface to an alternate material substrate comprises absorbing the irregular topology in the alternate material substrate such that an outward topology of the alternate material substrate is flat at a location corresponding to the location of the via.

8. The foundry-agnostic post-processing method according to claim 7, wherein at least one of the active surface and the silicon handle comprises at least one of silicon (Si) and silicon germanium (SiGe) and wherein the alternate material substrate comprises a high resistivity material.

9. The foundry-agnostic post-processing method according to claim 7, wherein the alternate material substrate comprises at least one of glass and fused silica.

10. The foundry-agnostic post-processing method according to claim 7, wherein the bonding comprises oxide bonding.

11. The foundry-agnostic post-processing method according to claim 7, wherein the thinning comprises:

grinding of outer layers of the silicon handle; and

chemical mechanical polishing of inner layers of the silicon handle.

12. The foundry-agnostic post-processing method according to claim 7, further comprising:

analyzing results of respective executions of each of the thinning and bonding to each wafer of the wafer set; and

optimizing the respective executions based on results of the analyzing.