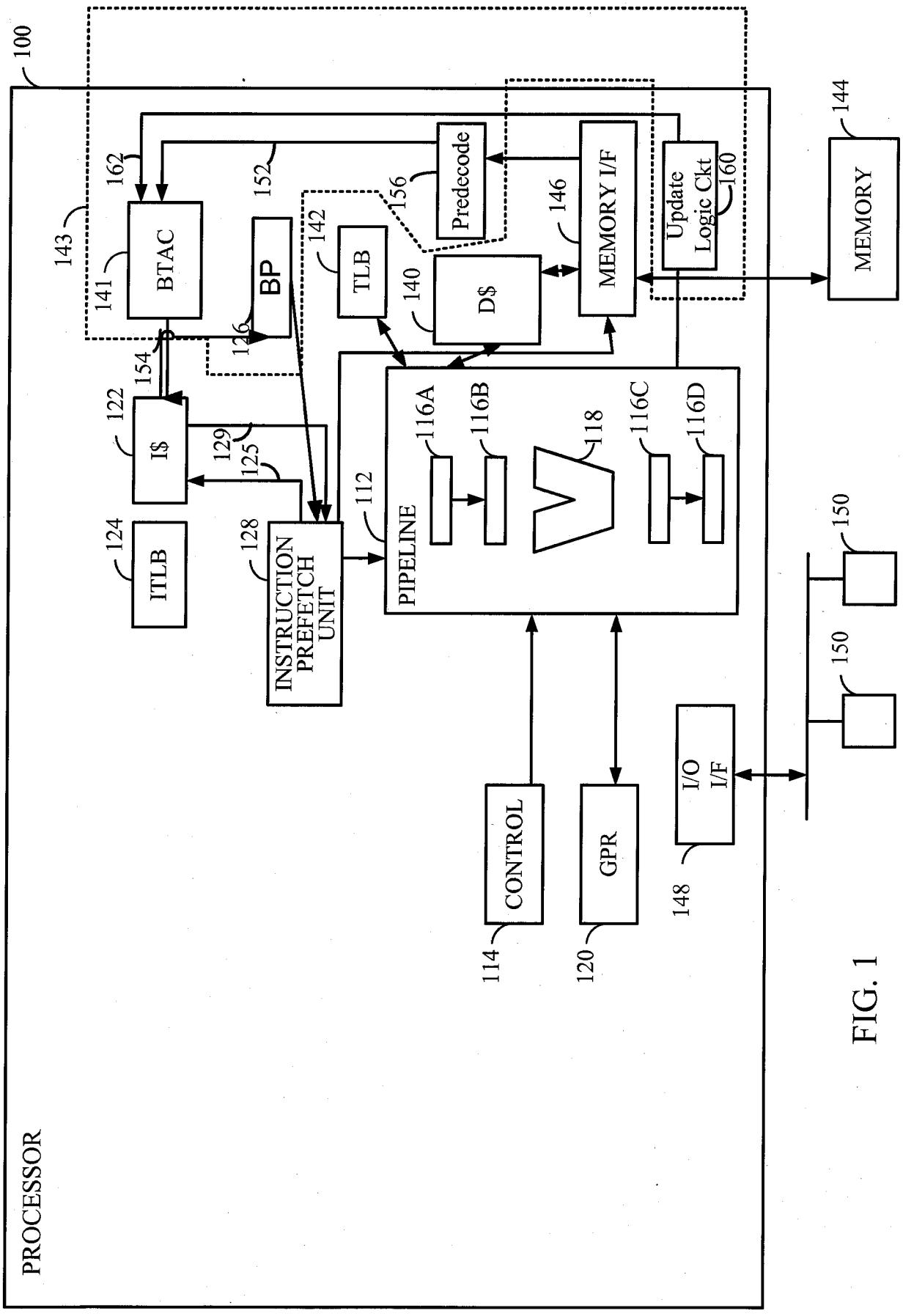

100
PROCESSOR
143
162
BTAC
141
152
BP
126
142
TLB
156
Predecode
140
D$
146
MEMORY I/F
Update Logic Ckt
160
144
MEMORY
154
122
I$
129
125
124
ITLB
128
INSTRUCTION PREFETCH UNIT
112
PIPELINE
116A
116B
118
116C
116D
150
150
I/O I/F
148
CONTROL
114
GPR
120

FIG. 1

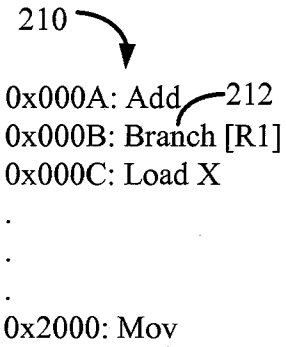


FIG. 2A

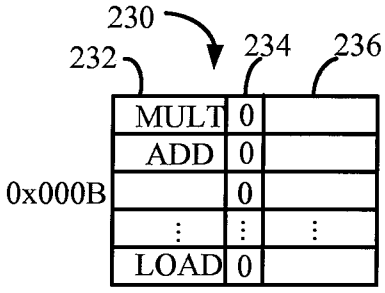


FIG. 2B

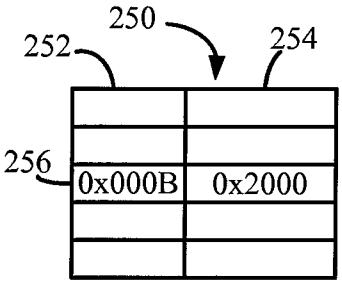


FIG. 2C

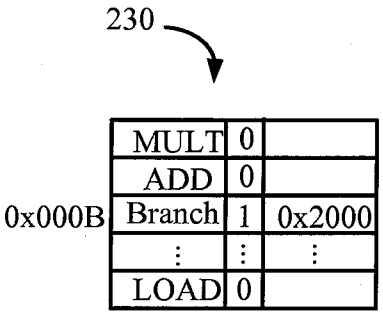


FIG. 3

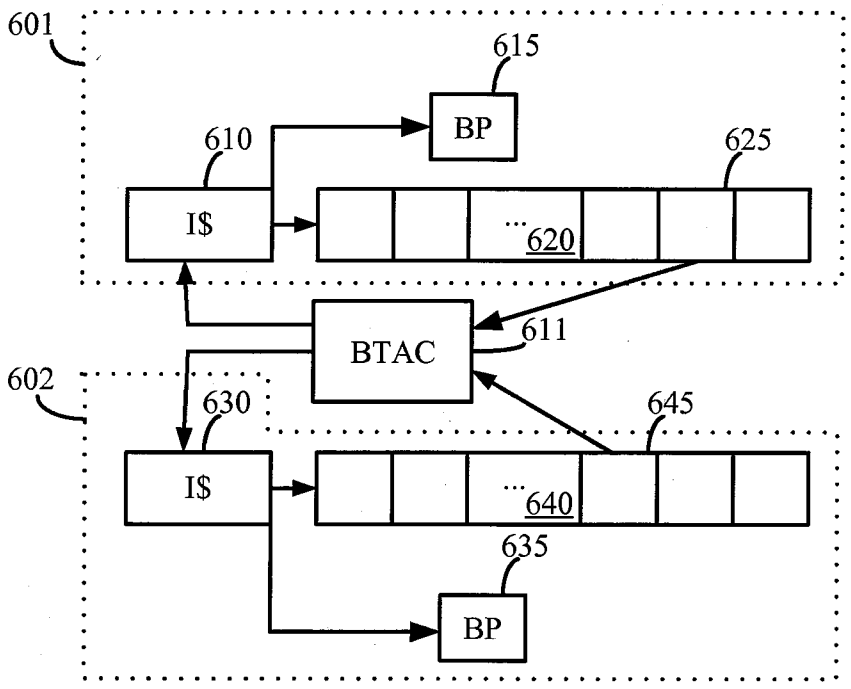


FIG. 6

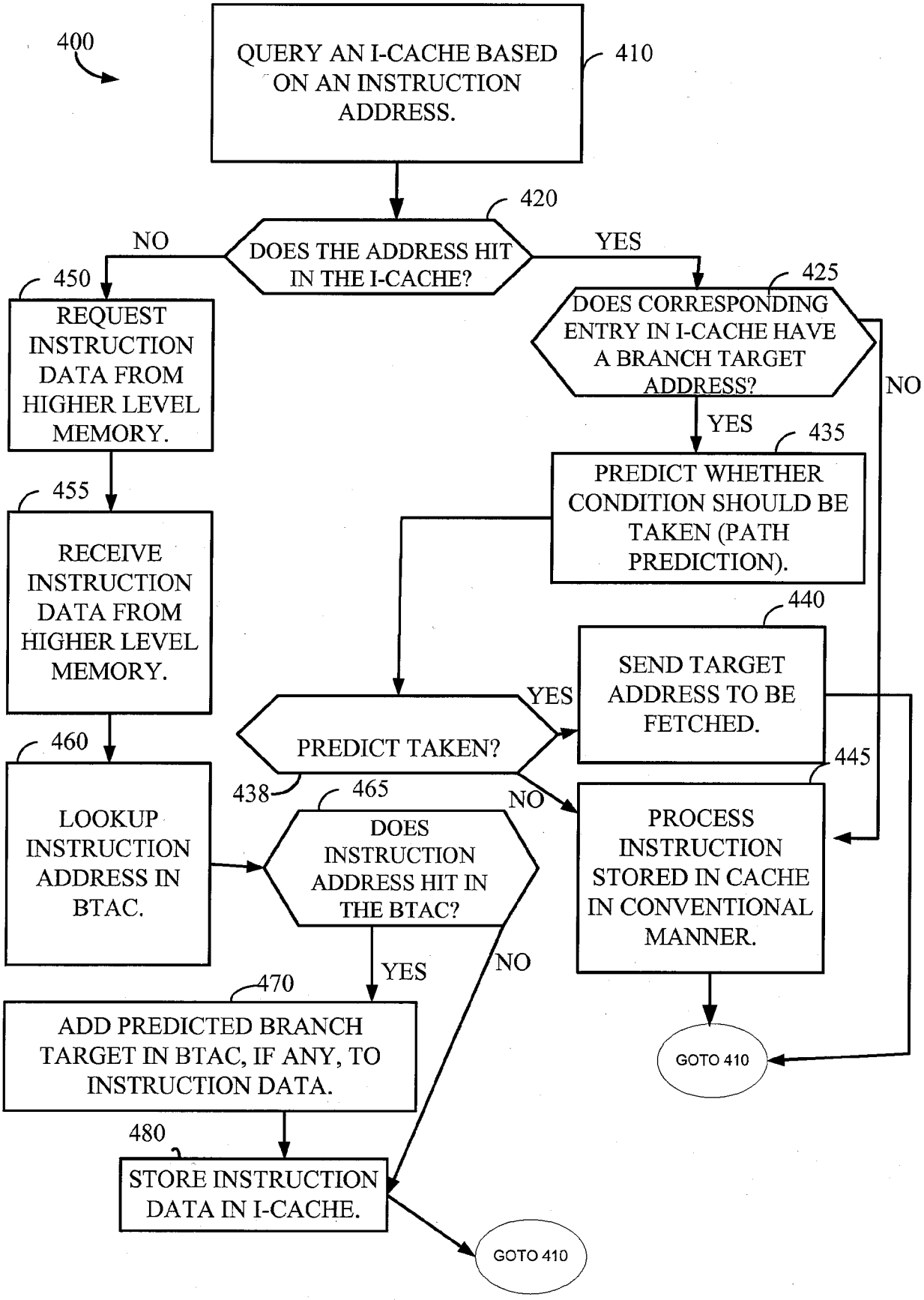

400
QUERY AN I-CACHE BASED ON AN INSTRUCTION ADDRESS.
410
420
DOES THE ADDRESS HIT IN THE I-CACHE?
NO
YES
450
REQUEST INSTRUCTION DATA FROM HIGHER LEVEL MEMORY.
425
DOES CORRESPONDING ENTRY IN I-CACHE HAVE A BRANCH TARGET ADDRESS?
NO
YES
435
PREDICT WHETHER CONDITION SHOULD BE TAKEN (PATH PREDICTION).
455
RECEIVE INSTRUCTION DATA FROM HIGHER LEVEL MEMORY.
440
SEND TARGET ADDRESS TO BE FETCHED.
YES
PREDICT TAKEN?
460
LOOKUP INSTRUCTION ADDRESS IN BTAC.
438
465
DOES INSTRUCTION ADDRESS HIT IN THE BTAC?
NO
445
PROCESS INSTRUCTION STORED IN CACHE IN CONVENTIONAL MANNER.
YES
NO
470
ADD PREDICTED BRANCH TARGET IN BTAC, IF ANY, TO INSTRUCTION DATA.
GOTO 410
480
STORE INSTRUCTION DATA IN I-CACHE.
GOTO 410

FIG. 4

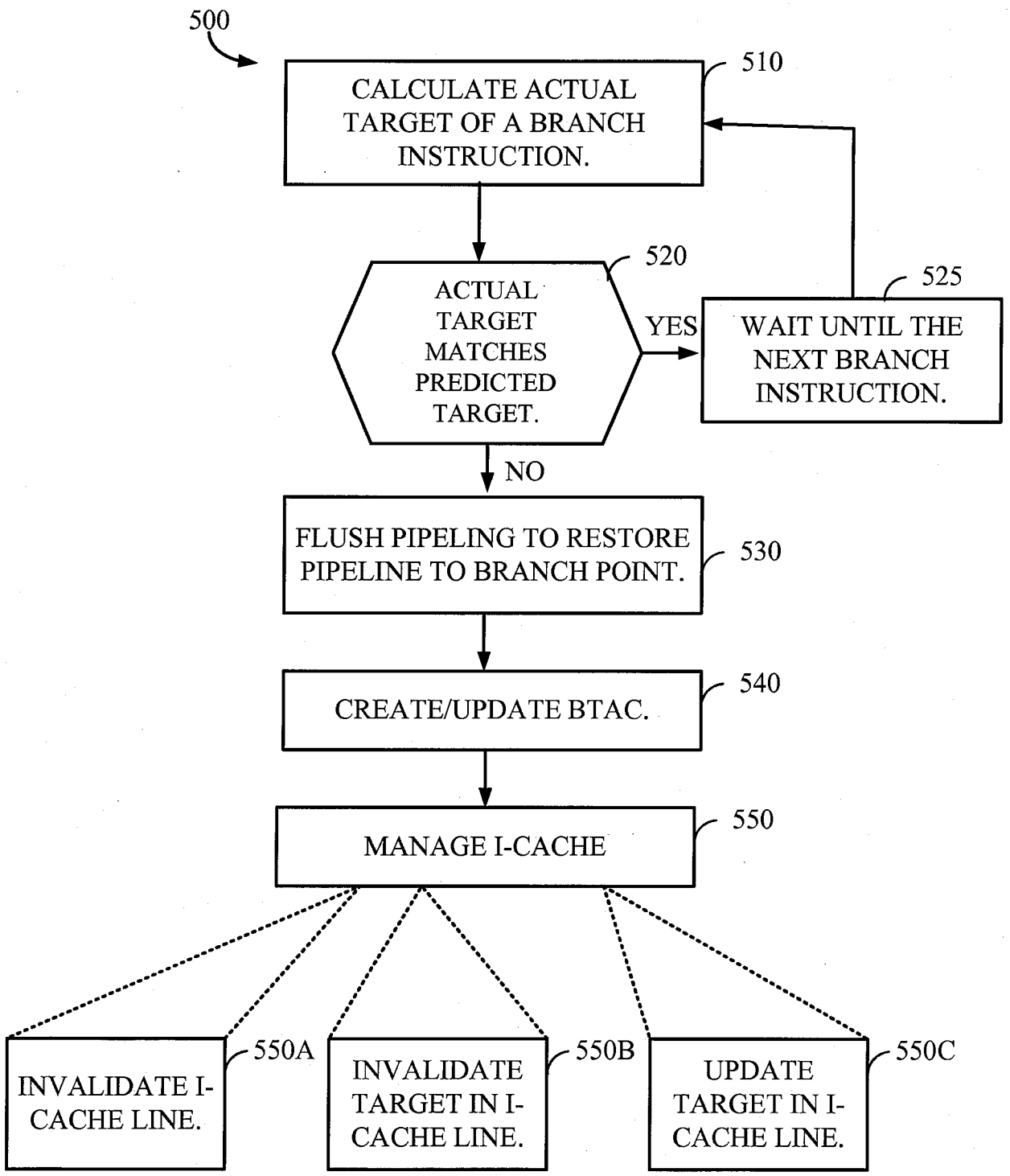

500
CALCULATE ACTUAL TARGET OF A BRANCH INSTRUCTION.
510
ACTUAL TARGET MATCHES PREDICTED TARGET.
520
YES
WAIT UNTIL THE NEXT BRANCH INSTRUCTION.
525
NO
FLUSH PIPELING TO RESTORE PIPELINE TO BRANCH POINT.
530
CREATE/UPDATE BTAC.
540
MANAGE I-CACHE
550
INVALIDATE I-CACHE LINE.
550A
INVALIDATE TARGET IN I-CACHE LINE.
550B
UPDATE TARGET IN I-CACHE LINE.
550C

FIG. 5