

LASER LIFT-OFF PROCESSING SYSTEM INCLUDING METAL GRID

TECHNICAL FIELD

[0001] The present disclosure generally relates to separation of a sapphire or other substrate
5 from a semiconductor LED attached to CMOS substrate.

BACKGROUND

[0002] Various emerging display applications, including wearable devices, head-mounted, and
large-area displays require miniaturized chips composed of arrays of microLEDs (μ LEDs or
10 uLEDs) with a high density having a lateral dimension down to less than 100 μ m X 100 μ m.
MicroLEDs (uLEDs) typically have dimensions of about 50 μ m in diameter or width and
smaller that are used to in the manufacture of color displays by aligning in close proximity
microLEDs comprising red, blue and green wavelengths. Generally, two approaches have been
utilized to assemble displays constructed from individual microLED dies. The first is a pick-
15 and-place approach, which comprises picking up and then aligning and attaching each
individual blue, green and red wavelength microLED onto a backplane, followed by
electrically connecting the backplane to a driver integrated circuit. Due to the small size of
each microLED, this assembly sequence is slow and subject to manufacturing errors.
Furthermore, as the die size decreases to satisfy increasing resolution requirements of displays,
20 larger and larger numbers of die must be transferred at each pick and place operation to
populate a display of required dimensions.

[0003] An alternative to pick-and-place manufacture of semiconductor light-emitting devices
(LEDs) or microLEDs is provided by wafer scale manufacture. Control electronics on a CMOS
die can be directly attached by solder, conductive pillars, or other suitable interconnects to an
25 LED wafer. Unfortunately, processing LED and CMOS connected dies and wafers can be
difficult as compared to processing LED die or wafers alone. Complex process steps such as
sapphire substrate removal, gallium cleaning, and phosphor attachment must be able to be
performed with damaging CMOS die integrity and functionality.

[0004] Laser lift-off processes, which involve projecting a laser light source through a
30 transparent material to be absorbed in an adjacent material on the backside, are a particular
concern. Confined plasma at the interface between a transparent substrate (e.g. sapphire) and
an absorbing material (e.g. GaN) results in lift-off or separation of the materials.

Unfortunately, coatings and processing steps associated with CMOS die attachment can interfere with lift-off. For example, underfill coating between a CMOS die or wafer and an LED die or wafer can include unwanted coating of the transparent substrate, which prevents lift-off unless the underfill is first partially removed.

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SUMMARY

[0005] In one embodiment, a method of manufacturing a light emitting diode (LED) device includes forming an LED structure by depositing a plurality of semiconductor layers on a transparent substrate. Trenched metal is placed in the plurality of semiconductor layers, with the trenched metal contacting the transparent substrate. The LED structure is attached to a CMOS structure with electrical interconnects that define a cavity therebetween. Laser light is used to provide laser lift-off of the transparent substrate from the plurality of semiconductor layers.

[0006] In some embodiments, an underfill material can be deposited in the cavity.

[0007] In some embodiments, the trenched metal is arranged to define a trenched grid.

[0008] In some embodiments, the transparent substrate is sapphire.

[0009] In some embodiments, the electrical interconnects are electrically conductive pillars.

[0010] In some embodiments, the plurality of semiconductor layers are GaN.

[0011] In some embodiments, the method of manufacturing a light emitting diode (LED) device includes attaching an LED structure including trenched metal within a plurality of semiconductor layers to a CMOS structure with electrical interconnects that define a cavity therebetween. Laser light is directed to provide laser lift-off of the transparent substrate from the plurality of semiconductor layers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Non-limiting and non-exhaustive embodiments of the present disclosure are described with reference to the following figures, wherein like reference numerals refer to like parts throughout the various figures unless otherwise specified.

[0013] FIG. 1 is an example process flow for packaging of an LED die attached to a CMOS die or wafer;

[0014] FIG. 2A illustrates an LED die attached to a CMOS die or wafer before underfill;

[0015] FIG. 2B illustrates an LED die attached to a CMOS die or wafer after underfill;

[0016] FIG. 3A illustrates coating an LED die attached to a CMOS die or wafer with an anti-stick coating;

[0017] FIG. 3B illustrates an LED die attached to a CMOS die or wafer after underfill; and

[0018] FIG. 4 illustrates in perspective view removal of sapphire from contact with the LED die and included trenched metal grid.

[0019] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. The figures are not drawn to scale. For example, the heights and widths of the CMOS die or wafer are not drawn to scale.

DETAILED DESCRIPTION

[0020] Before describing several exemplary embodiments of the disclosure, it is to be understood that the disclosure is not limited to the details of construction or process steps set forth in the following description. The disclosure is capable of other embodiments and of being practiced or being carried out in various ways.

[0021] The term "substrate" as used herein according to one or more embodiments refers to a structure, intermediate or final, having a surface, or portion of a surface, upon which a process acts. In addition, reference to a substrate in some embodiments also refers to only a portion of the substrate, unless the context clearly indicates otherwise. Further, reference to depositing on a substrate according to some embodiments includes depositing on a bare substrate, or on a substrate with one or more films or features or materials deposited or formed thereon.

[0022] In one or more embodiments, the "substrate" means any substrate or material surface formed on a substrate upon which film processing is performed during a fabrication process. In exemplary embodiments, a substrate surface on which processing is performed includes materials such as silicon, silicon oxide, silicon on insulator (SOI), strained silicon, amorphous silicon, doped silicon, carbon doped silicon oxides, germanium, gallium arsenide, glass, sapphire, and any other suitable materials such as metals, metal nitrides, III-nitrides (e.g., GaN, AlN, InN and alloys), metal alloys, and other conductive materials, depending on the application. Substrates include, without limitation, light emitting diode (LED) devices. Substrates in some embodiments are exposed to a pretreatment process to polish, etch, reduce, oxidize, hydroxylate, anneal, UV cure, e-beam cure and/or bake the substrate surface. In addition to film processing directly on the surface of the substrate itself, in some embodiments,

any of the film processing steps disclosed are also performed on an underlayer formed on the substrate, and the term "substrate surface" is intended to include such underlayer as the context indicates. Thus for example, where a film/layer or partial film/layer has been deposited onto a substrate surface, the exposed surface of the newly deposited film/layer becomes the substrate surface.

[0023] The term "wafer" and "substrate" will be used interchangeably in the instant disclosure. Thus, as used herein, a wafer serves as the substrate for the formation of the LED devices described herein.

[0024] FIG. 1 is an example process flow 100 for manufacture of an LED die attached to a CMOS die or wafer. In step 102, an LED die or wafer is attached to a CMOS die or wafer using solder, conductive pillars, conductive adhesive material, or other suitable interconnects to an LED wafer. An underfill is applied between the LED die or wafer and the attached to a CMOS die or wafer (step 104). Electrical connectivity and operation of each combined LED die or wafer and attached to a CMOS die or wafer can be tested in a pre-laser lift-off (LLO) yield test, with non-operational die marked for later discard (step 106). Transparent sapphire or other LED substrate material is removed by laser lift-off (step 108), with directed laser energy heating and vaporizing an absorbing interface material such as GaN and allowing separation. In one embodiment, GaN nitride is vaporized and broken down into nitrogen and metallic gallium. The gallium metal can be removed and cleaned using heated water (or weak acid) is used to wash away (or etch away) the gallium residue in step 110. Electrical connectivity and operation of each combined LED die or wafer and attached to a CMOS die or wafer can be tested in a post-laser lift-off (LLO) yield test, with non-operational die marked for later discard (step 112). In step 114, phosphor can be attached to the LED, and electrical connectivity and operation again tested (step 116). In a final step 118, a wafer can be diced (if necessary), and the combined CMOS die and LED packaged.

[0025] FIG. 2A illustrates a structure 200 that includes an LED die or wafer 202 attached to a CMOS die or wafer 210 before underfill. The LED die or wafer 202 includes a sapphire 240 or other transparent substrate that has semiconductor layers 230 including an N-type layer, an active layer, and a P-type layer that is capable of emitting light when electrically powered.

[0026] In one or more embodiments, the transparent substrate comprises one or more of sapphire, silicon carbide, silicon (Si), quartz, magnesium oxide (MgO), zinc oxide (ZnO), spinel, and the like. In one or more embodiments, the substrate is not patterned prior to the

growth of the Epi-layer. Thus, in some embodiments, the substrate is not patterned and can be considered to be flat or substantially flat. In other embodiments, the substrate is patterned, e.g. patterned sapphire substrate (PSS).

[0027] In some embodiments the transparent substrate can support an epitaxially grown or deposited semiconductor N-layer. A semiconductor p-layer can then be sequentially grown or deposited on the N-layer, forming an active region at the junction between layers. Semiconductor materials capable of forming high-brightness light emitting devices can include, but are not limited to, Group III-V semiconductors, particularly binary, ternary, and quaternary alloys of gallium, aluminum, indium, and nitrogen, also referred to as III-nitride materials. In some embodiments, the III-nitride material comprises one or more of gallium (Ga), aluminum (Al), and indium (In). Thus, in some embodiments, the semiconductor layer comprises one or more of gallium nitride (GaN), aluminum nitride (AlN), indium nitride (InN), gallium aluminum nitride (GaAlN), gallium indium nitride (GaInN), aluminum gallium nitride (AlGaIn), aluminum indium nitride (AlInN), indium gallium nitride (InGaIn), indium aluminum nitride (InAlIn), and the like. In one or more specific embodiments, the semiconductor layer 104 comprises gallium nitride and is an n-type layer.

[0028] Electrical and mechanical connection between the CMOS chip or wafer 210 can be provided by electrically conductive pillars 222. The pillars define a cavity or gap 220 that can be filled with an underfill material to improve mechanical stability and attachment, and also improve electrical isolation.

[0029] FIG. 2B illustrates the structure 200 of FIG. 2B with underfill 250 in place. In this embodiment, the underfill has been removed from areas outside cavity 220. Without removal or use of other techniques such as described with respect to FIG. 3A and 3B, underfill would typically form a fillet (denoted by dotted line 251) that makes contact with a sidewall 242 of the sapphire 240. Unfortunately, such an underfill fillet 251 contacting and adhesively retaining the sapphire sidewall 242 may prevent sapphire 240 removal by laser lift-off or require additional underfill removal steps.

[0030] With reference to FIG. 3A the sidewall 242 of an LED die (with sapphire substrate 240) attached to a CMOS die or wafer 210 can optionally be coated with an anti-stick coating 270. The anti-stick coating can be a hydrophobic liquid or other anti-stiction material (e.g., such as liquid Teflon) into which the sapphire 240 is dipped. Care must be taken to not to allow anti-coating material to get into the cavity between the LED and CMOS, since capillary action

would soak up the coating and prevent underfill from adhering within the cavity in later processing steps.

[0031] FIG. 3B illustrates an LED die attached to a CMOS die or wafer after the optional coating of sapphire 240 and sidewalls 242 with anti-stick coating material 270. When placed in the cavity between the LED die and wafer and the CMOS chip or wafer, underfill 250 can further include some excess underfill material 252. This excess material 252 can still contact the CMOS chip or wafer 210 but is not positioned within the cavity. However, since it does not contact the sapphire 240 and sidewalls 242 due to the earlier application of anti-stick coating material 270, there is no interference with laser lift-off.

[0032] FIG. 4 illustrates in perspective view a structure 400 that allows for laser lift-off removal of sapphire 440 from contact with the LED die and included trenched metal grid 460. The structure 400 includes an LED die with semiconductor layers 430 attached to a CMOS chip or wafer 410. Similar to the embodiment discussed with respect to FIG. 2A and 2B, electrical and mechanical connection between the CMOS chip or wafer 410 and the semiconductor layers 430 is provided by electrically conductive pillars 422. The pillars define a cavity or gap that can be filled with an underfill material 450 to improve mechanical stability and attachment, and also improve electrical isolation.

[0033] In this embodiment the semiconductor layers 430 include trenched metal 460 that together forms a trenched metal grid 462. In effect, trenches can help define a plurality of spaced mesas that in turn define pixels, with each of the plurality of spaced mesas comprising the semiconductor layers and each of the spaced mesas having a height less than or equal to their width. The trenched metal 460 is deposited in a space between each of the plurality of spaced mesas, the metal both providing optical isolation between each of the spaced mesas and allowing electrical contact with sidewalls of the GaN LED. In one embodiment, electrical contact can include electrically contacting the N-type layer of each of the spaced mesas along sidewalls of the N-type layers. The space between each of the plurality of spaced mesas can result in a pixel pitch in a range of from 1 μm to 100 μm and space between adjacent edges of the p-contact layer of less than 10% of the pixel pitch when the pixel pitch is in a range of from 10 μm to 100 μm and when the pixel pitch is in a range of 1 μm to 10 μm , the space gap is less than or equal to 5 μm and greater than 0.5 μm .

[0034] In some embodiments, the trenched metal 460 comprises a reflective metal. In some embodiments, the trench metal width is less than or equal to 4 μm and greater than 0.5 μm or

less than or equal to 3 μm and greater than 0.5 μm . In some embodiments, the plurality of spaced mesas between trenched metal grid 462 is arranged into pixels, and the pixel pitch ranges from 5 μm to 100 μm or from 30 μm to 50 μm . In some embodiments, the semiconductor layers 430 have a thickness in a range of from 2 μm to 10 μm .

5 [0035] Since the trenched metal 460 is attached between the sapphire 440 and the semiconductor layers 430 of the LED die, sapphire lift-off requires breaking connection with the metal 460. In this embodiment, laser light 402 decomposes the GaN (or other semiconductor material 430) to create separation from the sapphire 440. While the laser energy is not high enough to cause decomposition and direct release of the metal 460, in
10 regions where the area of GaN is sufficiently greater than the area of the metal 460 the force of nitrogen gas expansion from decomposition of GaN causes separation of metal from sapphire.

[0036] Having described the invention in detail, those skilled in the art will appreciate that, given the present disclosure, modifications may be made to the invention without departing from the spirit of the inventive concept described herein. Therefore, it is not intended that the
15 scope of the invention be limited to the specific embodiments illustrated and described.