(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

G00002

(43) International Publication Date
10 October 2002 (10.10.2002)

PCT

(10) International Publication Number
WO 02/080239 A3

(51) International Patent Classification[7]: H01L 21/027

(21) International Application Number: PCT/US01/48509

(22) International Filing Date:
12 December 2001 (12.12.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/819,342 28 March 2001 (28.03.2001) US

(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: SHIELDS, Jeffrey, A.; 445 Kenmore Avenue, Sunnyvale, CA 94086 (US). OKOROANYANWU, Uzodinma; 1939 Rock Street, Apt. #7, Mountain View, CA 94043 (US). YANG, Chih-Yuh; 1144 Little John Way, San Jose, CA 95129 (US).

(74) Agent: RODDY, Richard, J.; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

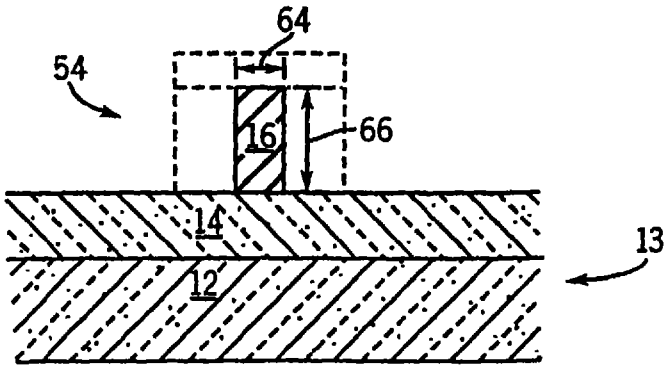
Published:
— *with international search report*

(88) Date of publication of the international search report:
12 December 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

162162

(54) Title: PROCESS FOR FORMING SUB-LITHOGRAPHIC PHOTORESIST FEATURES



(57) Abstract: A process for forming sub-lithographic features in an integrated circuit is disclosed herein. The process includes modifying a photoresist layer (16) after patterning and development but before it is utilized to pattern the underlying layers. The modified photoresist layer (16) has different etch rates in the vertical and horizontal directions. The modified photoresist layer (16) is trimmed with a plasma etch. A feature (54) included in the trimmed photoresist layer (16) has a sub-lithographic lateral dimension.

WO 02/080239 A3