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ABSTRACT OF THE DISCLOSURE**SLEW RATE CONTROL OF OUTPUT DRIVERS USING PVT
CONTROLLED EDGE RATES AND DELAYS**

A novel method and apparatus is presented for reducing the slew rate of transition edges of a digital signal (PAD) on a node (18, 118, 218) of an integrated circuit by adjusting the source resistance (R_{SC} , R_{SD}) of the pre-drive devices (14, 15, 24, 25, 113, 114, 123, 124) to generate a slew-
5 controlled pre-drive signal (DATA') for driving the output drive devices (16, 26, 227, 228, 227a, 228a).

FIG. 1