CLAIMS

What is claimed is:

1. A method comprising:

forming a conformal blocking material layer on a plurality of transistor fins in a non-planar transistor;

removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins, wherein removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins, comprises:

patterning a photoresist material on at least one portion of the conformal blocking material layer;

etching the conformal blocking material layer in areas not covered by the photoresist material; and

removing the photoresist material;

performing an ion implantation on the at least one exposed transistor fin; and removing the conformal blocking material layer.

2. The method of claim 1, wherein forming a conformal blocking layer comprises forming a conformal dielectric blocking material layer.

3. The method of claim 2, wherein forming a conformal dielectric blocking layer comprises forming a conformal dielectric blocking material layer.

~~4. The method of claim 1, wherein removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins, comprises:~~

~~patterning a photoresist material on at least one portion of the conformal blocking material layer;~~

~~etching the conformal blocking material layer in areas not covered by the photoresist material; and~~

~~removing the photoresist material.~~5<u>4</u>. The method of claim 1, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing an angled ion implantation on the at least one exposed transistor fin.

~~6~~5. The method of claim ~~5~~4, wherein performing an angled ion implantation on the at least one exposed transistor fin comprises performing an angled ion implantation on opposing sidewalls of the at least one exposed transistor fin.

~~7~~6. The method of claim 1 , wherein performing an ion implantation on the at least one exposed transistor fin comprises performing a P-type ion implantation on the at least one exposed transistor fin.

~~8~~7. The method of claim 1 , wherein performing an ion implantation on the at least one exposed transistor fin comprises performing an N-type ion implantation on the at least one exposed transistor fin.

~~9~~8. A method comprising:

forming a non-planar transistor having a plurality of transistor fins;

forming a conformal blocking material layer on the plurality of transistor fins such that at least one of the plurality of transistor fins is covered by the conformal blocking material layer and at least one of the plurality of transistor fins is not covered by the conformal blocking material layer, wherein forming the conformal blocking material layer comprises:

depositing the conformal blocking material layer on plurality of transistor fins; and removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins, wherein removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins, comprises:

patterning a photoresist material on at least one portion of the conformal blocking material layer; and

etching the conformal blocking material layer in areas not covered by the photoresist material; and

performing an ion implantation on the at least one transistor fin not covered by the conformal blocking material layer.

~~10. The method of claim 9, wherein forming the conformal blocking material layer comprises:~~

~~depositing the conformal blocking material layer on plurality of transistor fins; and removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins;~~

~~11. The method of claim 10, wherein removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins, comprises:~~

~~patterning a photoresist material on at least one portion of the conformal blocking material layer; and~~

~~etching the conformal blocking material layer in areas not covered by the photoresist material.~~12~~9~~. The method of claim ~~9~~8, further comprising removing the conformal blocking material layer.

~~13~~10. The method of claim ~~9~~8, wherein forming a conformal blocking material layer comprises forming a conformal dielectric blocking material layer.

~~14~~11. The method of claim ~~9~~8, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing an angled ion implantation on the at least one exposed transistor fin.

~~15~~12. The method of claim ~~14~~11, wherein performing an angled ion implantation on the at least one exposed transistor fin comprises performing an angled ion implantation on opposing sidewalls of the at least one exposed transistor fin.

~~16~~13. The method of claim ~~9~~8, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing a P-type ion implantation on the at least one exposed transistor fin.

~~17~~14. The method of claim ~~9~~8, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing an N-type ion implantation on the at least one exposed transistor fin.

~~18~~15. A microelectronic device, comprising:

at least one non-planar transistor having a plurality of transistor fins; and at least one of the plurality of transistor fins having a substantially uniform ion doping

along the height of the transistor fin, wherein doping is performed by a process comprising:

forming a conformal blocking material layer on the plurality of transistor fins such that at least one of the plurality of transistor fins is covered by the conformal blocking material layer and at least one of the plurality of transistor fins is not covered by the conformal blocking material layer, wherein forming the conformal blocking material layer comprises:

depositing the conformal blocking material layer on plurality of transistor fins; and removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins, wherein removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins, comprises:

patterning a photoresist material on at least one portion of the conformal blocking material layer; and

etching the conformal blocking material layer in areas not covered by the photoresist material; and

performing an ion implantation on the at least one transistor fin not covered by the conformal blocking material layer.

~~19. The microelectronic device of claim 18, wherein forming the conformal blocking material layer comprises:~~

~~depositing the conformal blocking material layer on plurality of transistor fins; and removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins;20. The microelectronic device of claim 19, wherein removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins, comprises:~~

~~patterning a photoresist material on at least one portion of the conformal blocking material layer; and~~

~~etching the conformal blocking material layer in areas not covered by the photoresist material.21~~16. The microelectronic device of claim ~~18~~15, further comprising removing the conformal blocking material layer.

~~22~~17. The microelectronic device of claim ~~18~~15, wherein forming a conformal blocking material layer comprises forming a conformal dielectric blocking material layer.

~~23~~18. The microelectronic device of claim ~~18~~15, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing an angled ion implantation on the at least one exposed transistor fin.

~~24~~19. The microelectronic device of claim ~~23~~18, wherein performing an angled ion implantation on the at least one exposed transistor fin comprises performing an angled ion implantation on opposing sidewalls of the at least one exposed transistor fin.

~~25~~20. The microelectronic device of claim ~~18~~15, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing a P-type ion implantation on the at least one exposed transistor fin.

~~26~~21. The microelectronic device of claim ~~18~~15, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing an N-type ion implantation on the at least one exposed transistor fin.