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MEMORY CIRCUITRY WITH AUXILIARY WORD LINE TO OBTAIN PREDICTABLE ARRAY OUTPUT WHEN AN INVALID ADDRESS IS REQUESTED

ABSTRACT

A memory circuit design efficiently obtains predictable array output when an invalid address is requested. The memory circuit component (200) comprises an invalid word line path (212), in addition to a standard valid word line path (207). To provide correct output, a dummy word line output (208) of a first decode logic (205) is delayed (209A), and the delayed dummy word line output (210) is ANDed (213) with a word line output (207) to update the data out latch (217). Further, the invalid word line output (212) of a second decode logic (211) is also delayed (209B), and the delayed invalid word line output (214) is ORed (215) with the delayed dummy word line output (210) to reset the control logic (219). ORing (215) the delayed signals allows the predictable output to be provided at a common clock time, irrespective of whether a valid address or an invalid address is decoded.

FIG. 2