SIGNAL PROCESSING DISTRIBUTED ARITHMETIC ARCHITECTURE

ABSTRACT OF THE DISCLOSURE

An apparatus computes an inner product vector of a matrix and a vector. The matrix has a first set of coefficients and the vector has a second set of coefficients. At least one input register (110) is used to store the second set of coefficients. A plurality of storage elements (120) are used to store partial sums that are pre-calculated from the first set of coefficients of the matrix. The outputs of the at least one input register (110) are used as the address inputs to the plurality of storage elements to select a subset of the partial sums. In addition, a select circuit (150) is coupled to the storage elements' address lines to determine which row in the matrix the vector forms one element of the resultant inner product for that row. The subset of partial sums from the outputs of the storage elements (120) are added in an adder circuit (130) to create a summation output that presents the element of the inner product vector of the matrix multiplied by the vector. The apparatus has the advantages of reduced integrated circuit area and the ability to create elements of the inner product vector in any desired order.

Figure 2