(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 December 2007 (13.12.2007)

PCT

(10) International Publication Number
WO 2007/143695 A2

(51) International Patent Classification:
G06F 13/42 (2006.01)

(21) International Application Number:
PCT/US2007/070527

(22) International Filing Date: 6 June 2007 (06.06.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/804,141 7 June 2006 (07.06.2006) US
11/428,211 30 June 2006 (30.06.2006) US

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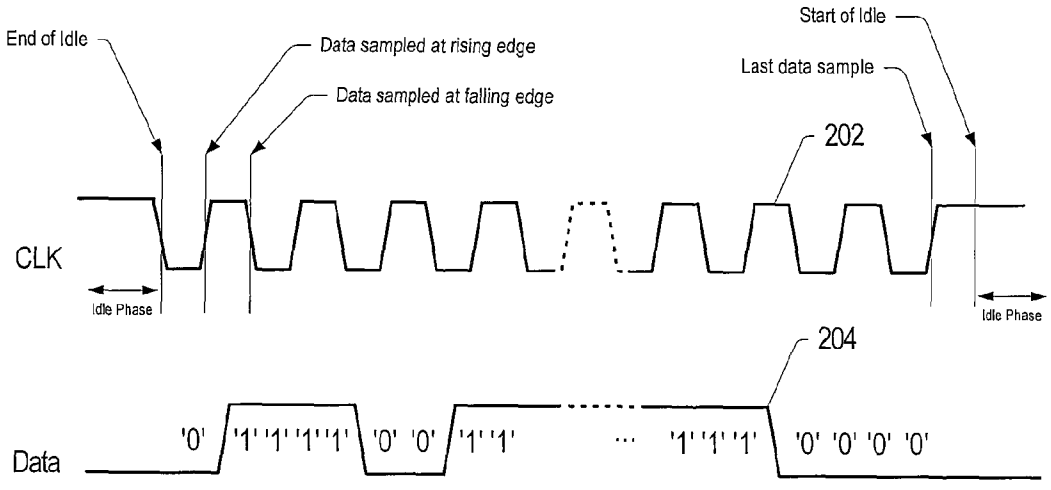
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** LOW POWER AND LOW PIN COUNT BI-DIRECTIONAL DUAL DATA RATE DEVICE INTERCONNECT INTERFACE



(57) **Abstract:** A simple clock source synchronous DDR data transfer mechanism may be combined with static bus state signaling to replace a complex bus (e.g. USB) with an easy to implement digital serial interconnect bus. This may eliminate various pull-up/pull-down resistors required in USB, and enable the interconnect bus to operate with little or no leakage current when the bus is in an idle state, or data transmission state. All required functionality may be implemented using only two signal pins. The interconnect bus may also enable silicon solutions for high speed USB that do not require a PLL, since the clock may be provided by the transmission source and may thus not need to be recovered from the serial data stream. The digital serial interconnect bus may provide an easy reuse mechanism for USB silicon by enabling a designer to remove the analog PHY and replace it with a serial digital I/O transfer mechanism, while retaining the IP's USB timers, and other protocol specific features.

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