

The invention relates to a filter for digitally transmitted communication signals. Such signals may, for example, serve for the digital transmission of audio items of information.

During the wireless transmission of communication signals, obliteration of certain components of the signal may occur due to multipath reception. It is known to reduce such interference by a suitable formulation of the make-up of the signal in combination with appropriate signal processing measures in the receiver and/or by selection of the transmitting frequencies.

With receivers which are stationary when operating, it is only necessary to undertake an optimum tuning of the receiver for the actual receiving situation once, e.g. each time one is switched on. However, with receivers that are operational in motor vehicles, a continuous matching to the rapidly altering reception conditions is required. To this end, a test frequency for example, can be periodically transmitted and evaluated in the receiver using a correlation process. The result of this then provides the adjustment magnitudes for an (adaptive) filter that is to be switched into the signal path. Such methods are described for example, in the following papers: G.D. Forney, Jr "Training adaptive linear filters", U.S. patent No. 3,723,911 March 27, 1973.

K.H. Mueller and D.A. Spaulding, "Cyclic equalisation - a new rapidly converging equalisation technique for synchronous data communication", Bell System J, pp 369 - 406, Feb 1975.

For the rapid multiplication of multi-place binary numbers, these are divided up into 8 place numbers, for example, in FR-A-2 276 635, the leading and trailing zeros are suppressed and the mantissae and exponents are then formed. Every number which differs from zero is used in the multiplication.

FIR filters using delay members are described in H. Göckler, "Einstellbare Digitalfilter für die Tontechnik", N.T.Z. -Archiv, pages 47 - 57, volume 7, No 3, March 1985.

The adaptive methods described in these papers require very complex technology which can be furnished, for example, by means of a computer (signal processor) having an appropriately powerful performance.

For solving the problem, a filter arrangement, which can be continually matched to the changing reception conditions by means of a shift register and a computer, is generally used. The message which has "to be filtered" consists, for example, of a sequence of digitally coded values each of 8 bits and it is continually fed to the shift register. The shift register is dimensioned such that for example, at least 1024 values each of 8

bits can be stored. By the utilisation of this great length of e.g. 1024 values, a new output value is calculated for each of these individual values by means of a computer e.g. a signal processor, in accordance with a predefined mathematical law. The new output value determined by the computer thus depends on 1024 individual values. The mathematical law provided can be considered to be constant for each new output value over this length of information and, in general, over still greater lengths of e.g. several 1000's of values. After the expiry of the predetermined length of e.g. 1024 values, or after the expiry of still greater lengths of e.g. several blocks each of 1024 bits, the formulation of the mathematical law for the calculation of the new output values, which is associated with the filter, then has to be altered.

Since the processes for each output value already demand very considerable expenditure in terms of the number of calculations required e.g. 1024, 8 bit multiplications together with the respective additions, but, on the other hand, the processing time of present day signal processors is substantially less than the time available for a multiplication process, the calculation expediently occurs in serial fashion even for the individual output values, whereby the corresponding base values are made available by intermediate circulations in the shift register. In the example chosen, the time available for the calculation of the great length (series) of data amounts to a few milliseconds i.e. ca 1000 output values have to be calculated in ca 1 ms, which, in turn, means ca 1000 multiplications (per output value) in 1 μ sec. This cannot be done even by the best of modern processors and, in addition, such a flow of data cannot be read out from a shift register. Since the processing time for a multiplication amounts to 25 nsec for example, a correspondingly large number of processors must be connected in parallel in order to fulfil this task, which is something however, that is out of the question for apparatus in the field of consumer goods on the grounds of cost and for other practical reasons.

The object of the invention is to develop a filter arrangement that is suitable for use in consumer receivers and that can be very rapidly matched to changing reception conditions. This object is achieved by the invention characterised in claim 1. Further developments of the invention are specified in the appendant claims.

For a more detailed explanation, the invention will be described hereinafter with the help of embodiments. These depict in

Fig. 1 a digital filter,

Fig. 2 an exemplary circuit,

Fig. 3 an example of simultaneous calculation,

Fig. 4 a further exemplary circuit.

Fig. 1 shows the basic construction of a transversal filter which is suitable for achieving the previously described object. The items of data of a digitally coded communication signal are supplied to a shift register 1. The output signal is formed by multiplying the individual shift register output signals by specific co-efficients ($C_1 \dots C_n$).

Fig. 2 shows an embodiment of the invention which strives to effect a serial calculation using only one processor. In order to achieve this, use is made of the fact that the multiplications that have to be carried out for one output value make different contributions to the output value (corresponding to multipliers or co-efficients of e.g. 0 to 1). Basically for this, each of the products involving a multiplier of 0 is sorted out in a "preliminary process" because they do not make any contribution to the sum of the products. The remaining number of values are arranged in accordance with their magnitude and are limited to a certain, previously determined number of e.g. 50 (from 1024).

The circuit then comprises a storing shift register of corresponding length, e.g. 1024 values each of 8 bits. Since the values to be used for the calculation are now arbitrarily distributed through the register, the relevant values can no longer be made directly available by shifting processes in the register. That is to say, this would unnecessarily increase the demands made on the technology used for the shift register. Consequently, the individual cells of the shift register are connected to a switching matrix (network of logical gates) so that corresponding groups of shift register outputs can be connected through to a corresponding number of outputs of the matrix. The switching matrix is controlled by means of the sequence of addresses detected in the previously described manner whereby the sequence during the calculation process for an output value can be quite arbitrary because all of the products are combined together into a total.

The 8 bit values are assigned serially to an output of the shift register or to the input of the matrix 3 so that the transmission of a value occurs serially. As in Fig. 1, it can be advantageous to buffer store (registers A, B etc) a part of the value at the output of the matrix for matching the calculating process in the processor. For this, the matrix has to be correspondingly extended when necessary.

Fig. 3 shows how the calculation is carried out simultaneously for a plurality of output values. The processor works alternately with a plurality of stores containing totals (accumulators). The association of the values in the calculating process is shown. The advantages consist in that respective adjacent cells of the shift register can be combined into blocks and read out serially during partial cycles; further, that the multipliers in the processor can be kept constant for the combined group of values. The shift register is shifted on by one block length for a new group of values.

Fig. 4 shows a further embodiment in which the function of the store is taken over by a RAM module (Random Access Memory) having a correspondingly lower access time. In this case, it is necessary to ensure that the required contents of the store reach the output by means of a preliminary address calculation and associated control process. The number of addresses theoretically required corresponds to the number of constants (co-efficients; 50 in the chosen example) multiplied by the number of output values which are to be calculated one after the other for a section having constant co-efficients. This would result in 100,000 addresses having to be calculated for e.g. 2000 output values. With an appropriate arrangement of the values in the RAM module (analogous to the shift register), one can commence in advantageous manner from a single (first) set of addresses, 50 in the chosen example, and all of the addresses can be respectively increased by 1 for each new output value in a simple calculating process, or, be decreased by 1 where the sequence in the store is reversed.

Basically, the total amount of information, for which the law of formation of the output values is constant, has to be kept available in the RAM store since, with a once selected sequence, any subsequent loading would mean exchanging the whole content of the store and thus interfering with the calculating process. The parts of the information that are no longer needed could of course be dropped, similarly to the case of the shift register, and be continuously replaced by the newly arriving information. However, with the RAM, one disadvantage would be that the sequence (with reference to the addresses) is then no longer harmonic and thus a complicated address calculation has to be carried out.

Where there are a plurality of signals e.g. the I and Q signal when using 4-PSK demodulation, it may be necessary to effect a filtering process in a receiver. Moreover, a plurality of different filtering processes may arise e.g. a so-called matched-filter process and an equaliser process. Insofar as the calculating capacity of the processor permits, the individual processes are combined (I and Q), or, they are executed, one

after the other, by the same processor (matched-filter and equaliser). Two storage registers running in parallel have to be provided in the case of the I and Q signals. Calculated intermediate values e.g. the output values of the matched-filter, have to be kept in a buffer store in order to be able to carry out the equalising process with them.



Claims

1. Digital filter for digitally coded communication signals, especially audio signals, including a shift register (SR) for storing the digital signal values, a computer for calculating new output values of predetermined length for each signal value and a circuit for determining the co-efficients for the digital filter, characterised by,
 - a preliminary process for sorting out signal values or co-efficients for all such signal value - co-efficients - products for which a multiplier of "0" or approximately "0" is provided;
 - a sorting of the remaining co-efficients in accordance with their magnitude;
 - a limiting, of the number of the sorted co-efficients, to a predetermined number,wherein, in particular, a correlator serves for determining the transmission properties for determining the co-efficients for the digital filter.
2. Digital filter in accordance with Claim 1, characterised in that, the individual cells of the shift register are connected to a switching matrix in such a way that corresponding groups of successive cells can be switched through to a corresponding number of outputs and the output signals available at the outputs are supplied to a signal processor.
3. Digital filter in accordance with Claim 1 or 2, characterised in that, the switching matrix and the signal processor are synchronously controlled by a pre-processor.
4. Digital filter in accordance with any of the Claims 1 to 3, characterised in that, the or a part of the values at the output of the switching matrix are buffer stored in order to be able to carry out a plurality of calculations, one after the other, without a shifting process.
5. Digital filter in accordance with Claim 4, characterised in that, the output signals are calculated, one after the other, using the same co-efficients and are respectively added in different output registers or accumulators.
6. Digital filter in accordance with any of the Claims 2 to 5, characterised in that, a RAM and an address store are used instead of a shift register and a matrix and the addresses are made available during a cyclic cycle of the address store and are increased by "1" at each cycle.