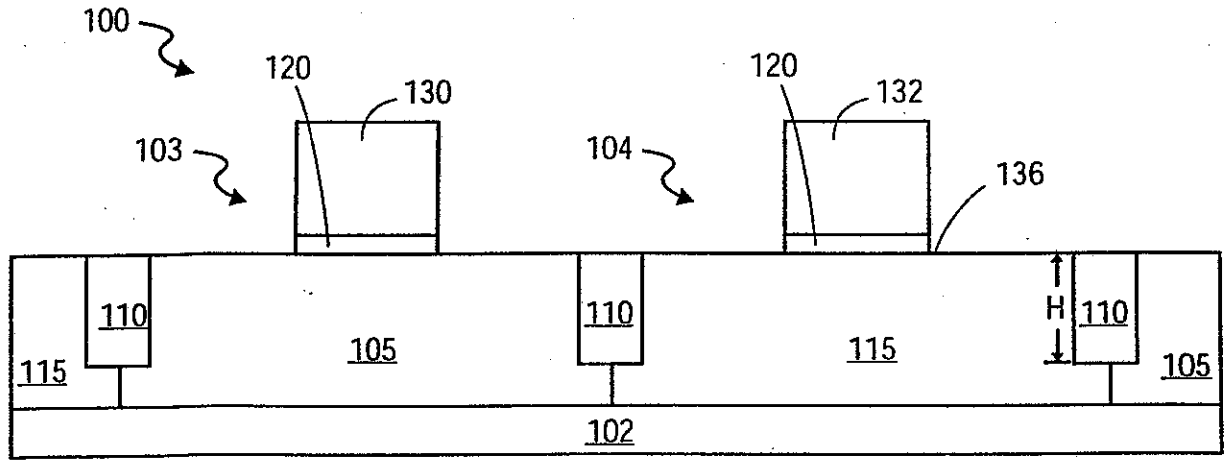

100
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103
104
120
132
136
110
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110
H
105
115
115
105
102

FIG. 1

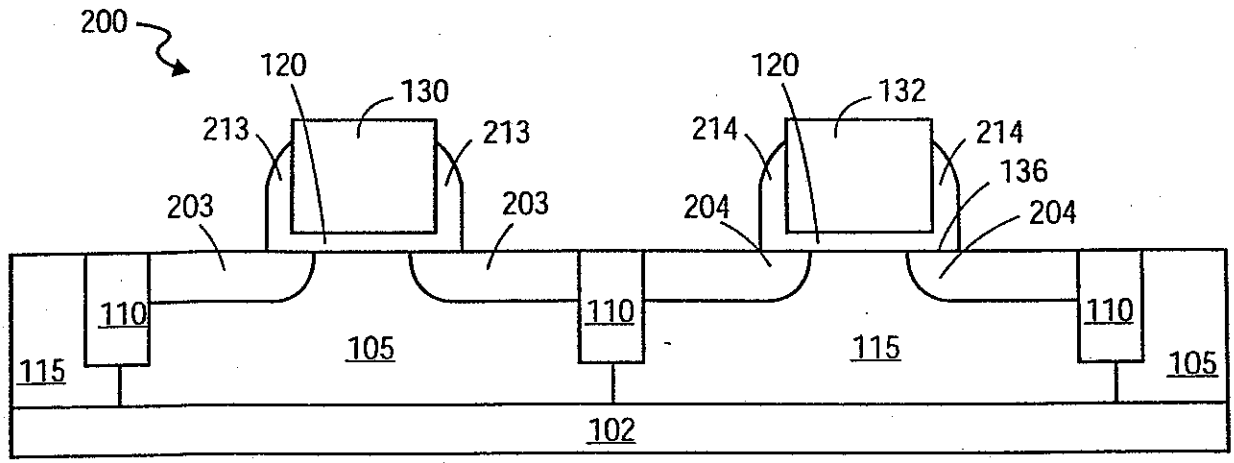

200
120
130
213
213
203
203
120
132
214
214
136
204
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110
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115
105
102

FIG. 2

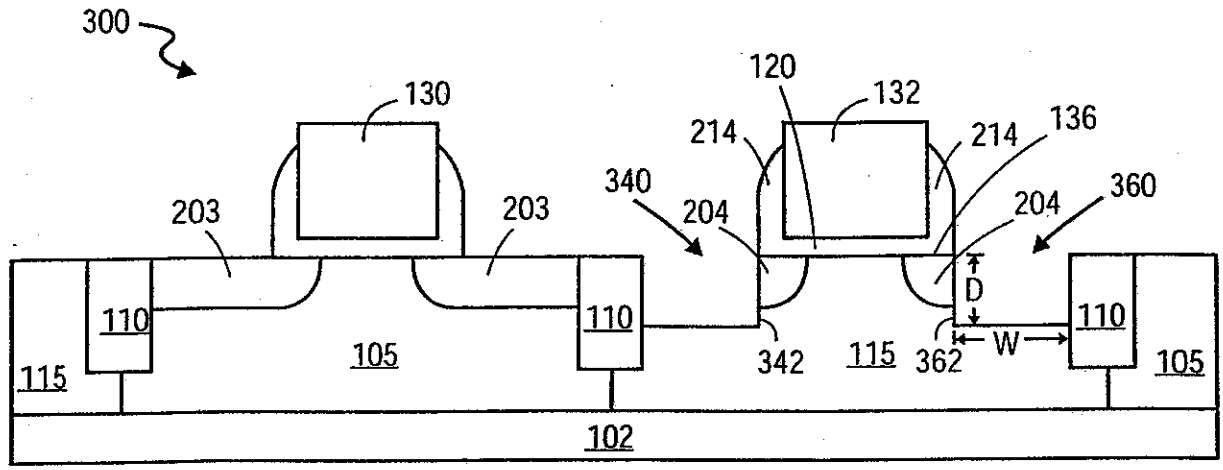


FIG. 3

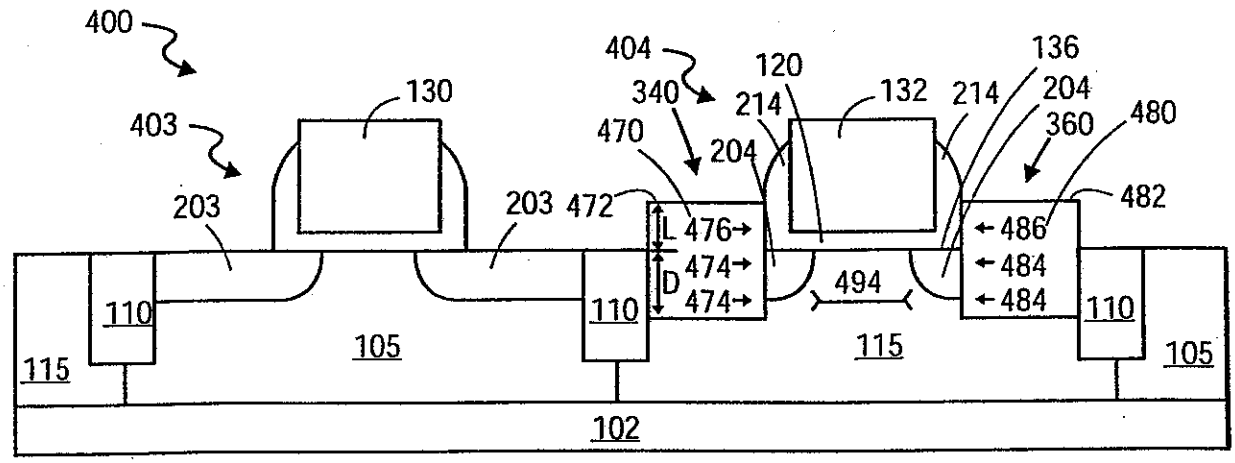


FIG. 4

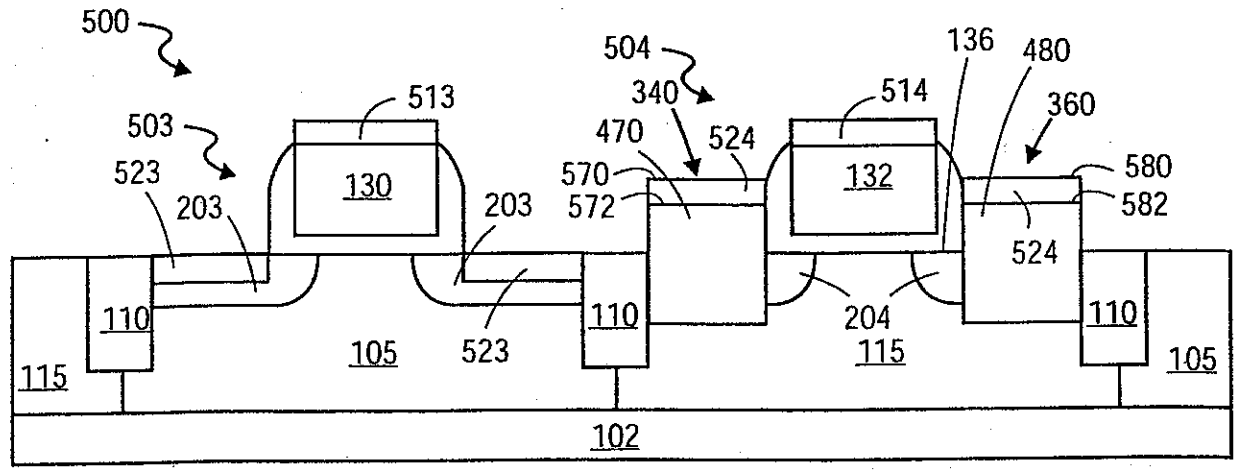


FIG. 5

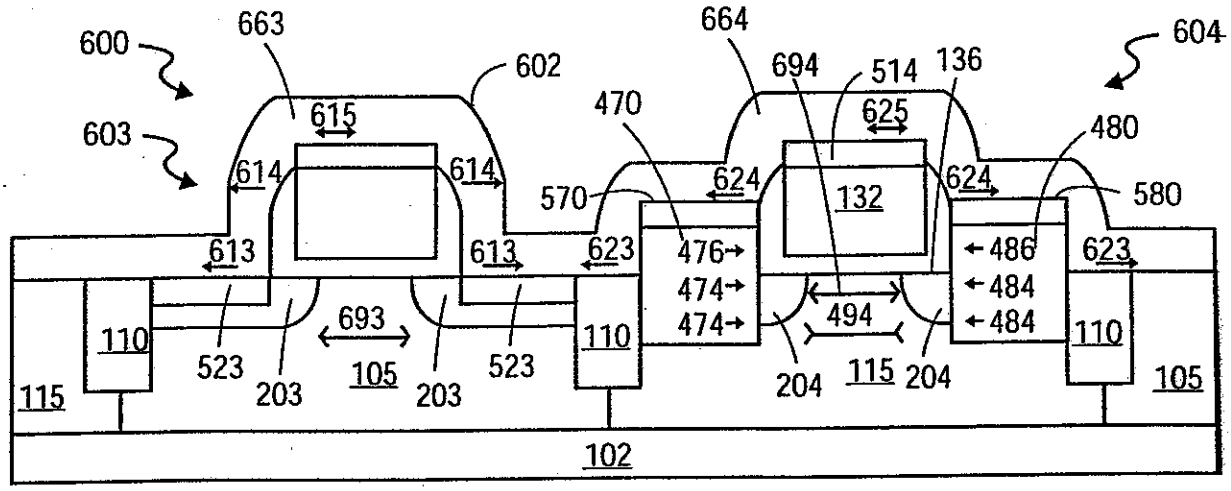

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613
623
623
476
474
474
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693
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110
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523
203
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523
204
115
204
115
105
102

FIG. 6

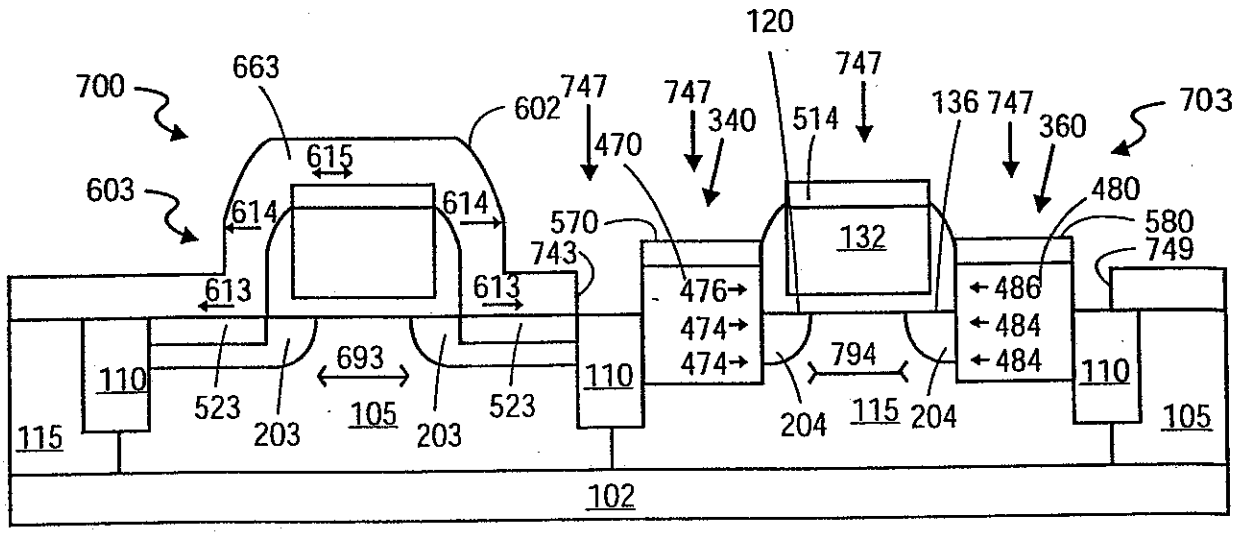

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747
747
602
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340
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136
747
360
703
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603
470
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570
132
580
743
749
613
613
476
474
474
486
484
484
693
794
110
110
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523
203
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203
523
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204
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105
102

FIG. 7

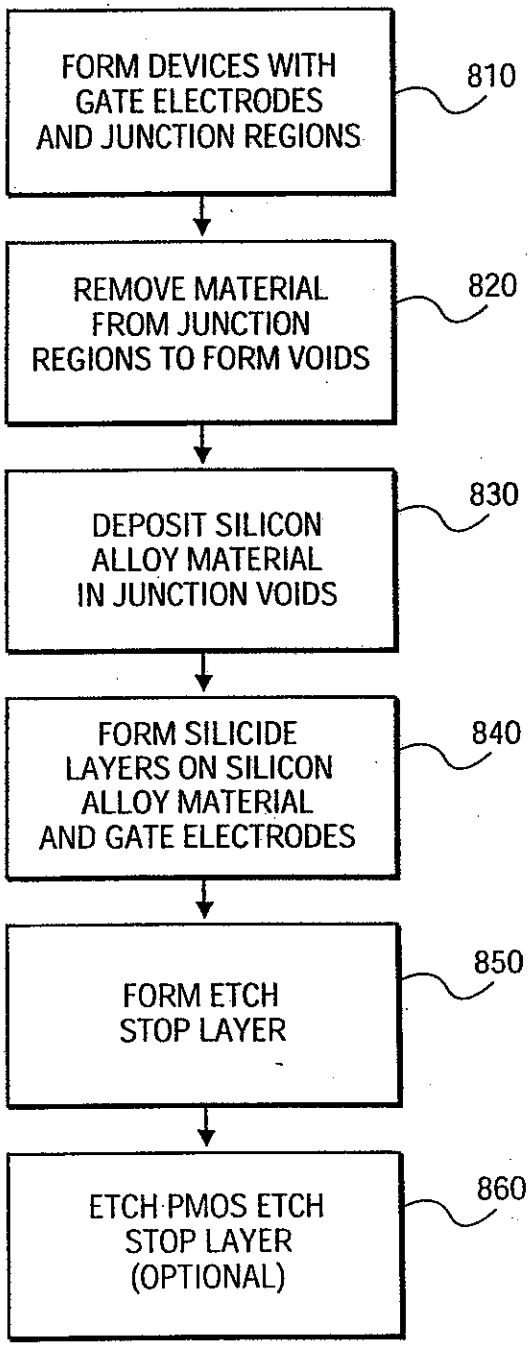

FORM DEVICES WITH GATE ELECTRODES AND JUNCTION REGIONS
810
REMOVE MATERIAL FROM JUNCTION REGIONS TO FORM VOIDS
820
DEPOSIT SILICON ALLOY MATERIAL IN JUNCTION VOIDS
830
FORM SILICIDE LAYERS ON SILICON ALLOY MATERIAL AND GATE ELECTRODES
840
FORM ETCH STOP LAYER
850
ETCH PMOS ETCH STOP LAYER (OPTIONAL)
860

FIG. 8