

SYSTEMS AND METHODS FOR LED STRUCTURES THAT INCREASE CURRENT FLOW DENSITY

TECHNICAL FIELD

[0001] The present disclosure relates generally to light emitting diode (LED) display devices, and more particularly, to systems and fabricating methods for micro-LED semiconductor devices and structures that increase the PN junction current flow density of the LED.

BACKGROUND

[0002] Display technologies are becoming increasingly popular in today's commercial electronic devices. These display panels are widely used in stationary large screens such as liquid crystal display televisions (LCD TVs) and organic light emitting diode televisions (OLED TVs) as well as portable electronic devices such as laptop personal computers, smartphones, tablets and wearable electronic devices. With the development of Mini LED and Micro LED technology in recent years, consumer devices and applications such as augmented reality (AR), projection, heads-up display (HUD), mobile device displays, wearable device displays, and automotive displays, require LED panels with improved efficiency and resolution. For example, an AR display integrated within a goggle and positioned close to a wearer's eyes can have a dimension of a fingernail while still demanding an HD definition (1280x720 pixels) or higher.

[0003] Also, active matrix liquid-crystal displays (LCD) and organic light emitting diode (OLED) displays combined with thin-film transistor (TFT) technology are becoming increasingly popular in today's commercial electronic devices. These displays are widely used in laptop personal computers, smartphones and personal digital assistants. Millions of pixels together create an image on a display. The TFTs act as switches to individually turn each pixel on and off, rendering the pixel light or dark, which allows for convenient and efficient control of each pixel and of the entire display.

[0004] However, conventional LCD displays suffer from low light efficiency, causing high power consumption and limited battery operation time. While active-matrix organic light-emitting diode (AMOLED) display panels generally consume less power than LCD

panels, an AMOLED display panel can still be the dominant power consumer in battery-operated devices. To extend battery life, it is desirable to reduce the power consumption of the display panel.

[0005] Conventional inorganic semiconductor light emitting diodes (LED) have demonstrated superior light efficiency, which makes active matrix LED displays more desirable for battery operated electronics. Arrays of driver circuitry and light emitting diodes (LEDs) are used to control millions of pixels, rendering images on the display. Both single-color display panels and full-color display panels can be manufactured according to a variety of fabrication methods.

[0006] However, the integration of thousands or even millions of micro LEDs with pixel driver circuit array is quite challenging. Various fabrication methods have been proposed. In one approach, control circuitry is fabricated on one substrate and LEDs are fabricated on a separate substrate. The LEDs are transferred to an intermediate substrate and the original substrate is removed. Then the LEDs on the intermediate substrate are picked and placed one or a few at a time onto the substrate with the control circuitry. However, this fabrication process is inefficient, costly and not reliable. In addition, there are no existing manufacturing tools for mass transferring micro LEDs. Therefore, new tools must be developed.

[0007] In another approach, the entire LED array with its original substrate is aligned and bonded to the control circuitry using metal bonding. The substrate on which the LEDs are fabricated remains in the final product, which may cause light cross-talk. Additionally, the thermal mismatch between the two different substrates generates stress at the bonding interface, which can cause reliability issues. Furthermore, multi-color display panels typically require more LEDs and different color LEDs grown on different substrate materials, compared with single-color display panels, thus making the traditional manufacturing process even more complicated and inefficient.

[0008] As such, it would be desirable to provide an LED structure for display panels that addresses one or more of the above-mentioned drawbacks, amongst others.

SUMMARY

[0009] There is a need for improved LED designs that improve upon, and help to address one or more of the shortcomings of conventional display systems, such as those described above. In particular, there is a need for an LED device structure that can improve the light emitting efficiency, fabrication efficiency, reliability, and resolution at the same time while efficiently maintaining low power consumption.

[0010] Light emitting diode (LED) is a junction luminescent device, and the main structure of LED is a P-N junction. Under a forward bias, the P-N junction emits visual light or infrared light. The emission efficiency of the LED is dependent on the epitaxy material, the ohmic contact electrode, the chip structure, the geometric shape, and so on.

[0011] Display panels display various colors using a mixture of colors such as red, green and blue. Each of the pixels of the display panel includes sub-pixels such as red, green and blue sub-pixels. The color of a particular pixel is determined based on the superimposed color from the sub-pixels. The image formed by the display panel is dependent on the combination formed by each of the pixels.

[0012] In some embodiments, a multi-color LED device integrates at least two micro-LED structures horizontally placed in separate areas within a pixel area on the display panel. In some embodiments, multiple light emitting layers are fabricated by bonding in a stacked structure as a starting structure for the multi-color LED device. Each of the multiple light emitting layers is configured to emit a distinct color. The number of light emitting layers corresponds to the number of LED structures within the pixel area of the display panel. For example, if the multi-color LED device includes two sub-pixels, the number of stacked light emitting layers needed during the multi-color LED fabrication process is two. In another example, if the multi-color LED device includes three sub-pixels, the number of stacked light emitting layers needed during the multi-color LED fabrication process is three. In some embodiments, the multiple stacked LED structures are aligned vertically coaxially, i. e., the multiple LED structures are aligned along the same common central axis.

[0013] In some embodiments, the stacked LED structures allow the light emitted from the bottom LED structure to go through the middle LED structure and the top LED structure, and allow the light emitted from the middle LED structure to go through the top LED

structure. The combined color of the stacked LED structures will be the final emitted color of the single pixel stacked LED device.

[0014] Pitch refers to the distance between the centers of adjacent pixels on a display panel. In some embodiments, the pitch can vary from about 40 microns, to about 20 microns, to about 10 microns, and/or preferably to about 5 microns or below. Many efforts have been made to reduce the pitch. A single pixel area is fixed when the pitch specification is determined.

[0015] Compared to conventional fabrication processes for micro-LED display chips, which rely on inefficient pick and place processes, the micro-LED fabrication processes disclosed herein effectively increases the light emission efficiency and reliability of the micro-LED device fabrication, simplifies the LED pixel device structure and reduces damage to the epitaxial layers of the LED device. For example, the PN junction current density is improved by confining the current through a layer oxidized at the edge or an oxidized ring. In another example, a two-time transfer process is used to fabricate the LED device that has the light emitted out from the p-side of the LED device. In addition, no substrate for the micro-LED structures remain in the final multi-color device so that cross-talk and mismatch can be reduced.

[0016] In addition, since each of the LED light emitting layers is a PN junction, in some embodiments, the relative positions, for example, up (closest to the emitting surface of the LED) and down (closest to a supporting substrate of the LED) positions of the P-type region and N-type region layers, within each of the LED light emitting layers in the stacked structure are not consistent. This allows flexibility and efficiency of the electrode connections within the multi-color LED structure.

[0017] The present disclosure includes, without limitation, the following exemplary embodiments.

[0018] Some exemplary embodiments of the present disclosure include a micro light emitting diode (LED) chip structure. The micro LED chip structure includes: a semiconductor substrate; an electrical contact layer on a surface of the semiconductor substrate; a first type of conductive layer on the semiconductor substrate; an active light emitting layer on the first type of conductive layer; and a second type of conductive layer on

the active light emitting layer. In some embodiments, the thickness of the second-type of conductive layer is smaller than the thickness of the first-type of conductive layer, and the surface of the second-type of conductive layer is obtained after an organic material layer is removed.

[0019] Some exemplary embodiments of the present disclosure include a micro light emitting diode (LED) chip structure. The micro LED chip structure includes: a semiconductor substrate; an electrical contact layer on a surface of the semiconductor substrate; a first type of conductive layer on the semiconductor substrate; an active light emitting layer on the first type of conductive layer; and a second type of conductive layer on the active light emitting layer. In some embodiments, the surface of the second-type of conductive layer is obtained after an organic material layer is removed.

[0020] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the micro LED chip structure further includes a second type of spacer layer between the active light emitting layer and the second type of conductive layer. In some embodiments, the second type of spacer layer is used for forming a PN junction structure with the active light emitting layer and the first type of conductive layer, and the second type of conductive layer includes one or more of second type of conductive transition layers.

[0021] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the first type of conductive layer is an N-type layer, and the second type of conductive layer is a P-type layer.

[0022] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the semiconductor substrate is an integrated circuits (IC) substrate.

[0023] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the electrical contact layer is a metal bonding layer, and the semiconductor substrate and the first type of conductive layer are bonded together through a bonding process.

[0024] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the second type of conductive layer is a P-type GaP layer, and the first type of conductive layer is an N-type GaAs layer.

[0025] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the micro LED chip structure further includes a first type of cladding layer between the first type of conductive layer and the active light emitting layer.

[0026] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the micro LED chip structure further includes an oxide layer within the first type of cladding layer.

[0027] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the micro LED chip structure further includes an oxide layer between the first type of conductive layer and the first type of cladding layer.

[0028] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the micro LED chip structure further includes a second type of cladding layer between the second type of conductive layer and the active light emitting layer.

[0029] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the micro LED chip structure further includes an oxide layer within the second type of cladding layer.

[0030] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the micro LED chip structure further includes an oxide layer between the second type of conductive layer and the second type of cladding layer.

[0031] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the material of the oxide layer is $\text{Al}_x\text{OGa}_{1-x}\text{As}$, and x is greater or equal to 0.9 and less than 1.

[0032] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the material of the first type of cladding layer is AlInP.

[0033] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the second type of cladding layer includes one or more layers of AlInP, $\text{Al}_x\text{Ga}_{1-x}\text{InP}$ (x is greater than 0 and less than 1), and GaInP.

[0034] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the organic material layer is an ultraviolet (UV) curable bonding layer.

[0035] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the ratio of a thickness of the second type of conductive layer to a thickness of the first type of conductive layer is 0.025 to 100.

[0036] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the ratio of a thickness of the second type of conductive layer to a thickness of the first type of conductive layer is 1.5 to 2.

[0037] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the micro LED chip structure further includes a second type of cladding layer between the second type of conductive layer and the active light emitting layer, wherein the second type of conductive layer includes a second type of conductive transition layer.

[0038] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the ratio of the thickness of the second type of cladding layer to the thickness of the second type of conductive transition layer is 0.02 to 120.

[0039] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the ratio of the thickness of the second type of cladding layer to the thickness of the second type of conductive transition layer is 1 to 2.5.

[0040] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the second type of conductive layer comprises

sequentially a lower second type of conductive transition layer, a middle second type of conductive transition layer, and an upper second type of conductive transition layer in a direction from the semiconductor substrate to the first type of conductive layer.

[0041] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the conductivity of the lower second type of conductive transition layer is less than that of the middle second type of conductive transition layer, and the conductivity of the middle second type of conductive transition layer is less than the upper second type of conductive transition layer.

[0042] In some exemplary embodiments or any combination of exemplary embodiments of the micro LED chip structure, the second type of cladding layer includes one or more layers of AlInP, and $\text{Al}_x\text{Ga}_{1-x}\text{InP}$ (x is greater than or equal to 0 and less than or equal to 1).

[0043] Some exemplary embodiments of the present disclosure include an epitaxial structure for a micro light emitting diode (LED). The epitaxial structure for the micro LED includes: a semiconductor substrate; an electrical conductive layer of a first conductivity type on the semiconductor substrate; a cladding layer of the first conductivity type on the electrical conductive layer of the first conductivity type; a first oxide layer within the cladding layer of the first conductivity type; an active light emitting layer on the cladding layer of the first conductivity type; a cladding layer of a second conductivity type on the active light emitting layer; and an electrical conductive layer of the second conductivity type on the cladding layer of the second conductivity type.

[0044] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the epitaxial structure for the micro LED further includes a second oxide layer within the cladding layer of the second conductivity type.

[0045] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the epitaxial structure for the micro LED further includes a second oxide layer between the cladding layer of the second conductivity type and the electrical conductive layer of the second conductivity type.

[0046] Some exemplary embodiments of the present disclosure include an epitaxial structure for a micro light emitting diode (LED). The epitaxial structure for the micro LED includes: a semiconductor substrate; an electrical conductive layer of a first conductivity type on the semiconductor substrate; a cladding layer of the first conductivity type on the electrical conductive layer of the first conductivity type; a first oxide layer between the electrical conductive layer of the first conductivity type and the cladding layer of the first conductivity type; an active light emitting layer on the cladding layer of the first conductivity type; a cladding layer of a second conductivity type on the active light emitting layer; and an electrical conductive layer of the second conductivity type on the cladding layer of the second conductivity type.

[0047] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the epitaxial structure for the micro LED further includes a second oxide layer between the cladding layer of the second conductivity type and the electrical conductive layer of the second conductivity type.

[0048] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the epitaxial structure for the micro LED further includes a second oxide layer within the cladding layer of the second conductivity type.

[0049] Some exemplary embodiments of the present disclosure include an epitaxial structure for a micro light emitting diode (LED). The epitaxial structure for the micro LED includes: a semiconductor substrate; an electrical conductive layer of a first conductivity type on the semiconductor substrate; a cladding layer of the first conductivity type on the electrical conductive layer of the first conductivity type; an active light emitting layer on the cladding layer of the first conductivity type; a cladding layer of a second conductivity type on the active light emitting layer; a first oxide layer within the cladding layer of the second conductivity type; and an electrical conductive layer of the second conductivity type on the cladding layer of the second conductivity type.

[0050] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the epitaxial structure for the

micro LED further includes a second oxide layer within the cladding layer of the first conductivity type.

[0051] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the epitaxial structure for the micro LED further includes a second oxide layer between the cladding layer of the first conductivity type and the electrical conductive layer of the first conductivity type.

[0052] Some exemplary embodiments of the present disclosure include an epitaxial structure for a micro light emitting diode (LED). The epitaxial structure for the micro LED includes: a semiconductor substrate; an electrical conductive layer of a first conductivity type on the semiconductor substrate; a cladding layer of the first conductivity type on the electrical conductive layer of the first conductivity type; an active light emitting layer on the cladding layer of the first conductivity type; a cladding layer of a second conductivity type on the active light emitting layer; an electrical conductive layer of the second conductivity type on the cladding layer of the second conductivity type; and a first oxide layer between the cladding layer of the second conductivity type and the electrical conductive layer of the second conductivity type.

[0053] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the epitaxial structure for the micro LED further includes a second oxide layer between the cladding layer of the first conductivity type and the electrical conductive layer of the first conductivity type.

[0054] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the epitaxial structure for the micro LED further includes a second oxide layer within the cladding layer of the first conductivity type.

[0055] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the oxide layer is formed as an oxide ring from an oxide layer precursor $\text{Al}_x\text{Ga}_{1-x}\text{As}$, and x is greater or equal to 0.9 and less than 1.

[0056] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the cladding layer of the first conductivity type includes one or more layers.

[0057] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the cladding layer of the second conductivity type includes one or more layers.

[0058] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the epitaxial structure for the micro LED further includes between the semiconductor substrate and the electrical conductive layer of the first conductivity type, sequentially a buffer layer of the first conductivity type and an etch-stop layer of the first conductivity type in a direction from the semiconductor substrate to the electrical conductive layer of the first conductivity type.

[0059] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the epitaxial structure for the micro LED further includes a spacer layer of the first conductivity type located on a bottom of the active light emitting layer, and a spacer layer of the second conductivity type located on a top of the active light emitting layer.

[0060] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the electrical conductive layer of the second conductivity type comprises one or more conductive transition layers.

[0061] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the electrical conductive layer of the second conductivity type comprises sequentially a lower conductive transition layer of the second conductivity type, a middle conductive transition layer of the second conductivity type, and an upper conductive transition layer of the second conductivity type in a direction from the semiconductor substrate to the electrical conductive layer of the first conductivity type.

[0062] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the conductivity of the lower

conductive transition layer of the second conductivity type is less than that of the middle conductive transition layer of the second conductivity type, and the conductivity of the middle conductive transition layer of the second conductivity type is less than the upper conductive transition layer of the second conductivity type.

[0063] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the material of the first oxide layer is $\text{Al}_x\text{OGa}_{1-x}\text{As}$, and x is greater or equal to 0.9 and less than 1.

[0064] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the material of the cladding layer of the first conductivity type is AlInP .

[0065] In some exemplary embodiments or any combination of exemplary embodiments of the epitaxial structure for the micro LED, the material of the cladding layer of the second conductivity type includes one or more layers of AlInP , and $\text{Al}_x\text{Ga}_{1-x}\text{InP}$ (x is greater than or equal to 0 and less than or equal to 1).

[0066] The compact design of the LED devices and systems disclosed herein utilizes the bonding layers and introduces intermediate substrate(s), thereby reducing the complexity of the fabrication steps and increase the overall performance to cost ratio of the LED display systems. Furthermore, the fabrication of the LED display systems can reliably and efficiently form the LED structure patterns without retaining extra substrates. Thus, implementation of the multi-color LED display systems can satisfy the rigorous display requirements for AR and VR, heads-up displays (HUD), mobile device displays, wearable device displays, high definition small projectors, and automotive displays compared with the use of the conventional LEDs.

[0067] Note that the various embodiments described above can be combined with any other embodiments described herein. The features and advantages described in the specification are not all inclusive and, in particular, many additional features and advantages will be apparent to one of ordinary skill in the art in view of the drawings, specification, and claims. Moreover, it should be noted that the language used in the specification has been principally selected for readability and instructional purposes, and may not have been selected to delineate or circumscribe the inventive subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0068] So that the present disclosure can be understood in greater detail, a more particular description may be had by reference to the features of various embodiments, some of which are illustrated in the appended drawings. The appended drawings, however, merely illustrate pertinent features of the present disclosure and are therefore not to be considered limiting, for the description may admit to other effective features.

[0069] Figure 1 is a cross-sectional view of an LED structure, in accordance with some embodiments.

[0070] Figure 2A is a cross-sectional view of an LED structure with an oxide precursor layer within the n-cladding layer, in accordance with some embodiments.

[0071] Figure 2B is a cross-sectional view of an LED structure with an oxide layer within the n-cladding layer, in accordance with some embodiments.

[0072] Figure 3A is a cross-sectional view of an LED structure with an oxide precursor layer between the n^+ -contact layer and the n-cladding layer, in accordance with some embodiments.

[0073] Figure 3B is a cross-sectional view of an LED structure with an oxide layer between the n^+ -contact layer and the n-cladding layer, in accordance with some embodiments.

[0074] Figure 4A is a cross-sectional view of an LED structure with an oxide precursor layer within the p-cladding layer, in accordance with some embodiments.

[0075] Figure 4B is a cross-sectional view of an LED structure with an oxide layer within the p-cladding layer, in accordance with some embodiments.

[0076] Figure 5A is a cross-sectional view of an LED structure with an oxide precursor layer between the p-cladding layer and the p-transition layer 120, in accordance with some embodiments.

[0077] Figure 5B is a cross-sectional view of an LED structure with an oxide layer between the p-cladding layer and the p-transition layer, in accordance with some embodiments.

[0078] Figures 6A-6D illustrate a fabrication process utilizing a one-time transfer process to form an LED structure with a supporting substrate with integrated circuits, in accordance with some embodiments.

[0079] Figures 7A-7H illustrate a fabrication process utilizing a two-time transfer process to form an LED structure with a supporting substrate with integrated circuits, in accordance with some embodiments.

[0080] Figure 8 is a top view of a micro LED display panel, in accordance with some embodiments.

[0081] In accordance with common practice, the various features illustrated in the drawings may not be drawn to scale. Accordingly, the dimensions of the various features may be arbitrarily expanded or reduced for clarity. In addition, some of the drawings may not depict all of the components of a given system, method or device. Finally, like reference numerals may be used to denote like features throughout the specification and figures.

DETAILED DESCRIPTION

[0082] Numerous details are described herein in order to provide a thorough understanding of the example embodiments illustrated in the accompanying drawings. However, some embodiments may be practiced without many of the specific details, and the scope of the claims is only limited by those features and aspects specifically recited in the claims. Furthermore, well-known processes, components, and materials have not been described in exhaustive detail so as not to unnecessarily obscure pertinent aspects of the embodiments described herein.

[0083] Embodiments consistent with the disclosure include a display panel, including a substrate with an array of pixel driver circuits, an array of LEDs with structures described below, formed over the substrate, and methods of making the display panel. The display

panels having a high light extraction efficiency are capable of overcoming the drawbacks of the conventional display systems.

[0084] Generally, at least red, green and blue colors are superimposed to reproduce a broad array of colors. In some instances, to include at least red, green and blue colors within a pixel area, separate monochromatic LED structures are fabricated at different non-overlapping zones within the pixel area.

[0085] In some embodiments, three LEDs, are formed in a stacked structure, for example, starting from a base layer formed by a substrate, the green LED is directly on top of the red LED, and the blue LED is directly on top of the green LED. In some embodiments, the light emitted from the red LED is able to propagate through the green LED and then through the blue LED to be emitted out of the tri-color LED device. In some embodiments, the light emitted from the green LED is able to propagate through the blue LED to be emitted out of the tri-color LED device. In other embodiments, the color of the monochromatic LEDs are not limited to red, green and blue and can be any other visible or invisible colors. In other embodiments, the monochromatic LEDs' order from bottom (closest to the substrate) to top (closest to the emitting surface of the LED) are not limited to red, green and blue colors.

[0086] In some embodiments, a single pixel area on a display panel includes at least one single pixel light emitting device, such as an LED or a micro-LED, or an OLED, and light is emitted from the LED. The LED has a top surface and a bottom surface. In some embodiments, the diameter or width of the top surface of the LED is in the range of $1\mu\text{m}$ – $8\mu\text{m}$, and the diameter or width of the bottom surface of the LED is in the range of $3\mu\text{m}$ – $10\mu\text{m}$. In some embodiments, the diameter or width of the top surface of the LED is in the range of $8\mu\text{m}$ – $25\mu\text{m}$, and the diameter or width of the bottom surface of the LED is in the range of $10\mu\text{m}$ – $35\mu\text{m}$. In some embodiments, the height of the LED is in the range of 1 – $10\mu\text{m}$. In some embodiments, the height of the LED is about $1.3\mu\text{m}$. In some embodiments, the diameter or width of the top surface of the LED is equal to or less than the diameter or width of the bottom surface of the LED.

[0087] In some embodiments, a display panel includes an array of single pixel LEDs. In some embodiments, the distance between center axes of the two adjacent LEDs is in the range of $1\mu\text{m}$ - $10\mu\text{m}$. In some embodiments, the distance between center axes of the two

adjacent LEDs may vary from about 40 μm , to about 20 μm , to about 10 μm , and/or to about 5 μm or below. In some embodiments, sizes of the mesas and distances between the LEDs may depend on the resolution of the display. For example, for a display panel with 5000 Pixels Per Inch (PPI), the diameter or width of the top surface of the LED is 1.5 μm and the diameter or width of the bottom surface of the LED is 2.7 μm . In some embodiments, the distance between the closest bottom edges of two adjacent LEDs may be in the range of 1 μm -10 μm . In some embodiments, the distance between the closest bottom edges of two adjacent LEDs is 2.3 μm .

[0088] Figure 1 is a cross-sectional view of an LED structure 100, in accordance with some embodiments. In some embodiments, the LED structure 100 is for forming one of the three color LED devices within a pixel area in a display panel. In some embodiments, the three color LED devices include three color LED structures, such as 100. Each of the three color LED structures forms a sub-pixel within the single pixel area. In some embodiments, the three color LED structures each emit a single color, for example, blue, green, and a red. In some embodiments, the colors emitted by the three color LED structures are different and distinct. In some embodiments, the color emitted by the LED structure 100 is red.

[0089] In some embodiments, a display panel includes a plurality of pixels, such as millions of pixels, and each pixel includes a set of three color LED devices. In some embodiments, the color LED devices can be micro LEDs. Micro LEDs typically have a lateral dimension of 50 microns (μm) or less, and can have lateral dimensions less than 10 μm and even just a few μm .

[0090] In some embodiments, the LED structure 100 includes a substrate 102. For convenience, "up" is used to mean away from the substrate 102, "down" means toward the substrate 102, and other directional terms such as top, bottom, above, below, under, beneath, etc. are interpreted accordingly.

[0091] In general, an LED color light emitting layer includes a PN junction with a p-type region/layer and an n-type region/layers, and an active layer between the p-type region/layer and n-type region/layer.

[0092] In some embodiments, the substrate 102 is made of GaAs. In some embodiments, the thickness of the substrate 102 is about 350 μm . In some embodiments, the

thickness of the substrate 102 is about 325 μm to 375 μm . In some embodiments, the substrate 102 is doped with Si at a carrier concentration of 0.4×10^{18} to $4.0 \times 10^{18} \text{ cm}^{-3}$.

[0093] Although some features are described herein with the term “layer”, it should be understood that such features are not limited to a single layer but may include a plurality of sublayers. In some instance, a “structure” can take the form of a “layer”.

[0094] In some embodiments, the layers of the LED structure are formed from an epitaxial process, such as metal organic chemical vapor deposition (MOCVD).

[0095] In some embodiments, an n-buffer layer 104 is formed above the substrate 102. A buffer layer is formed before the subsequent layers are formed to reduce lattice growth mismatch in an epitaxial process. In some embodiments, the n-buffer layer 104 is formed by GaAs. In some embodiments, the thickness of the n-buffer layer 104 is about 200 nm. In some embodiments, the thickness of the n-buffer layer 104 is about 190 nm to 210 nm. In some embodiments, the n-buffer layer 104 is doped with Si at a carrier concentration of 1.0×10^{18} to $5.0 \times 10^{18} \text{ cm}^{-3}$.

[0096] In some embodiments, an n-etch stop layer 106 is formed above the n-buffer layer 104. The n-etch stop layer 106 is used in a subsequent process to prevent the etching of an n^+ -contact layer 108 in a subsequent etching process to remove the substrate 102. The n-etch stop layer 106 is not reactive to the selective etching solution for removing GaAs. In some embodiments, the n-etch stop layer 106 is formed by $\text{Al}_{0.15}\text{GaInP}$. In some embodiments, the thickness of the n-etch stop layer 106 is about 200 nm. In some embodiments, the thickness of the n-etch stop layer 106 is about 190 nm to 210 nm. In some embodiments, the n-etch stop layer 106 is doped with Si at a carrier concentration of 1.0×10^{18} to $5.0 \times 10^{18} \text{ cm}^{-3}$.

[0097] In some embodiments, the n^+ -contact layer 108 is formed above the n-etch stop layer 106. The n^+ -contact layer 108 is an n-type conductive layer. In some embodiments, the n^+ -contact layer 108 is formed by GaAs. In some embodiments, the thickness of the n^+ -contact layer 108 is about 5 nm to 200 nm. In some embodiments, the n^+ -contact layer 108 is doped with Si at a carrier concentration of 1.0×10^{18} to $5.0 \times 10^{18} \text{ cm}^{-3}$.

[0098] In some embodiments, an n-cladding layer 110 is formed above the n⁺-contact layer 108. The n-cladding layer 110 is used for providing and confinement of the n-type carriers in a PN junction. In some embodiments, the n-cladding layer 110 is formed by AlInP. In some embodiments, the thickness of the n-cladding layer 110 is about 100 nm to 5 μm. In some embodiments, the n-cladding layer 110 is doped with Si at a carrier concentration of 1.0×10^{18} to $5.0 \times 10^{18} \text{ cm}^{-3}$.

[0099] In some embodiments, an n-spacer layer 112 is formed above the n-cladding layer 110 and below an active light emitting layer 114. The n-spacer layer 112 is used as barrier layer between the n-cladding layer 110 and the active light emitting layer 114. In some embodiments, the n-spacer layer 112 is formed by Al_{0.8}GaInP. In some embodiments, the thickness of the n-spacer layer 112 is about 10 nm to 200 nm.

[00100] In some embodiments, the active light emitting layer 114 is formed above n-spacer layer 112. In some embodiments, the active light emitting layer 114 is formed as a multiple quantum well structure. In some embodiments, the active light emitting layer 114 is formed of alternative layers of Al_xInGaP (x is from 0 to 0.5) and Al_{0.8}InGaP, for example, a first layer of Al_xInGaP is formed above a first layer of Al_{0.8}InGaP, a second layer of Al_{0.8}InGaP is formed on the first layer of Al_xInGaP, and a second layer of Al_xInGaP is formed on the second layer of Al_{0.8}InGaP. In some embodiments, the active light emitting layer 114 is composed of 1 to 30 pairs of layers of Al_xInGaP (x is from 0 to 0.5) and Al_{0.8}InGaP. In some embodiments, the single layer of Al_xInGaP (x is from 0 to 0.5) is about 3.5 nm. In some embodiments, the single layer of Al_xInGaP (x is from 0 to 0.5) is about 1 to 30 nm. In some embodiments, the single layer of Al_{0.8}InGaP is about 6.5 nm. In some embodiments, the single layer of Al_{0.8}InGaP is about 1 to 30 nm.

[00101] In some embodiments, the active LED light emitting layer 114, includes many epitaxial sub-layers with different compositions. Examples of the active LED light emitting layer includes III-V nitride, III-V arsenide, III-V phosphide, and III-V antimonide epitaxial structures. Examples of active LED light emitting layers include GaN based UV/blue/green light emitting layers, AlInGaP based red/orange light emitting layers, and GaAs or InP based infrared (IR) light emitting layers.

[00102] In some embodiments, a p-spacer layer 116 is formed above the active light emitting layer 114. The p-spacer layer 116 is used as barrier layer between a p-cladding layer 118 and the active light emitting layer 114. In some embodiments, the p-spacer layer 116 is formed by $\text{Al}_{0.8}\text{GaInP}$. In some embodiments, the thickness of the p-spacer layer 116 is about 10 nm to 200 nm.

[00103] In some embodiments, the p-cladding layer 118 is formed above the p-spacer layer 116. The p-cladding layer 118 is used for providing and confinement of the p-type carriers in a PN junction. In some embodiments, the p-cladding layer 118 is formed by one or more layers composed of AlInP , $\text{Al}_x\text{Ga}_y\text{InP}$ (x changes from 1 to 0.9 and y changes from 0 to 1), and $\text{Al}_{0.5}\text{GaInP}$. For example, the p-cladding layer 118 is formed by three layers of AlInP , AlInP , and $\text{Al}_{0.5}\text{GaInP}$ from bottom to top. In another example, the p-cladding layer 118 is formed by three layers of AlInP , $\text{Al}_{0.9}\text{GaInP}$, and $\text{Al}_{0.5}\text{GaInP}$ from bottom to top. Yet in another example, the p-cladding layer 118 is formed by a bottom layer composed of AlInP , a top layer composed of $\text{Al}_x\text{Ga}_{1-x}\text{InP}$ (from bottom to up, the layer composition gradually changes, i.e. x changes from 0 to 1). In some examples, the p-cladding layer 118 is formed by multiple groups of layers of AlInP , and $\text{Al}_x\text{Ga}_{1-x}\text{InP}$ (x changes from 0 to 1), periodically. In some embodiments, the thickness of the p-cladding layer 118 is about 100 nm to 5 μm . In some embodiments, the p-cladding layer 118 is doped with Mg at a carrier concentration of 1.0×10^{17} to $9.0 \times 10^{17} \text{ cm}^{-3}$.

[00104] In some embodiments, a p-transition layer 120 is formed above the p-cladding layer 118. In some embodiments, the p-transition layer 120 is formed by $\text{Al}_{0.17}\text{GaInP}$. In some embodiments, the thickness of the p-transition layer 120 is about 20 nm to 100 nm. In some embodiments, the p-transition layer 120 is doped with Mg at a carrier concentration of greater than $1.0 \times 10^{18} \text{ cm}^{-3}$ and less than $2.0 \times 10^{18} \text{ cm}^{-3}$.

[00105] In some embodiments, a p^+ -transition layer 122 is formed above the p-transition layer 120. In some embodiments, the p^+ -transition layer 122 is formed by GaP . In some embodiments, the thickness of the p^+ -transition layer 122 is about 10 nm to 5 μm . In some embodiments, the p^+ -transition layer 122 is doped with Mg at a carrier concentration of 2.0×10^{18} to $9.0 \times 10^{18} \text{ cm}^{-3}$. The doping concentration of the p^+ -transition layer 122 is higher than the doping concentration of the p-transition layer 120.

[00106] In some embodiments, a p^{++} -transition layer 124 is formed above the p^{+} -transition layer 122. In some embodiments, the p^{++} -transition layer 124 is formed by GaP. In some embodiments, the thickness of the p^{++} -transition layer 124 is about 10 nm to 30 nm. In some embodiments, the p^{++} -transition layer 124 is doped with Carbon at a carrier concentration of 1.0×10^{19} to $9.0 \times 10^{19} \text{ cm}^{-3}$. The doping concentration of the p^{++} -transition layer 124 is higher than the doping concentration of the p^{+} -transition layer 122. The gradual elevation of the doping concentration can stabilize the growth of the p-transition layers and prevent or ease defect and stress formed from the lattice change.

[00107] The p-type conductive layers include layers such as the p-transition layer 120, p^{+} -transition layer 122, and p^{++} -transition layer 124.

[00108] Figure 2A is a cross-sectional view of an LED structure 200 with an oxide precursor layer 202 within the n-cladding layer 110, in accordance with some embodiments. In some embodiments, the LED structure 200 includes a layer 202 composed of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1). In some embodiments, the thickness of the layer 202 is about 1 nm to 100 nm. The rest of the structure of the LED structure is similar or the same as all the layers of the LED structure 100 as described in Figure 1. In some embodiments, the layer 202 is located within the n-cladding layer 110, for example, in between a first layer 204 within the n-cladding layer 110 and a second layer 206 within the n-cladding layer 110. In some embodiments, the layer 202 is used as a pre-cursor before a subsequent oxidation process. In some embodiments, the layer 202 is doped with Si at a carrier concentration of 1.0×10^{17} to $9.0 \times 10^{18} \text{ cm}^{-3}$.

[00109] Figure 2B is a cross-sectional view of an LED structure 208 with an oxide layer 210 within the n-cladding layer 110, in accordance with some embodiments. In some embodiments, the LED structure 208 includes an oxide layer 210. In some embodiments, the oxide layer 210 is composed of $\text{Al}_x\text{OGa}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1). The rest of the structure of the LED structure 208 is similar or the same as all the layers of the LED structure 100 as described in Figure 1. In some embodiments, the layer 210 is located within the n-cladding layer 110, for example, in between a first layer 204 within the n-cladding layer 110 and a second layer 206 within the n-cladding layer 110. In some

embodiments, the oxide layer 210 is formed from an oxidation process after all the layers of the LED structure 200 as described in Figure 2A is formed.

[00110] In some embodiments, a subsequent oxidation process is applied after all the epitaxial layers of the LED structure 200 are formed. In some embodiments, the oxidation process is a wet oxidation. In some embodiments, the wet oxidation is conducted in a wet oxygen oxidation furnace. In one example, the wet oxygen oxidation furnace is VF3000 VCSEL furnace from Koyo Thermo Systems. In some embodiments, a nitrogen gas is used as carrier gas at a flow rate of 1 liter per minute. Oxygen is obtained from the water heated at around 98 °C in the wet oxygen oxidation furnace. In some embodiments, the wet oxidation uses an ambient temperature from 380 °C to 500 °C, and a time of equal to or under 2 hours. The oxidation is a controlled oxidation on the side wall of the LED structure 200. Since all the other layers in the LED structure 200 are not reactive to the oxidation process, the side wall of the layer 202 is oxidized. The oxidation process is stopped when the desired oxidation depth of the side wall of the layer 202 is reached. In some embodiments, the preferred oxidation depth of the side wall of the layer 202 is around one fourth of the lateral diameter of the layer 202. In some embodiments, the preferred oxidation depth of the side wall of the layer 202 is around one fifth of the lateral diameter of the layer 202. In some embodiments, the preferred oxidation depth of the side wall of the layer 202 is around one third of the lateral diameter of the layer 202.

[00111] In some embodiments, after the oxidation process, the oxide layer 210 composed of $\text{Al}_x\text{OGa}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1) is formed from the original layer 202 composed of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1). In a preferred embodiment, the oxide layer 210 has $\text{Al}_x\text{OGa}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1) formed around the edge, for example, 212 and 214, of the layer of 210, i.e., toward the side of the LED structure 208, while the center of the layer 210 remains less oxidized /or remains not oxidized. In some embodiments, all the other layers in the LED structure 200/208 other than the original layer 202 composed of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1) are resistant to the oxidation process and remain unoxidized.

[00112] Non-radiative electron-hole pair recombination at the side surface, especially, defect sites, of the n-cladding layer 110 may cause additional energy loss, such as heat, and reduce the light emission efficiency. The introduction of the oxide layer 210 within the n-cladding layer 110 can reduce the surface non-radiative recombination and improve the light emission efficiency of the LED device. Specifically, when the oxidation mostly happens at the edge of the layer 210, the formed oxide layer can reduce or eliminate the non-radiative recombination at the side surfaces or edge, such as, locations 212 and 214, around the layer 210. The main current of an LED is in a vertical direction and there are some current diffusions to the side of the LED in the electric current flowing process. In some embodiments, when the oxidation mostly happens at the edge of the layer 210, the formed oxide layer can reduce the lateral diffusion of the electric current to the edge, and confine the electric current to the central portion of the LED device formed from the LED structure 208, therefore, increasing the effective electric current density and improving the LED light emission efficiency. In some embodiments, the light emission efficiency is at least 20%. In some embodiments, the light emission efficiency is at least 30%. In some embodiments, the light emission efficiency is at least 40%. In some embodiments, the light emission efficiency is at least 50%. In some embodiments, the light emission efficiency is at least 60%.

[00113] Figure 3A is a cross-sectional view of an LED structure 300 with an oxide precursor layer 302 between the n⁺-contact layer 108 and the n-cladding layer 110, in accordance with some embodiments. In some embodiments, the LED structure 300 includes a layer 302 composed of Al_xGa_{1-x}As (x is greater than or equal to 0.9 and less than 1). In some embodiments, the thickness of the layer 302 is about 1 nm to 100 nm. The rest of the structure of the LED structure is similar or the same as all the layers of the LED structure 100 as described in Figure 1. In some embodiments, the layer 302 is located between the n⁺-contact layer 108 and the n-cladding layer 110. In some embodiments, the layer 302 is used as a pre-cursor before a subsequent oxidation process. In some embodiments, the layer 302 is doped with Si at a carrier concentration of 1.0×10^{17} to $9.0 \times 10^{18} \text{ cm}^{-3}$.

[00114] Figure 3B is a cross-sectional view of an LED structure 308 with an oxide layer 310 between the n⁺-contact layer 108 and the n-cladding layer 110, in accordance with some embodiments. In some embodiments, the LED structure 308 includes an oxide layer 310. In some embodiments, the oxide layer 310 is composed of Al_xOGa_{1-x}As (x is greater

than or equal to 0.9 and less than 1). The rest of the structure of the LED structure 308 is similar or the same as all the layers of the LED structure 100 as described in Figure 1. In some embodiments, the layer 310 is located between the n^+ -contact layer 108 and the n-cladding layer 110. In some embodiments, the oxide layer 310 is formed from an oxidation process after all the layers of the LED structure 300 as described in Figure 3A is formed.

[00115] In some embodiments, a subsequent oxidation process is applied after all the epitaxial layers of the LED structure 300 are formed. In some embodiments, the oxidation process is a wet oxidation. In some embodiments, the wet oxidation is conducted in a wet oxygen oxidation furnace. In one example, the wet oxygen oxidation furnace is VF3000 VCSEL furnace from Koyo Thermo Systems. In some embodiments, a nitrogen gas is used as carrier gas at a flow rate of 1 liter per minute. Oxygen is obtained from the water heated at around 98 °C in the wet oxygen oxidation furnace. In some embodiments, the wet oxidation uses an ambient temperature from 380 °C to 500 °C, and a time of equal to or under 2 hours. The oxidation is a controlled oxidation on the side wall of the LED structure 300. Since all the other layers in the LED structure 300 are not reactive to the oxidation process, the side wall of the layer 302 is oxidized. The oxidation process is stopped when the desired oxidation depth of the side wall of the layer 302 is reached. In some embodiments, the preferred oxidation depth of the side wall of the layer 302 is around one fourth of the lateral diameter of the layer 302. In some embodiments, the preferred oxidation depth of the side wall of the layer 302 is around one fifth of the lateral diameter of the layer 302. In some embodiments, the preferred oxidation depth of the side wall of the layer 302 is around one third of the lateral diameter of the layer 302.

[00116] In some embodiments, after the oxidation process, the oxide layer 310 composed of $Al_xOGa_{1-x}As$ (x is greater than or equal to 0.9 and less than 1) is formed from the original layer 302 composed of $Al_xGa_{1-x}As$ (x is greater than or equal to 0.9 and less than 1). In a preferred embodiment, the oxide layer 310 has $Al_xOGa_{1-x}As$ (x is greater than or equal to 0.9 and less than 1) formed around the edge of the layer of 310, for example, 312 and 314, i.e., toward the side of the LED structure 308, while the center of the layer 310 remains less oxidized /or remains not oxidized. In some embodiments, all the other layers in the LED structure 300/308 other than the original layer 302 composed of $Al_xGa_{1-x}As$ (x is greater

than or equal to 0.9 and less than 1) are resistant to the oxidation process and remain unoxidized.

[00117] Non-radiative electron-hole pair recombination at the side surfaces, especially, defect sites, of the n^+ -contact layer 108 and the n-cladding layer 110 may cause additional energy loss, such as heat, and reduce the light emission efficiency. The introduction of the oxide layer 310 between the n^+ -contact layer 108 and the n-cladding layer 110 can reduce the surface non-radiative recombination and improve the light emission efficiency of the LED device. Specifically, when the oxidation mostly happens at the edge of the layer 310, the formed oxide layer can reduce or eliminate the non-radiative recombination at the side surfaces or edge, such as, locations 312 and 314, around the layer 310. The main current of an LED is in a vertical direction and there are some current diffusions to the side of the LED in the electric current flowing process. In some embodiments, when the oxidation mostly happens at the edge of the layer 310, the formed oxide layer can reduce the lateral diffusion of the electric current to the edge, and confine the electric current to the central portion of the LED device formed from the LED structure 308, therefore, increasing the effective electric current density and improving the LED light emission efficiency. In some embodiments, the light emission efficiency is at least 20%. In some embodiments, the light emission efficiency is at least 30%. In some embodiments, the light emission efficiency is at least 40%. In some embodiments, the light emission efficiency is at least 50%. In some embodiments, the light emission efficiency is at least 60%.

[00118] Figure 4A is a cross-sectional view of an LED structure 400 with an oxide precursor layer 402 within the p-cladding layer 118, in accordance with some embodiments. In some embodiments, the LED structure 400 includes a layer 402 composed of $Al_xGa_{1-x}As$ (x is greater than or equal to 0.9 and less than 1). In some embodiments, the thickness of the layer 402 is about 1 nm to 100 nm. The rest of the structure of the LED structure is similar or the same as all the layers of the LED structure 100 as described in Figure 1. In some embodiments, the layer 402 is located within the p-cladding layer 118, for example, in between a first layer 404 within the p-cladding layer 118 and a second layer 406 within the p-cladding layer 118. In some embodiments, the layer 402 is used as a pre-cursor before a subsequent oxidation process. In some embodiments, the layer 402 is doped with Mg at a carrier concentration of 1.0×10^{17} to $9.0 \times 10^{18} \text{ cm}^{-3}$.

[00119] Figure 4B is a cross-sectional view of an LED structure 408 with an oxide layer 410 within the p-cladding layer 118, in accordance with some embodiments. In some embodiments, the LED structure 408 includes an oxide layer 410. In some embodiments, the oxide layer 410 is composed of $\text{Al}_x\text{OGa}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1). The rest of the structure of the LED structure 408 is similar or the same as all the layers of the LED structure 100 as described in Figure 1. In some embodiments, the layer 410 is located within the p-cladding layer 118, for example, in between a first layer 404 within the p-cladding layer 118 and a second layer 406 within the p-cladding layer 118. In some embodiments, the oxide layer 410 is formed from an oxidation process after all the layers of the LED structure 400 as described in Figure 4A is formed.

[00120] In some embodiments, a subsequent oxidation process is applied after all the epitaxial layers of the LED structure 400 are formed. In some embodiments, the oxidation process is a wet oxidation. In some embodiments, the wet oxidation is conducted in a wet oxygen oxidation furnace. In one example, the wet oxygen oxidation furnace is VF3000 VCSEL furnace from Koyo Thermo Systems. In some embodiments, a nitrogen gas is used as carrier gas at a flow rate of 1 liter per minute. Oxygen is obtained from the water heated at around 98 °C in the wet oxygen oxidation furnace. In some embodiments, the wet oxidation uses an ambient temperature from 380 °C to 500 °C, and a time of equal to or under 2 hours. The oxidation is a controlled oxidation on the side wall of the LED structure 400. Since all the other layers in the LED structure 400 are not reactive to the oxidation process, the side wall of the layer 402 is oxidized. The oxidation process is stopped when the desired oxidation depth of the side wall of the layer 402 is reached. In some embodiments, the preferred oxidation depth of the side wall of the layer 402 is around one fourth of the lateral diameter of the layer 402. In some embodiments, the preferred oxidation depth of the side wall of the layer 402 is around one fifth of the lateral diameter of the layer 402. In some embodiments, the preferred oxidation depth of the side wall of the layer 402 is around one third of the lateral diameter of the layer 402.

[00121] In some embodiments, after the oxidation process, the oxide layer 410 composed of $\text{Al}_x\text{OGa}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1) is formed from the original layer 402 composed of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1). In a preferred embodiment, the oxide layer 410 has $\text{Al}_x\text{OGa}_{1-x}\text{As}$ (x is greater than or

equal to 0.9 and less than 1) formed around the edge, for example, 412 and 414, of the layer of 410, i.e., toward the side of the LED structure 408, while the center of the layer 410 remains less oxidized /or remains not oxidized. In some embodiments, all the other layers in the LED structure 400/408 other than the original layer 402 composed of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1) are resistant to the oxidation process and remain unoxidized.

[00122] Non-radiative electron-hole pair recombination at the side surface, especially, defect sites, of the p-cladding layer 118 may cause additional energy loss, such as heat, and reduce the light emission efficiency. The introduction of the oxide layer 410 within the p-cladding layer 118 can reduce the surface non-radiative recombination and improve the light emission efficiency of the LED device. Specifically, when the oxidation mostly happens at the edge of the layer 410, the formed oxide layer can reduce or eliminate the non-radiative recombination at the side surfaces or edge, such as, locations 412 and 414, around the layer 410. The main current of an LED is in a vertical direction and there are some current diffusions to the side of the LED in the electric current flowing process. In some embodiments, when the oxidation mostly happens at the edge of the layer 410, the formed oxide layer can reduce the lateral diffusion of the electric current to the edge, and confine the electric current to the central portion of the LED device formed from the LED structure 408, therefore, increasing the effective electric current density and improving the LED light emission efficiency. In some embodiments, the light emission efficiency is at least 20%. In some embodiments, the light emission efficiency is at least 30%. In some embodiments, the light emission efficiency is at least 40%. In some embodiments, the light emission efficiency is at least 50%. In some embodiments, the light emission efficiency is at least 60%.

[00123] Figure 5A is a cross-sectional view of an LED structure 500 with an oxide precursor layer 502 between the p-cladding layer 118 and the p-transition layer 120, in accordance with some embodiments. In some embodiments, the LED structure 500 includes a layer 502 composed of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1). In some embodiments, the thickness of the layer 502 is about 1 nm to 100 nm. The rest of the structure of the LED structure is similar or the same as all the layers of the LED structure 100 as described in Figure 1. In some embodiments, the layer 502 is located between the p-cladding layer 118 and the p-transition layer 120. In some embodiments, the layer 502 is

used as a pre-cursor before a subsequent oxidation process. In some embodiments, the layer 502 is doped with Mg at a carrier concentration of 1.0×10^{17} to $9.0 \times 10^{18} \text{ cm}^{-3}$.

[00124] Figure 5B is a cross-sectional view of an LED structure 508 with an oxide layer between the p-cladding layer 118 and the p-transition layer 120, in accordance with some embodiments. In some embodiments, the LED structure 508 includes an oxide layer 510. In some embodiments, the oxide layer 510 is composed of $\text{Al}_x\text{OGa}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1). The rest of the structure of the LED structure 508 is similar or the same as all the layers of the LED structure 100 as described in Figure 1. In some embodiments, the layer 510 is located between the p-cladding layer 118 and the p-transition layer 120. In some embodiments, the oxide layer 510 is formed from an oxidation process after all the layers of the LED structure 500 as described in Figure 5A is formed.

[00125] In some embodiments, a subsequent oxidation process is applied after all the epitaxial layers of the LED structure 500 are formed. In some embodiments, the oxidation process is a wet oxidation. In some embodiments, the wet oxidation is conducted in a wet oxygen oxidation furnace. In one example, the wet oxygen oxidation furnace is VF3000 VCSEL furnace from Koyo Thermo Systems. In some embodiments, a nitrogen gas is used as carrier gas at a flow rate of 1 liter per minute. Oxygen is obtained from the water heated at around 98°C in the wet oxygen oxidation furnace. In some embodiments, the wet oxidation uses an ambient temperature from 380°C to 500°C , and a time of equal to or under 2 hours. The oxidation is a controlled oxidation on the side wall of the LED structure 500. Since all the other layers in the LED structure 500 are not reactive to the oxidation process, the side wall of the layer 502 is oxidized. The oxidation process is stopped when the desired oxidation depth of the side wall of the layer 502 is reached. In some embodiments, the preferred oxidation depth of the side wall of the layer 502 is around one fourth of the lateral diameter of the layer 502. In some embodiments, the preferred oxidation depth of the side wall of the layer 502 is around one fifth of the lateral diameter of the layer 502. In some embodiments, the preferred oxidation depth of the side wall of the layer 502 is around one third of the lateral diameter of the layer 502.

[00126] In some embodiments, after the oxidation process, the oxide layer 510 composed of $\text{Al}_x\text{OGa}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1) is formed from

the original layer 502 composed of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1). In a preferred embodiment, the oxide layer 510 has $\text{Al}_x\text{OGa}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1) formed around the edge of the layer of 510, for example, 512 and 514, i.e., toward the side of the LED structure 508, while the center of the layer 510 remains less oxidized /or remains not oxidized. In some embodiments, all the other layers in the LED structure 500/508 other than the original layer 502 composed of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ (x is greater than or equal to 0.9 and less than 1) are resistant to the oxidation process and remain unoxidized.

[00127] Non-radiative electron-hole pair recombination at the side surfaces, especially, defect sites, of the p-cladding layer 118 and p-transition layer 120 may cause additional energy loss, such as heat, and reduce the light emission efficiency. The introduction of the oxide layer 510 between the p-cladding layer 118 and p-transition layer 120 can reduce the surface non-radiative recombination and improve the light emission efficiency of the LED device. Specifically, when the oxidation mostly happens at the edge of the layer 510, the formed oxide layer can reduce or eliminate the non-radiative recombination at the side surfaces or edge, such as, locations 512 and 514, around the layer 510. The main current of an LED is in a vertical direction and there are some current diffusions to the side of the LED in the electric current flowing process. In some embodiments, when the oxidation mostly happens at the edge of the layer 510, the formed oxide layer can reduce the lateral diffusion of the electric current to the edge, and confine the electric current to the central portion of the LED device formed from the LED structure 508, therefore, increasing the effective electric current density and improving the LED light emission efficiency. In some embodiments, the light emission efficiency is at least 20%. In some embodiments, the light emission efficiency is at least 30%. In some embodiments, the light emission efficiency is at least 40%. In some embodiments, the light emission efficiency is at least 50%. In some embodiments, the light emission efficiency is at least 60%.

[00128] In some other embodiments, the precursor layer or the oxidized layer is formed between the n-cladding layer 110 and the n-spacer layer 112. In yet some other embodiments, the precursor layer or the oxidized layer is formed between the p-cladding layer 118 and the p-transition layer 120.

[00129] In some embodiments, the pre-cursor layers or the oxidized layers shown in any one of the Figures 2A-5B or mentioned above can be included in an LED structure in any combination. For example, the LED structure can include one to four layers of the pre-cursor layers or the oxidized layers at different positions of the LED structure as mentioned above. In another example, the LED structure can include one to six layers of the pre-cursor layers or the oxidized layers at different positions of the LED structure as mentioned above.

[00130] In some embodiments, it is preferred to have the oxide layer (s) formed on the n-side of the LED structure. In some processes, it is possible but difficult to introduce any Arsenic containing layers on the p-side of the LED structure that may impact the stability of the device.

[00131] In some embodiments, the substrate 102, for example, the GaAs substrate, from which the rest of the LED structure layers are grown from, by an epitaxial process, has a good lattice matching property with the epitaxial layers, but has some undesirable characteristics as the final LED device substrate, such as a low conductivity to support circuit structures, and a high light absorption to the light emitted from an LED. Therefore, the original substrate 102 may be removed from the final LED structure and a new substrate for better supporting circuit structures may be needed to form the LED device.

[00132] Figures 6A-6D illustrate a fabrication process utilizing a one-time transfer process to form an LED structure 612 with a supporting substrate 604 with integrated circuits, in accordance with some embodiments. In some embodiments, the initial color LED structure 602 shown in Figures 6A and 6C has the same or similar structures as any one of the LED structures described in Figures 1-5B, or any combination thereof. For illustration purpose, the exemplary structure 100 described in Figure 1 is shown in Figures 6A-6D as the LED structure 602. Other color LED structures such as 200, 208, 300, 308, 400, 408, 500, and 508 described in Figure 2A-5B, or any other LED structure embodiments described herein can be shown in Figures 6A-6D as the LED structure 602 in the same P to N direction as the LED structure 100.

[00133] In some embodiments, in Figure 6A, a metal bonding layer 606 is deposited on the p-side of the LED structure 602, for example, above the p^{++} -transition layer 124.

[00134] In some embodiments, in Figure 6B, a metal bonding layer 608 is deposited on a supporting substrate 604 with integrated circuit. In some embodiments, the supporting substrate 604 is the substrate on which the array of individual driver circuits 610 is fabricated. Each driver circuit 610 is a pixel driver. In some instances, the pixel drivers are thin-film transistor pixel drivers or silicon CMOS pixel drivers. In a preferred embodiment, the substrate 604 is a Silicon substrate. In another embodiment, the supporting substrate 604 is a transparent substrate, for example, a glass substrate. Other example substrates include GaAs, GaP, InP, SiC, ZnO, and sapphire substrates. The driver circuits 610 form individual pixel drivers to control the operation of the individual color LED device formed from the LED structure 602. The circuitry on substrate 604 includes contacts to each individual pixel driver 610 and also a ground contact.

[00135] In some embodiments, the LED structure 602 also has two types of contacts: P electrodes or anodes (not shown in Figures 6A-6D), which are connected to both the p-side of the LED structure 602 and the respective driver circuit 610; and N electrodes or cathodes (not shown in Figures 6A-6D), which are connected to both the n-side of the LED structure 602 and the ground (i.e., the common electrode).

[00136] In some embodiments, the driver circuit 610, for example, a pixel driver, includes a number of transistors and capacitors (not shown in Figures 6A-6D). The transistors include a driving transistor connected to a voltage supply, and a control transistor configured with its gate connected to a scan signal bus line. The capacitors include a storage capacitor used maintain the gate voltage of the driving transistor during the time that the scan signal is setting other pixels.

[00137] In some embodiments, in Figure 6C, the LED structure 602 and the supporting substrate 604 are bonded together by the bonding of the metal bonding layers 606 and 608. The combined metal bonding layer 606 and 608 may include ohmic contact layers in addition to the metal bonding layers. In some embodiments, the thickness of the combined metal bonding layer 606 and 608 is about 0.1 micron to about 3 microns. In some instances, two metal layers, such as 606 and 608 are included in the metal bonding layer. One of the metal layers is deposited on the LED structure 602. A counterpart metal bonding layer is deposited on the supporting substrate 604. In some embodiments, compositions for the combined metal

bonding layer include Au-Au bonding, Au-Sn bonding, Au-In bonding, Ti-Ti bonding, Cu-Cu bonding, or a mixture thereof. For example, if Au-Au bonding is selected, the two layers of Au respectively need a Cr coating as an adhesive layer, and Pt coating as an anti-diffusion layer. And the Pt coating is between the Au layer and the Cr layer. The Cr and Pt layers are positioned on the top and bottom of the two bonded Au layers. In some embodiments, when the thicknesses of the two Au layers are about the same, under a high pressure and a high temperature, the mutual diffusion of Au on both layers bonds the two layers together. Eutectic bonding, thermal compression bonding, and transient liquid phase (TLP) bonding are example techniques that may be used.

[00138] As shown in Figure 6C, the p-side of the LED structure 602, for example, the p^{++} -transition layer 124, is bonded with the supporting substrate 604 through the bonding metal layers 606 and 608. In some embodiments, the P-electrode (not shown in Figures 6A-6D) connects to the p^{++} -transition layer 124 through the combined metal bonding layer 606 and 608. In some embodiments, the P-electrode is connected through the metal bonding layer 606 and 608 to the driver circuit 610. In some embodiments, the metal bonding layer can function as an electrical contact layer.

[00139] In some embodiments, the substrate 102 of the LED structure 602 is then removed after the bonding step, for example, by a laser lift-off process or wet chemical etching, leaving the LED structure 612 shown in Figure 6D including the supporting substrate 604, the combined metal bonding layer 606 and 608, and the remaining layers of the LED structure 602 without the substrate 102. In some embodiments, the n-buffer layer 104 is also removed with the substrate 102. In some embodiments, the n-buffer layer 104 and the n-etch stop layer 106 are also removed with the substrate 102 in the same or different process.

[00140] In Figure 6D, the n-side of the LED structure 612, for example, n^{+} -contact layer 108, is the side where the light from the color LED device formed from the LED structure 612 is emitted out.

[00141] Figures 7A-7H illustrate a fabrication process utilizing a two-time transfer process to form an LED structure 732 with a supporting substrate 714 with integrated circuits, in accordance with some embodiments. In some embodiments, the initial color LED structure 702 has the same or similar structures as any one of the LED structures described in

Figures 1-5B, or any combination thereof. For illustration purpose, the exemplary structure 100 described in Figure 1 is shown in Figures 7A-7H as the LED structure 702. Other color LED structures such as 200, 208, 300, 308, 400, 408, 500, and 508 described in Figures 2-5, or any other LED structure embodiments described herein can be shown in Figures 7A-7H as the LED structure 702 in the same P to N direction as the LED structure 100.

[00142] In some embodiments, in Figure 7A, an Ultraviolet (UV) curable adhesive layer 706 is deposited on the p-side of the LED structure 702, for example, above the p^{++} -transition layer 124. The UV curable adhesive materials comprise one or more polymers selected from the group consisting of bonding adhesive Micro Resist BCL-1200, SU-8, photosensitive polyimide (PSPI), PermiNex, Benzocyclobutene (BCB), and transparent plastic (resin) including spin-on glass (SOG), or any combination thereof.

[00143] In some embodiments, in Figure 7B, an intermediate substrate 704 and the LED color structure 702 is bonded together by the UV curable adhesive layer 706. In some embodiments, the intermediate substrate 704 is made of sapphire. The intermediate substrate is needed to hold the LED structure on the substrate since the LED chip is thin and difficult to transfer. In another embodiment, the intermediate substrate 704 is a transparent substrate, for example, a glass substrate. Other example substrates include GaAs, GaP, InP, SiC, and ZnO substrates. In some embodiments, the UV curable adhesive layer 706 is cured by shining a UV light through the intermediate substrate 704 on the UV curable adhesive layer 706, therefore forming a high strength bond between the intermediate substrate 704 and the LED color structure 702. As shown in Figure 7B, the p-side of the LED structure 702, for example, the p^{++} -transition layer 124, is bonded with the intermediate substrate 704 through the UV curable adhesive layer 706.

[00144] In an alternative embodiments, the UV curable adhesive is deposited on the intermediate substrate 704 for bonding. In some embodiments, the UV curable adhesive is deposited on both the p-side of the LED color structure 702 and on the surface of the intermediate substrate 704 for bonding.

[00145] As shown in Figure 7C, in some embodiments, the substrate 102 of the LED structure 702 is then removed after the bonding step, for example, by a laser lift-off process or wet chemical etching, leaving the LED structure 712 shown in Figure 7C including the

intermediate substrate 704, the UV curable adhesive layer 706, and the remaining layers of the LED structure 702 without the substrate 102. In some embodiments, the n-buffer layer 104 is also removed with the substrate 102. In some embodiments, as shown in Figure 7C, the n-buffer layer 104 and the n-etch stop layer 106 are also removed with the substrate 102.

[00146] In some embodiments, in Figure 7D, a metal bonding layer 716 is deposited on the n-side of the LED structure 712, for example, above the n⁺-contact layer 108.

[00147] In some embodiments, in Figure 7E, a metal bonding layer 718 is deposited on a supporting substrate 714 with integrated circuit. In some embodiments, the supporting substrate 714 is the substrate on which the array of individual driver circuits 710 is fabricated. Each driver circuit 710 is a pixel driver. In some instances, the pixel drivers are thin-film transistor pixel drivers or silicon CMOS pixel drivers. In a preferred embodiment, the substrate 714 is a Silicon substrate. In another embodiment, the supporting substrate 714 is a transparent substrate, for example, a glass substrate. Other example substrates include GaAs, GaP, InP, SiC, ZnO, and sapphire substrates. The driver circuits 710 form individual pixel drivers to control the operation of the individual color LED device formed from the LED structure 712. The circuitry on substrate 714 includes contacts to each individual pixel driver 710 and also a ground contact.

[00148] In some embodiments, the LED structure 712 also has two types of contacts: P electrodes or anodes (not shown in Figures 7A-7H), which are connected to both the p-side of the LED structure 712 and the respective driver circuit 710; and N electrodes or cathodes (not shown in Figures 7A-7H), which are connected to both the n-side of the LED structure 712 and the ground (i.e., the common electrode).

[00149] In some embodiments, the driver circuit 710, for example, a pixel driver, includes a number of transistors and capacitors (not shown in Figures 7A-7H). The transistors include a driving transistor connected to a voltage supply, and a control transistor configured with its gate connected to a scan signal bus line. The capacitors include a storage capacitor used maintain the gate voltage of the driving transistor during the time that the scan signal is setting other pixels.

[00150] In some embodiments, in Figure 7F, the LED structure 712 and the supporting substrate 714 are bonded together by the bonding of the metal bonding layers 716 and 718.

The combined metal bonding layer 716 and 718 may include ohmic contact layers in addition to the metal bonding layers. In some embodiments, the thickness of the combined metal bonding layer 716 and 718 is about 0.1 micron to about 3 microns. In some instances, two metal layers, such as 716 and 718 are included in the metal bonding layer. One of the metal layers is deposited on the LED structure 712. A counterpart metal bonding layer is deposited on the supporting substrate 714. In some embodiments, compositions for the combined metal bonding layer include Au-Au bonding, Au-Sn bonding, Au-In bonding, Ti-Ti bonding, Cu-Cu bonding, or a mixture thereof. For example, if Au-Au bonding is selected, the two layers of Au respectively need a Cr coating as an adhesive layer, and Pt coating as an anti-diffusion layer. And the Pt coating is between the Au layer and the Cr layer. The Cr and Pt layers are positioned on the top and bottom of the two bonded Au layers. In some embodiments, when the thicknesses of the two Au layers are about the same, under a high pressure and a high temperature, the mutual diffusion of Au on both layers bonds the two layers together. Eutectic bonding, thermal compression bonding, and transient liquid phase (TLP) bonding are example techniques that may be used.

[00151] As shown in Figure 7F, the n-side of the LED structure 712, for example, the n^+ -contact layer 108, is bonded with the supporting substrate 714 through the bonding metal layers 716 and 718. In some embodiments, the P-electrode (not shown in Figures 7A-7H) connects to the p^{++} -transition layer 124 or the N-electrode (not shown in Figures 7A-7H) connects to the n^+ -contact layer 108 through the combined metal bonding layer 716 and 718. In some embodiments, the P-electrode or the N-electrode is connected through the metal bonding layer 716 and 718 to the driver circuit 710. In some embodiments, the metal bonding layer can function as an electrical contact layer.

[00152] In some embodiments, in Figure 7G, the intermediate substrate 704 of the LED structure 712 is then removed after the bonding step, for example, by a laser lift-off process or wet chemical etching, leaving the LED structure 722 shown in Figure 7G including the supporting substrate 714, the combined metal bonding layer 716 and 718, and the remaining layers of the LED structure 712 without the intermediate substrate 704.

[00153] In some embodiments, the UV curable adhesive layer 706 of the LED structure 722 is then removed after the intermediate substrate 704 is removed, for example,

by a chemical etching or laser lift-off, leaving the LED structure 732 shown in Figure 7H including the supporting substrate 714, the combined metal bonding layer 716 and 718, and the remaining layers of the LED structure 722 without the UV curable adhesive layer 706.

[00154] In Figure 7H, the p-side of the LED structure 732, for example, p^{++} -transition layer 124, is the side where the light from the color LED device formed from the LED structure 732 is emitted out.

[00155] In some embodiments, when the p-side is the side where light from an LED device is emitted out, a transparent electrode layer to the light of the LED, such as an Indium tin oxide (ITO) layer, can be deposited on the top of the p-side layers (not shown in Figures 7A-7H) of the LED to allow light to transmit further through the transparent electrode. In some embodiments, the transparent electrode is a p-electrode. In some embodiments, the material of the top electrode layer is selected from the group consisting of graphene, ITO, Aluminum-Doped Zinc Oxide (AZO), and Fluorine doped Tin Oxide (FTO). In general, it is hard for an ITO layer to form an ohmic contact with the n-side of an LED. The electrode layer used for the n-side of an LED is made of metal which may not be transparent to the light emitted from the LED. Compared to one-time transfer as described in Figures 6A-6D, the two-time transfer described in Figures 7A-7H forms a p-side emission LED that would allow better integration and easy fabrication of a transparent electrode at the top of the LED device.

[00156] In some embodiments, the p-side layers include the p-type layers such as the p-spacer layer 116, p-cladding layer 118, p-transition layer 120, p^{+} -transition layer 122, and p^{++} -transition layer 124. In some embodiments, the n-side layers include the n-type layers such as the n-spacer layer 112, n-cladding layer 110, and n⁺-contact layer 108.

[00157] In some embodiments, the thickness of the p-side layers of the LED structure 732 is thinner than the thickness of the n-side layers of the LED structure 732. In some embodiments, the thickness of the p-side layers of the LED structure 732 is thinner than the thickness of the n-side layers of the LED structure 732 as a result of the UV curable adhesive layer removal. In some embodiments, the reduction of the thickness of the p-side layers of the LED can limit the lateral diffusion of the electric current, make the current flow focused on the vertical direction of the LED, and enhance the light emission efficiency.

[00158] In some embodiments, the ratio of the total thickness of the p-type layers to the total thickness of the n-type layers is 0.025 to 100. In some preferred embodiments, the ratio of the total thickness of the p-type layers to the total thickness of the n-type layers is 1.5 to 2.

[00159] In some embodiments, the ratio of the thickness of the p-type conductive layers including the p-transition layer 120, p⁺-transition layer 122, and p⁺⁺-transition layer 124 to the thickness of the n-type conductive layer(s) including the n⁺-contact layer 108 is 0.025 to 100. In some preferred embodiments, the ratio of the thickness of the p-type conductive layers including the p-transition layer 120, p⁺-transition layer 122, and p⁺⁺-transition layer 124 to the thickness of the n-type conductive layer(s) including the n⁺-contact layer 108 is 1.5 to 2.

[00160] In some embodiments, the ratio of the thickness of the p-cladding layer 118 to the total thickness of the one or more of p-transition layer 120, p⁺-transition layer 122, and p⁺⁺-transition layer 124 is 0.02 to 120. In some preferred embodiments, the ratio of the thickness of the p-cladding layer 118 to the total thickness of the one or more of p-transition layer 120, p⁺-transition layer 122, and p⁺⁺-transition layer 124 is 1 to 2.5.

[00161] Various design aspects of the single color or multi-color LED device, such as the dimensions of the layers (*e.g.*, width, length, height, and cross-sectional area of each layer), the dimension of the electrodes, size, shape, spacing, and arrangement of the two or more LED structures, the two or more active light emitting layers, bonding layers, the conductive layers, other reflection layers, and the configuration between the integrated circuits, pixel driver and electrical connections are selected (*e.g.*, optimized using a cost or performance function) for obtaining the desired LED characteristics. LED characteristics that vary based on the above design aspects include, *e.g.*, size, materials, cost, fabrication efficiency, light emission efficiency, power consumption, directivity, luminous intensity, luminous flux, color, spectrum and spatial radiation pattern.

[00162] Further embodiments also include various subsets of the above embodiments including embodiments in Figures 1-7H combined or otherwise re-arranged in various embodiments.

[00163] Figure 8 is a top view of a micro LED display panel 800, in accordance with some embodiments. The display panel 800 includes a data interface 810, a control module 820 and a pixel region 850. The data interface 810 receives data defining the image to be displayed. The source(s) and format of this data will vary depending on the application. The control module 820 receives the incoming data and converts it to a form suitable to drive the pixels in the display panel. The control module 820 may include digital logic and/or state machines to convert from the received format to one appropriate for the pixel region 840, shift registers or other types of buffers and memory to store and transfer the data, digital-to-analog converters and level shifters, and scan controllers including clocking circuitry.

[00164] The pixel region 850 includes an array of mesas (not separately shown from the LED 834 in Figure 8) including pixels. The pixels include micro LEDs, such as a single color or multi-color LED 834, integrated with pixel drivers, for example as described above. An array of micro-lens (not separately shown from the LED 834 in Figure 8) covers the top of the array of mesas. In this example, the display panel 800 is a color RGB display panel. It includes red, green and blue pixels. Within each pixel, the LED 834 is controlled by a pixel driver. The pixel makes contact to a supply voltage (not shown in Figure 8) and ground via a ground pad 836, and also to a control signal, according to the embodiments shown previously. Although not shown in Figure 8, the p-electrode of the LED 834 and the output of the driving transistor are electrically connected. The LED current driving signal connection (between p-electrode of LED and output of the pixel driver), ground connection (between n-electrode and system ground), the supply voltage Vdd connection (between source of the pixel driver and system Vdd), and the control signal connection to the gate of the pixel driver are made in accordance with various embodiments. Any of the micro-lens array disclosed herein can be implemented with the micro LED display panel 800.

[00165] Figure 8 is merely a representative figure. Other designs will be apparent. For example, the colors do not have to be red, green and blue. They also do not have to be arranged in columns or stripes. As one example, apart from the arrangement of a square matrix of pixels shown in Figure 8, an arrangement of hexagonal matrix of pixels can also be used to form the display panel 800.

[00166] In some applications, a fully programmable rectangular array of pixels is not necessary. Other designs of display panels with a variety of shapes and displays may also be formed using the device structures described herein. One class of examples is specialty applications, including signage and automotive. For example, multiple pixels may be arranged in the shape of a star or a spiral to form a display panel, and different patterns on the display panel can be produced by turning on and off the LEDs. Another specialty example is automobile headlights and smart lighting, where certain pixels are grouped together to form various illumination shapes and each group of LED pixels can be turned on or off or otherwise adjusted by individual pixel drivers.

[00167] Even the lateral arrangement of devices within each pixel can vary. In Figure 1A, the LEDs and pixel drivers are arranged vertically, i.e., each LED is located on top of the corresponding pixel driver circuit. Other arrangements are possible. For example, the pixel drivers could also be located "behind", "in front of", or "beside" the LED.

[00168] Different types of display panels can be fabricated. For example, the resolution of a display panel can range typically from 8x8 to 3840x2160. Common display resolutions include QVGA with 320x240 resolution and an aspect ratio of 4:3, XGA with 1024x768 resolution and an aspect ratio of 4:3, D with 1280x720 resolution and an aspect ratio of 16:9, FHD with 1920x1080 resolution and an aspect ratio of 16:9, UHD with 3840x2160 resolution and an aspect ratio of 16:9, and 4K with 3264x2160 resolution. There can also be a wide variety of pixel sizes, ranging from sub-micron and below to 10 mm and above. The size of the overall display region can also vary widely, ranging from diagonals as small as tens of microns or less up to hundreds of inches or more.

[00169] Different applications will also have different requirements for optical brightness and viewing angle. Example applications include direct viewing display screens, light engines for home/office projectors and portable electronics such as smart phones, laptops, wearable electronics, AR and VR glasses, and retinal projections. The power consumption can vary from as low as a few milliwatts for retinal projectors to as high as kilowatts for large screen outdoor displays, projectors, and smart automobile headlights. In terms of frame rate, due to the fast response (nanoseconds) of inorganic LEDs, the frame rate can be as high as KHz, or even MHz for small resolutions.

[00170] Further embodiments also include various subsets of the above embodiments including embodiments as shown in Figures 1-8 combined or otherwise re-arranged in various other embodiments.

[00171] Although the detailed description contains many specifics, these should not be construed as limiting the scope of the invention but merely as illustrating different examples and aspects of the invention. It should be appreciated that the scope of the invention includes other embodiments not discussed in detail above. For example, the approaches described above can be applied to the integration of functional devices other than LEDs with control circuitry other than pixel drivers. Examples of non-LED devices include vertical cavity surface emitting lasers (VCSEL), photodetectors, micro-electro-mechanical system (MEMS), silicon photonic devices, power electronic devices, and distributed feedback lasers (DFB). Examples also include Organic LED (OLED) devices. Examples of other control circuitry include current drivers, voltage drivers, trans-impedance amplifiers, and logic circuits.

[00172] The preceding description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the embodiments described herein and variations thereof. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the subject matter disclosed herein. Thus, the present disclosure is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the following claims and the principles and novel features disclosed herein.

[00173] Features of the present invention can be implemented in, using, or with the assistance of a computer program product, such as a storage medium (media) or computer readable storage medium (media) having instructions stored thereon/in which can be used to program a processing system to perform any of the features presented herein. The storage medium can include, but is not limited to, high-speed random access memory, such as DRAM, SRAM, DDR RAM or other random access solid state memory devices, and may include non-volatile memory, such as one or more magnetic disk storage devices, optical disk storage devices, flash memory devices, or other non-volatile solid state storage devices. Memory optionally includes one or more storage devices remotely located from the CPU(s).

Memory or alternatively the non-volatile memory device(s) within the memory, comprises a non-transitory computer readable storage medium.

[00174] Stored on any machine readable medium (media), features of the present invention can be incorporated in software and/or firmware for controlling the hardware of a processing system, and for enabling a processing system to interact with other mechanisms utilizing the results of the present invention. Such software or firmware may include, but is not limited to, application code, device drivers, operating systems, and execution environments/containers.

[00175] It will be understood that, although the terms “first,” “second,” etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another.

[00176] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the claims. As used in the description of the embodiments and the appended claims, the singular forms “a,” “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will also be understood that the term “and/or” as used herein refers to and encompasses any and all possible combinations of one or more of the associated listed items. It will be further understood that the terms “comprises” and/or “comprising,” when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[00177] As used herein, the term “if” may be construed to mean “when” or “upon” or “in response to determining” or “in accordance with a determination” or “in response to detecting,” that a stated condition precedent is true, depending on the context. Similarly, the phrase “if it is determined [that a stated condition precedent is true]” or “if [a stated condition precedent is true]” or “when [a stated condition precedent is true]” may be construed to mean “upon determining” or “in response to determining” or “in accordance with a determination” or “upon detecting” or “in response to detecting” that the stated condition precedent is true, depending on the context.

[00178] The foregoing description, for purpose of explanation, has been described with reference to specific embodiments. However, the illustrative discussions above are not intended to be exhaustive or to limit the claims to the precise forms disclosed. Many modifications and variations are possible in view of the above teachings. The embodiments were chosen and described in order to best explain principles of operation and practical applications, to thereby enable others skilled in the art.

What is claimed is:

1. A micro light emitting diode (LED) chip structure, comprising:
 - a semiconductor substrate;
 - an electrical contact layer on a surface of the semiconductor substrate;
 - a first type of conductive layer on the semiconductor substrate;
 - an active light emitting layer on the first type of conductive layer; and
 - a second type of conductive layer on the active light emitting layer;wherein a thickness of the second-type of conductive layer is smaller than a thickness of the first-type of conductive layer, and a surface of the second-type of conductive layer is obtained after an organic material layer is removed.
2. A micro light emitting diode (LED) chip structure, comprising:
 - a semiconductor substrate;
 - an electrical contact layer on a surface of the semiconductor substrate;
 - a first type of conductive layer on the semiconductor substrate;
 - an active light emitting layer on the first type of conductive layer; and
 - a second type of conductive layer on the active light emitting layer;wherein a surface of the second-type of conductive layer is obtained after an organic material layer is removed.
3. The micro LED chip structure according to claim 1 or claim 2, further comprising a second type of spacer layer between the active light emitting layer and the second type of conductive layer, wherein the second type of spacer layer is used for forming a PN junction structure with the active light emitting layer and the first type of conductive layer, and the second type of conductive layer includes one or more of second type of conductive transition layers.
4. The micro LED chip structure according to claim 1 or claim 2, wherein the first type of conductive layer is an N-type layer, and the second type of conductive layer is a P-type layer.

5. The micro LED chip structure according to claim 1 or claim 2, wherein the semiconductor substrate is an integrated circuits (IC) substrate.

6. The micro LED chip structure according to claim 1 or claim 2, wherein the electrical contact layer is a metal bonding layer, and the semiconductor substrate and the first type of conductive layer are bonded together through a bonding process.

7. The micro LED chip structure according to claim 1 or claim 2, wherein the second type of conductive layer is a P-type GaP layer, and the first type of conductive layer is an N-type GaAs layer.

8. The micro LED chip structure according to claim 1 or claim 2, further comprising a first type of cladding layer between the first type of conductive layer and the active light emitting layer.

9. The micro LED chip structure according to claim 8, further comprising an oxide layer within the first type of cladding layer.

10. The micro LED chip structure according to claim 8, further comprising an oxide layer between the first type of conductive layer and the first type of cladding layer.

11. The micro LED chip structure of claim 1 or claim 2, further comprising a second type of cladding layer between the second type of conductive layer and the active light emitting layer.

12. The micro LED chip structure according to claim 11, further comprising an oxide layer within the second type of cladding layer.

13. The micro LED chip structure according to claim 11, further comprising an oxide layer between the second type of conductive layer and the second type of cladding layer.

14. The micro LED chip structure according to any one of claims 9, 10, 12, and 13, wherein material of the oxide layer is $\text{Al}_x\text{OGa}_{1-x}\text{As}$, and x is greater or equal to 0.9 and less than 1.

15. The micro LED chip according to claim 8, wherein material of the first type of cladding layer is AlInP .

16. The micro LED chip according to claim 11, wherein the second type of cladding layer includes one or more layers of AlInP , $\text{Al}_x\text{Ga}_{1-x}\text{InP}$ (x is greater than 0 and less than 1), and GaInP .

17. The micro LED chip according to claim 1 or claim 2, wherein the organic material layer is an ultraviolet (UV) curable bonding layer.

18. The micro LED chip structure according to claim 1 or claim 2, wherein a ratio of a thickness of the second type of conductive layer to a thickness of the first type of conductive layer is 0.025 to 100.

19. The micro LED chip structure according to claim 1 or claim 2, wherein a ratio of a thickness of the second type of conductive layer to a thickness of the first type of conductive layer is 1.5 to 2.

20. The micro LED chip structure of claim 1 or claim 2, further comprising a second type of cladding layer between the second type of conductive layer and the active light emitting layer, wherein the second type of conductive layer includes a second type of conductive transition layer.

21. The micro LED chip structure of claim 20, wherein a ratio of a thickness of the second type of cladding layer to a thickness of the second type of conductive transition layer is 0.02 to 120.

22. The micro LED chip structure according to claim 20, wherein a ratio of a thickness of the second type of cladding layer to a thickness of the second type of conductive transition layer is 1 to 2.5.

23. The micro LED chip structure according to claim 1 or claim 2, wherein the second type of conductive layer comprises sequentially a lower second type of conductive transition layer, a middle second type of conductive transition layer, and an upper second type of conductive transition layer in a direction from the semiconductor substrate to the first type of conductive layer.

24. The micro LED chip structure according to claim 23, wherein a conductivity of the lower second type of conductive transition layer is less than that of the middle second type of conductive transition layer, and the conductivity of the middle second type of conductive transition layer is less than the upper second type of conductive transition layer.

25. The micro LED chip according to claim 11, wherein the second type of cladding layer includes one or more layers of AlInP, and $\text{Al}_x\text{Ga}_{1-x}\text{InP}$ (x is greater than or equal to 0 and less than or equal to 1).

26. An epitaxial structure for a micro light emitting diode (LED), comprising:
a semiconductor substrate;
an electrical conductive layer of a first conductivity type on the semiconductor substrate;
a cladding layer of the first conductivity type on the electrical conductive layer of the first conductivity type;
a first oxide layer within the cladding layer of the first conductivity type;
an active light emitting layer on the cladding layer of the first conductivity type;
a cladding layer of a second conductivity type on the active light emitting layer; and

an electrical conductive layer of the second conductivity type on the cladding layer of the second conductivity type.

27. The epitaxial structure for the micro LED according to claim 26, further comprising: a second oxide layer within the cladding layer of the second conductivity type.

28. The epitaxial structure for the micro LED according to claim 26, further comprising: a second oxide layer between the cladding layer of the second conductivity type and the electrical conductive layer of the second conductivity type.

29. An epitaxial structure for a micro light emitting diode (LED), comprising:
a semiconductor substrate;
an electrical conductive layer of a first conductivity type on the semiconductor substrate;
a cladding layer of the first conductivity type on the electrical conductive layer of the first conductivity type;
a first oxide layer between the electrical conductive layer of the first conductivity type and the cladding layer of the first conductivity type;
an active light emitting layer on the cladding layer of the first conductivity type;
a cladding layer of a second conductivity type on the active light emitting layer; and
an electrical conductive layer of the second conductivity type on the cladding layer of the second conductivity type.

30. The epitaxial structure for the micro LED according to claim 29, further comprising: a second oxide layer between the cladding layer of the second conductivity type and the electrical conductive layer of the second conductivity type.

31. The epitaxial structure for the micro LED according to claim 29, further comprising: a second oxide layer within the cladding layer of the second conductivity type.

32. An epitaxial structure for a micro light emitting diode (LED), comprising:

- a semiconductor substrate;
- an electrical conductive layer of a first conductivity type on the semiconductor substrate;
- a cladding layer of the first conductivity type on the electrical conductive layer of the first conductivity type;
- an active light emitting layer on the cladding layer of the first conductivity type;
- a cladding layer of a second conductivity type on the active light emitting layer;
- a first oxide layer within the cladding layer of the second conductivity type;
- and
- an electrical conductive layer of the second conductivity type on the cladding layer of the second conductivity type.

33. The epitaxial structure for the micro LED according to claim 32, further comprising: a second oxide layer within the cladding layer of the first conductivity type.

34. The epitaxial structure for the micro LED according to claim 32, further comprising: a second oxide layer between the cladding layer of the first conductivity type and the electrical conductive layer of the first conductivity type.

35. An epitaxial structure for a micro light emitting diode (LED), comprising:

- a semiconductor substrate;
- an electrical conductive layer of a first conductivity type on the semiconductor substrate;
- a cladding layer of the first conductivity type on the electrical conductive layer of the first conductivity type;
- an active light emitting layer on the cladding layer of the first conductivity type;

a cladding layer of a second conductivity type on the active light emitting layer;

an electrical conductive layer of the second conductivity type on the cladding layer of the second conductivity type; and

a first oxide layer between the cladding layer of the second conductivity type and the electrical conductive layer of the second conductivity type.

36. The epitaxial structure for the micro LED according to claim 35, further comprising: a second oxide layer between the cladding layer of the first conductivity type and the electrical conductive layer of the first conductivity type.

37. The epitaxial structure for the micro LED according to claim 35, further comprising: a second oxide layer within the cladding layer of the first conductivity type.

38. The epitaxial structure for the micro LED according to any one of claims 26, 29, 32, or 35, wherein the first oxide layer is formed as an oxide ring from an oxide layer precursor $\text{Al}_x\text{Ga}_{1-x}\text{As}$, and x is greater or equal to 0.9 and less than 1.

39. The epitaxial structure for the micro LED according to any one of claims 26, 29, 32, or 35, wherein the cladding layer of the first conductivity type includes one or more layers.

40. The epitaxial structure for the micro LED according to any one of claims 26, 29, 32, or 35, wherein the cladding layer of the second conductivity type includes one or more layers.

41. The epitaxial structure for the micro LED according to any one of claims 26, 29, 32, or 35, further comprising: between the semiconductor substrate and the electrical conductive layer of the first conductivity type, sequentially a buffer layer of the first conductivity type and an etch-stop layer of the first conductivity type in a direction from the semiconductor substrate to the electrical conductive layer of the first conductivity type.

42. The epitaxial structure for the micro LED according to any one of claims 26, 29, 32, or 35, further comprising: a spacer layer of the first conductivity type located on a bottom of the active light emitting layer, and a spacer layer of the second conductivity type located on a top of the active light emitting layer.

43. The epitaxial structure of the micro LED according to any one of claims 26, 29, 32, or 35, wherein the electrical conductive layer of the second conductivity type comprises one or more conductive transition layers.

44. The epitaxial structure for the micro LED according to any one of claims 26, 29, 32, or 35, wherein the electrical conductive layer of the second conductivity type comprises sequentially a lower conductive transition layer of the second conductivity type, a middle conductive transition layer of the second conductivity type, and an upper conductive transition layer of the second conductivity type in a direction from the semiconductor substrate to the electrical conductive layer of the first conductivity type.

45. The epitaxial structure of the micro LED according to claim 44, wherein a conductivity of the lower conductive transition layer of the second conductivity type is less than that of the middle conductive transition layer of the second conductivity type, and the conductivity of the middle conductive transition layer of the second conductivity type is less than the upper conductive transition layer of the second conductivity type.

46. The epitaxial structure for the micro LED according to any one of claims 26, 29, 32, or 35, wherein material of the first oxide layer is $\text{Al}_x\text{OGa}_{1-x}\text{As}$, and x is greater or equal to 0.9 and less than 1.

47. The epitaxial structure for a micro LED according to any one of claims 26, 29, 32, or 35, wherein material of the cladding layer of the first conductivity type is AlInP .

48. The epitaxial structure for the micro LED according to any one of claims 26, 29, 32, or 35, wherein material of the cladding layer of the second conductivity type includes one or more layers of AlInP, and $\text{Al}_x\text{Ga}_{1-x}\text{InP}$ (x is greater than or equal to 0 and less than or equal to 1).