

TRANSISTOR. TRANSISTOR ARRAY. METHOD FOR MANUFACTURING
TRANSISTOR ARRAY. AND NONVOLATILE SEMICONDUCTOR MEMORY

ABSTRACT OF THE DISCLOSURE

A memory cell comprises source-drain regions, a channel region, floating gate electrodes, and a control gate electrode. The floating gate electrodes are placed next to each other over the channel region on a gate insulating layer. The control gate electrode is located over the floating gate electrodes on an insulating layer and an insulating layer, both layers being formed by a LOCOS method. Protuberances are formed on the upper corners of the floating gate electrodes by the insulating layer. A central portion of the control gate electrode is laid over the channel region on insulating layers, to form a selecting gate. A selecting transistor comprises this selecting gate between both the source-drain regions.

Figure 1(a)

This Sheet Has Been Replaced

