SURFACE TREATMENT FOR MULTI-LAYER WAFERS FORMED FROM LAYERS OF MATERIALS CHOSEN FROM AMONG SEMICONDUCTING MATERIALS

This invention relates in general to surface treatment of multi-layer wafers formed from layers of materials chosen from among semiconducting materials.

More precisely, the invention relates to a process for treatment of a multi-layer wafer with materials having differential thermal characteristics, the process comprising a high temperature heat treatment step that can generate secondary defects.

Note that a "wafer" means a structure that may include one or several layers.

Thus, a multi-layer wafer is such a structure that contains several layers.

And the wafers concerned by this invention are wafers comprising a thin surface layer (made of a material such as silicon) for applications in micro-electronics.

Remember that the useful layer is generally a surface layer of the wafer, on which components will be created.

This layer must be very good quality and free from defects.

The term "differential thermal characteristics" will be explained below.

In the case of a multi-layer wafer, the different layers may have been associated with each other by any type of technique known in itself (layer transfer, gluing, epitaxy, etc.).

For applications in microelectronics, it is frequently necessary to perform heat treatment of the wafer - for example heat treatment designed to improve the surface condition of the surface layer of the wafer or thinning by sacrificial oxidation.

Surface treatments are also known involving a high temperature heat treatment.

The term "high temperature heat treatment" in this text denotes a heat treatment in which at least some phases are carried out at temperatures of several hundred degrees, for example exceeding 750°C for silicon films in a silicon on Quartz (SOQ - Silicon On Quartz) structure.

Note that this high temperature heat treatment definition is not absolute: it is simply given in the context of this text, and it can cover other temperature ranges outside the context of the invention.

This type of heat treatment can be carried out according to an RTA (Rapid Thermal Annealing) mode, for a limited time (of the order of a few seconds to a few minutes only).

But RTA mode is not limitative and the invention is applicable to any other type of high temperature heat treatment.

For example, this type of heat treatment may be applied to wafers concerned by the invention.

For example, this type of heat treatment may be intended to modify the structure of the wafer, and / or to improve the surface condition of the wafer.

For example surface treatments involving smoothing annealing are also known.

In particular, this type of annealing lowers the surface roughness of a surface layer of a semiconducting material (for example such as silicon) to values compatible with specifications in force in the semiconducting industry.

Thus, one process well adapted to this effect in the case of a surface layer of silicon, consists of performing a smoothing annealing on the wafer comprising the layer, under a reducing atmosphere and, particularly under a hydrogen atmosphere) at a high temperature (that may be more than 950°C - for example 1100°C).

"Smoothing annealing" is thus defined as being annealing carried out under a reducing atmosphere at high temperature - and more precisely at a temperature of the order of 950°C or more. Smoothing annealing is thus a particular form of high temperature heat treatment.

This type of annealing can be carried out for a relatively long time (for example of the order of two hours).

It can also be done in RTA mode at a very high temperature (of the order of 1100°C or more), for a duration of a few seconds to a few minutes only.

This type of annealing smoothes the surface of the wafer. It can also cure some structural defects.

According to known processes, this type of high temperature heat treatment is done on the wafer once it has been created (in other words once operations have been carried out in advance - for example transfer of layers and gluing and / or epitaxy - necessary for creation of the multi-layer wafer).

However, these known high temperature heat treatments cannot be used on all types of wafers, since there are some limitations associated with them.

The application of this type of high temperature heat treatment to the treatment of single-layer wafers, or multi-layer wafers in which the different layers have differential thermal characteristics, can be problematic.

Note that " differential thermal characteristics" means a differential behaviour during exposure of the different layers of the wafer at a given thermal budget.

This type of differential typically corresponds to a difference in the coefficients of thermal expansion of materials forming the different layers of the wafer, combined with dimensional characteristics of these layers.

And more precisely, in the context of this text, "differential thermal characteristics" of a multi-layer structure are characterized as follows for the purposes of this text:

- at least some layers of the structure are associated with different coefficients of thermal expansion,

- furthermore, there is at least one layer with a significant thickness close to the surface layer (in this case the term "significant thickness" is defined as being a thickness of at least an order of magnitude greater than (namely 10 times greater than) the thickness of the surface layer) that is associated with a coefficient of thermal expansion significantly different from the coefficient of thermal expansion associated with the said surface layer.

An SOQ type wafer, comprising a thin surface layer of silicon directly associated with a Quartz support layer with a significant thickness, is thus a typical example of such a structure for which the layers have differential thermal characteristics.

In the case of this type of wafer that relaxes after exposure to a large thermal budget (such as thermal budgets that occur with the treatments mentioned above), the thin surface layer of silicon recovers a significant part of the mechanical stresses generated by exposure of the wafer to the thermal budget.

In this case, the thin surface layer of silicon, for which the coefficient of thermal expansion is of the order of $2.5 \times 10^{-6} K^{-1}$, which is five times greater than the corresponding value for the subjacent Quartz layer which is of the order of $0.5 \times 10^{-6} K^{-1}$, naturally tends to expand to relax stresses caused by heating.

Note that the coefficient of thermal expansion is defined as being a dimensional variation compared with a

reference dimension, per degree of temperature difference. This coefficient is therefore expressed in K^{-1}.

But at the same time, the subjacent layer of Quartz to which the surface layer of silicon is fixed does not tend to expand in the same way, and this applies stresses to the surface silicon layer.

In the frequent case in which the surface of the said thin layer of silicon includes defects (corresponding to "initial" defects that will be defined in more detail in the remainder of the text), such defects vary under the effect of the said stresses to produce secondary dislocation type defects.

Note that the term "secondary defects" will be defined later on.

A wafer for which only a very thin buried layer has a coefficient of thermal expansion significantly different from the coefficient of thermal expansion of the material in the surface layer would not correspond to the definition of a wafer given above for which the layers have "differential thermal characteristics".

A conventional SOI (Silicon On Insulator) type wafer is thus an example of a wafer comprising a surface layer of silicon, under which there is firstly a very thin layer of SiO2, then a thick support layer that is typically made of silicon.

In this case, the buried layer SiO2 is associated with a coefficient of thermal expansion that is significantly different from the coefficient of thermal expansion associated with the silicon surface layer, but no secondary defect generation is observed like that mentioned above.

In the case of SOI, the SiO2 layer is buried between two silicon layers that have thicknesses comparable to the SOI layer or are thicker.

The very thin layer of SiO2 under these conditions cannot "impose" its mechanical behaviour when exposed to high thermal stresses.

Finally, note that it would certainly be possible to observe secondary defects of the dislocation type in the layer of SiO2 itself. But since the material in this layer is amorphous, it does not generate any dislocation type crystalline defects.

Returning to the presentation of the problem that the invention is intended to solve, when a wafer for which the layers have a differential thermal characteristic receives a large thermal budget, at least one of the layers of the wafer may be affected by high mechanical stresses due to the difference in expansion of the different layers under the effect of the received heat load.

Remember that the different layers in a wafer remain fixed to each other.

The applicant thus observed the appearance of "secondary" defects in SOQ wafers following high temperature heat treatment like that mentioned above (for example, possibly a smoothing annealing, a heat treatment under neutral gas, oxidation, etc.).

We will now mention that the term "quartz" in this description means molten silica.

In the example of an SOQ structure, the observed defects are located in the silicon film and in particular are crystalline defects corresponding to "secondary

defects", since they are generated during the high temperature heat treatment and are related to the initial defects already present in the wafer.

Note that in particular, secondary defects may be dislocation type defects, or other crystalline defects associated with initial defects.

"Initial defects" means defects that are already present in materials from which the wafer is composed, or defects generated during one of the steps in initial manufacture of the wafer, before application of the heat treatment associated with appearance of secondary defects (in particular, these initial defects may be sharp edges caused by the strong roughness after detachment of the wafer from a donor substrate).

And in general, the Applicant has observed the appearance of secondary defects in multi-layer wafers with differential thermal characteristics when the wafers are exposed to a high temperature heat treatment step (for example, the heat treatment may be a smoothing annealing or an RTA treatment, or an oxidation annealing, or in general a high temperature heat treatment).

This undesirable effect is shown in figures 1 and 2, which represent observations obtained by TEM (Transmission Electronic Microscopy) on a section through two SOQ wafers (one control indicating the scale of the figure in its bottom left corner).

These two figures show a section through the upper part of an SOQ wafer on which a high temperature heat treatment has been carried out.

This top part corresponds to the surface layer of Si, and to (at least part of) the SiO2 layer inserted between the surface layer of Si and the Quartz support of the wafer (support not shown).

Thus, Figure 1 illustrates a dislocation passing through the entire thickness of the surface layer of crystalline silicon (separated from a quartz layer that is not shown on the figures and is located below an SiO2 layer).

This type of dislocation is obviously a very serious defect for the silicon surface layer.

Figure 2 illustrates a loop dislocation 20 - that also creates a serious disadvantage.

Note that this type of defect generated by smoothing annealing and sometimes extending through the entire thickness of the surface layer (400 nm in the example in Figure 1) cannot be completely eliminated by thinning the layer, for example by polishing after the said annealing.

The Applicant has demonstrated that this type of defect appears particularly when the surface of the multi-layer wafer has initial defects before being exposed to annealing.

In this case, the initial defects are involved in secondary defect generation mechanisms (of the dislocation type in Figures 1 and 2) under the effect of mechanical stresses resulting from exposure to a heat budget of the multi-layer wafer with differential thermal characteristics, starting from initial defects already present in the wafer before the high temperature heat treatment.

For example, the initial defects might be disturbances on the wafer surface.

These initial defects may have been created during previous treatment steps applied to the wafer.

Figure 3 thus illustrates the layer of silicon in the SOQ wafer in Figures 1 and 2 before a high temperature heat treatment was applied to it, this Figure 3 showing a disturbed silicon surface.

The disturbances on this surface layer may for example correspond to initial defects that will be involved during a high temperature heat treatment in the generation of secondary defects.

One purpose of the invention is to be able to eliminate such secondary defects in the case of a multi-layer wafer for which the materials have differential thermal characteristics.

Another purpose of the invention is to not generate defect lines during a high temperature heat treatment (the meaning of these defect lines being explained later in this text).

The background and the purposes mentioned here above are thus very specific. And it shall be noted in this respect that known documents such as US 6 500 732, WO 02/27783 and US 6 150 239 do not belong to the specific background which has been set here above.

US 6 500 732 is generally focused on the operations which allow to form the cleaving layer of a structure, for a subsequent cleaving in order to make a multilayer wafer.

This document thus proposes means for suppressing (or reducing) a cleaving layer.

But it does not make any mention of any background or objective of avoiding forming secondary defects during a high temperature heat treatment.

Furthermore, this document does not even mention any high temperature heat treatment of the wafer itself. This document only mentions the option of smoothing by a high temperature heat treatment (through the reference to US 6 171 965), only for the treatment of the residue of a donor wafer, for its recycling.

And this document does not either mention any background or problem which would be associated to a multilayer wafer with materials having differential thermal characteristics.

WO 02/27783 discloses a step of polishing by CMP after cleaving a layer, for reducing the surface roughness of the cleaved layer.

But this document does no more than US 6 500 732 mention any problem or objective associated with a high temperature heat treatment.

US 6 150 239 does not in any way aim at preventing undesirable effects such as the apparition of secondary defects during a high temperature heat treatment which would be applied to a multilayer wafer.

On the contrary, this document proposes means which precisely aim at avoiding submitting a multilayer to temperatures which would be too high. In this respect, the objective of this document is to allow reducing the temperature of a heat treatment in a transfer process (and it shall moreover be noted that such heat treatment for a

transfer is in any event not a "high temperature" heat treatment).

Thus, and as it shall even better appear when reading the description of the present invention, US 6 150 239 not only does not belong to the specific background defined for the invention, but it furthermore teach the man skilled in the art away from any high temperature treatment. Coming back now to the presentation of the background of the invention and of its purposes, according to a first aspect of the invention there is provided a process for treatment of a multi-layer wafer with materials having differential thermal characteristics, the process comprising a high temperature heat treatment step that can generate secondary defects, characterized in that the process includes a wafer surface preparation step before the high temperature heat treatment step.

Preferred but non-limitative embodiments of such a process are as follows:

- the said preparation step may include a thinning operation on the surface layer of the wafer,
- the said preparation may include polishing,
- the said polishing may be mechanical-chemical polishing,
- the said preparation may include an ionic or chemical etching,
- the said differential thermal characteristics may correspond to a combination of the following two conditions:

at least some layers of the wafer are associated with different thermal expansion coefficients,

there is a layer with a significant thickness close to the surface layer of the wafer associated with a coefficient of thermal expansion that is significantly different from the coefficient of thermal expansion associated with the said surface layer,

- the wafer may include a silicon support substrate and a surface layer made of Ge or SiGe,

- the high temperature heat treatment may be RTA annealing,

- the high temperature heat treatment may be a smoothing annealing,

- the process may include a second treatment in association with the preparation step designed to prevent the appearance of defect lines during the high temperature heat treatment,

- the said second treatment may include a second heat treatment,

- the said second heat treatment may be done before the preparation step,

- the said second heat treatment may be carried out with a thermal budget lower than a limiting thermal budget beyond which defects will appear during the high temperature heat treatment,

- the wafer may be an SOQ wafer and the second heat treatment may be carried out with a thermal budget less than or equal to the thermal budget corresponding to two hours of annealing at a temperature of 700°C,

- the wafer may be a Germanium on Silicon wafer and the second heat treatment may be carried out with a thermal budget

less than or equal to the thermal budget corresponding to two hours of annealing at a temperature of 500°C,

- the said second treatment may include a second chemical treatment,

- the said second chemical treatment may be carried out after the preparation step,

- the said second chemical treatment may use the RIE type of wet etching or dry etching,

- the second chemical treatment may be associated with an oxide deposition and then selective etching of the oxide so as to define an etching pattern,

- the said second chemical treatment may use etching on the projecting back face,

- the said second treatment may include a second mechanical treatment,

- the said second mechanical treatment may be carried out after the preparation step,

- the second mechanical treatment may use attack by a diamond, laser or ionic bombardment of neutral molecules,

- the second mechanical treatment may use local polishing at the ring, to make a bevel,

- the second treatment may include the definition of regions that are to be isolated from any singular points in the surface layer of the wafer,

- the second treatment may use a photolithography that etches grooves delimiting the said regions in the surface of the said surface layer,

- the said isolated regions may correspond to required locations at which chips will be formed on the wafer.

- regions may be defined such that their contour does not form a projecting angle, the top of which could form a singular point that could be associated with a defect line.

Other aspects, purposes and advantages of the invention will become clearer after reading the following description of the invention made with reference to the attached drawings on which, apart from Figures 1 to 3 that have already been commented upon above:

- Figures 4a, 4b1 and 4b2, 4c1 and 4c2 are diagrammatic top views of a multi-layer wafer that has not been treated according to the invention. In these figures:

Figure 4a shows the wafer before the preparation step,

Figures 4b1 and 4b2 show the same wafer after the preparation step - "singular points" type defects being shown in figure 4b2 which is an enlarged partial view derived from Figure 4b1,

Figures 4c1 and 4c2 are diagrammatic views of the same wafer, which have also been subjected to a high temperature heat treatment after the preparation step. Once again in this case, Figure 4c2 is a partial enlarged view derived from Figure 4c1. These figures diagrammatically show defect lines that form secondary defects.

- Figures 5a and 5b show two diagrammatic representations of steps in one embodiment of a treatment according to the invention (the wafer treated being shown in section in these figures).

- Figure 6 is a view corresponding to the views in Figures 5a and 5b, illustrating another embodiment of the invention,

- Figures 7a to 7c show three diagrammatic representations of top views of wafers, illustrating a variant embodiment of the invention.

As mentioned above, the invention is applicable to multi-layer wafers with differential thermal characteristics.

"Differential thermal characteristics" have been defined above. In particular, they correspond to a difference in the coefficients of thermal expansion of two layers in the wafer, if this difference is large enough to generate secondary defects when the wafer is exposed to a high temperature heat treatment.

In order to avoid the generation of such secondary defects and to apply the demonstration of the "starting point" effect mentioned above demonstrated by the Applicant (initial defects in a wafer - for example defects on its disturbed surface - form starting points from which much larger secondary defects are generated during a high temperature heat treatment), the high temperature heat treatment according to the invention is preceded by a surface preparation step of the wafer to be treated.

This preparation corresponds to a thinning step of the surface layer of the wafer.

It may be achieved by polishing (but the preparation step may also include thinning of the surface layer of the wafer by ionic etching - ion or ion cluster bombardment, or by chemical etching - dry or wet).

In the case of preparation by polishing, this type of preparation polishing is preferably a mechanical-chemical (CMP) polishing. This type of polishing removes 1000Å from the surface layer on which the defects are located.

It also eliminates initial defects in the surface layer of the wafer that would generate secondary defects observed during a high temperature heat treatment such as a smoothing annealing.

The Applicant has observed that the use of such a preliminary polishing step for example subsequently enabled smoothing annealing under a hydrogenated atmosphere for a duration of about two hours, on an SOQ wafer.

And this type of smoothing annealing did not generate dislocation type secondary defects (observable in transmission electronic microscopy), defects which are observed in the absence of prior polishing on similar wafers.

Note that the process according to the invention may be used after detachment of the multi-layer wafer from a donor substrate, for example detachment by the addition of heat and / or mechanical energy at a weakening interface.

Thus, the invention may be used for example in a Smart-Cut® type process.

Remember that the Smart-Cut® process can be used to build up multi-layer wafers and requires a step in which wafers are detached from a substrate.

In this context, it is possible to use a Smart-Cut® type technique to make multi-layer wafers with differential thermal characteristics, then to treat these wafers by a high temperature heat treatment such as smoothing

annealing, without observing secondary defects (for example of the dislocations type).

In this example embodiment of the invention, insertion of a preparation step (particularly by polishing) between when the wafers are detached and when the high temperature heat treatment is applied, can avoid the appearance of such secondary defects during the high temperature heat treatment.

And more generally, the invention can be used to apply high temperature heat treatments to multi-layer wafers with differential thermal characteristics: the invention is not limited to wafers obtained by a Smart-Cut® type process.

Remember that the high temperature heat treatment may be any type of high temperature heat treatment.

It may also be done in RTA annealing mode.

And regardless of the embodiment, it may be a smoothing annealing.

Note that a second treatment can be associated with the preparation step (which then corresponds to a "first" treatment), designed to prevent the appearance of defect lines during the high temperature heat treatment of the wafer.

Note also that the terms "first" treatment and "second" treatment do not involve any chronology or any systematic sequence between these two treatments.

The Applicant has observed that the preparation step itself can cause singular points on the wafer (for example at the wafer ring), and these singular points are revealed and amplified during the high temperature heat treatment.

For example, these singular points may correspond to material "micro-tearing" points - for example micro-tearing at the wafer ring.

The Applicant has thus observed defects arranged in lines (or "defect lines") that appear during the high temperature heat treatment.

These defect lines are due to singular points generated during the preparation (particularly for the case of polishing).

Figures 4a, 4b1 and 4b2, 4c1 and 4c2 diagrammatically illustrate generation of these defect lines:

Figure 4a shows a diagrammatic top view of a multi-layer wafer 100 comprising a substrate 110 forming the lower layer, and a surface layer 120.

The layer 120 has a diameter slightly less than the diameter of the layer 110, and thus forms a projecting peripheral shoulder that leaves a peripheral part of the surface of the layer 110 exposed.

This annular peripheral part is known as "the ring".

Figure 4a shows the wafer 100 before polishing corresponding to the preparation step.

As can be seen, the contour around the ring is regular.

Figures 4b1 and 4b2 show corresponding views, representing the wafer 100 after a polishing step has been carried out on it (typically CMP polishing).

Figure 4b2 shows that the polishing has caused micro-tearing points 130 at the wafer ring (these singular points being represented in an exaggerated manner enlarged in the figures).

Figures 4c1 and 4c2 illustrate defect lines 140 that can appear starting from these singular points, when a high temperature heat treatment is subsequently applied to the wafer.

Therefore a second treatment is performed on the wafers to prevent the appearance of these defect lines during the high temperature heat treatment, in association with the preparation step.

As will be seen, the expression "in association with" the preparation step does not imply that the complementary treatment is necessarily done at the same time as the preparation.

The second treatment may also be done before or after the preparation step.

In particular, the second treatment may include:

- a heat treatment, and / or
- a mechanical treatment, and / or
- a chemical treatment.

This type of second treatment can limit the generation of singular points (which as described above correspond to points that can give rise to defect lines during a high temperature treatment) during this preparation step.

In particular, this limitation of singular points enables limitation of singular points at the wafer ring.

Thus, this type of second treatment minimizes or completely prevents the appearance of defect lines during a high temperature treatment.

It is said that this second treatment may be done particularly by a thermal, and / or mechanical, and / or chemical process.

The main purpose of such a second treatment is to cut around the wafer ring (in other words so that it forms a regular contour).

A second chemical treatment is preferably carried out after the preparation step.

This type of second chemical treatment may in particular use wet etching, or dry etching - for example an RIE type dry etching that uses bombardment by particles that are chemically reactive with the bombarded wafer.

In this case, the exposed face of the ring needs to be protected in advance. This type of protection is necessary particularly for the case of an RIE type dry etching.

The back face of the wafer also needs protection for wet etching.

It is important to avoid using a high temperature heat treatment when performing this type of protection.

Therefore, this protection of surfaces to be protected cannot be done by oxidation involving a high temperature heat treatment.

One preferred solution for building up a protection layer consists of depositing an oxide on the surfaces to be protected.

In particular, this oxide may be a PECVD (Plasma Enhanced Chemical Vapour Deposition) or LPCVD (Low Plasma Chemical Vapour Deposition) type oxide.

The choice between these two types of deposition will depend on the type of operation selected to cut around the wafer ring afterwards, and also on the difference in the coefficient of thermal expansion between the layers of the wafer:

- a PECVD type deposition is done at a temperature of about 400°C, and can therefore be used even on wafers with layers with significantly different coefficients of expansion,

- an LPCVD type deposition is used at a temperature of about 700°C, and therefore can only be used if the coefficients of thermal expansion of the layers in the wafer are fairly similar.

In the case of an SOQ wafer, the two types of deposition could be envisaged since it is observed that defect lines start to appear from a temperature of about 750°C.

In the case of a Germanium on silicon wafer, the defect lines may appear at temperatures lower than in the case of an SOQ wafer. Therefore, it will be preferred to use a PECVD type deposition.

The next step after depositing an oxide on all faces of the wafer, is to selectively etch the oxide near the edge of the ring, so as to eliminate this oxide.

For example, this selective etching may be done by photolithography.

In photolithography, the deposited oxide 1000 has to be covered by a layer of resin 1001 as shown in Figure 5a.

This figure shows a wafer 100 in section, in which the peripheral edge 1101 has been exposed by such a selective etching.

The other parts of the wafer remain covered by the protective oxide 1000.

The next step is to remove the resin 1001 and selective etching of silicon around the peripheral edge of

the ring, as shown in figure 5b (on this figure, the arrows symbolize the etching operation).

The result is a ring with a clean and smooth periphery with no singular points.

A Spin Etcher type equipment (registered trademark), marketed by the SEZ company could also be used to do this type of selective etching of the ring.

In this variant shown in figure 6, the wafer 100 is chemically etched on its back face, opposite to the face on which the ring to be cut around is located.

The said back face was covered by a protective layer 1002 before this etching.

Figure 6 shows arrival 20 of the etching product on the back face of the wafer 100.

The chemical etching product may be allowed to overlap slightly on the front face of the wafer (facing downwards on the figure), the path of the chemical etching product is shown symbolically in the Figure by arrows.

This makes it possible to attack the periphery of the layer 120 and to make the ring uniform.

Note that a neutral gas flow such as nitrogen is applied onto the main face of the layer 120, during this operation so as to avoid chemical etching solutions running on this main face.

Etching done according to this variant will be referred to as "overlapping back edge etching".

A second mechanical treatment may also be applied, using mechanical cutting around the ring of the wafer.

Like the second chemical treatment process mentioned above, this type of second mechanical process is preferably done after the polishing step.

This mechanical treatment may particularly make use of:

- mechanical means for cutting around the ring. This may be done using a diamond, a laser or ionic bombardment of neutral molecules causing cleaning of this ring.

- local polishing at the ring, for bevelling.

And if a second heat treatment process is used, this type of treatment is preferably done before the preparation step.

Note that a second prior treatment carried out in the form of a heat treatment can also consolidate bonding interfaces of the wafer layers (for example between a quartz layer and a silicon layer) before the preparation step.

In the case of a second heat treatment, the applicant has also demonstrated the existence of a limiting heat budget beyond which a subsequent high temperature heat treatment would cause the appearance of supplementary defects, and / or encourage the appearance of the defect lines mentioned above.

Therefore, the second heat treatment must be carried out with a heat budget that remains less than or equal to this limiting heat budget, which corresponds to a maximum heat input that can be applied to the wafer during this preliminary thermal heat treatment.

The limiting thermal budget depends on the nature of the layers of the treated wafer.

And in particular, the applicant has determined that this limiting thermal budget corresponds to:

- for SOQ wafers, annealing carried out for two hours at a temperature of 700°C,
- for germanium on silicon wafers, annealing carried out for two hours at a temperature of 500°C.

Obviously, during the second heat treatment, the duration of annealing can be extended for the same thermal budget and the temperature can be lowered, or vice versa.

It has been seen above that different types of "second" treatments can minimize or completely prevent the appearance of defect lines during the high temperature treatment applied to the wafer.

Note that the invention is applicable to all types of multi-layer wafers for which materials have differential thermal characteristics.

The invention may thus be applied to an SOQ type structure as described.

It can also be applied to wafers comprising a surface layer made of Germanium or SiGe (particularly SiGe rich in Germanium) on a support substrate (possibly silicon).

According to one variant embodiment of the invention, it may be required to treat these defect lines only in regions of the wafer in which chips will be formed later (particularly in the useful layer of the wafer).

In this variant embodiment of the invention, the second treatment includes definition of regions 1200 that are to be isolated from singular points (singular points that are formed particularly around the periphery of the wafer ring as already mentioned), in the surface layer of

the wafer (layer 120 in figures 4a to 4c2, 5 and 6, the same reference being used in figures 7a to 7c).

One or several chips may be located in each region 1200.

The regions 1200 can be selectively isolated by photolithography, by etching grooves delimiting the said regions 1200 in the surface of the layer 120.

These regions 1200 correspond to the locations required for chips to be formed on the wafer.

Figure 7a thus very diagrammatically illustrates two wafers 100, each of which includes three regions 1200 that have been isolated from singular points 130 around the edge of the ring, the said singular points being capable of generating defect lines 140.

Concerning this variant embodiment of the invention, the applicant also determined that defect lines were preferably oriented along given crystallographic directions.

In particular, this has been observed on SOQ wafers on which a high temperature heat treatment has been applied.

Preferably, the contour around regions 1200 is made such that these contours do not have projecting corners that could form a singular point, that could also correspond to an "initial defect".

Therefore, contours without projecting angles are preferably made for regions 1200. For example, these contours may be in the form of a circle or an oval.

Figures 7b and 7c thus illustrate poor configurations in this respect in which the regions 1200 are blocks, in

which there are corners in the periphery that should preferably be avoided.

CLAIMS

1. Process for treatment of a multi-layer wafer with materials having differential thermal characteristics, the process comprising a high temperature heat treatment step that can generate secondary defects, characterised in that this process includes a wafer surface preparation step before the high temperature heat treatment step.

2. Process according to the previous claim, characterised in that the said preparation step includes a step for thinning the wafer surface layer.

3. Process according to the previous claim, characterised in that the said preparation step includes polishing.

4. Process according to the previous claim, characterised in that polishing is mechanical-chemical polishing.

5. Process according to claim 1 or 2, characterised in that the said preparation step includes an ionic or chemical etching.

6. Process according to any one of the previous claims, characterised in that the said differential thermal characteristics correspond to a combination of the following two conditions:

- at least some layers of the wafer are associated with different thermal expansion coefficients,
- there is a layer with a significant thickness close to the surface layer of the wafer associated with a coefficient of thermal expansion that is significantly

different from the coefficient of thermal expansion associated with the said surface layer.

7. Process according to any one of the previous claims, characterised in that the wafer includes a silicon support substrate and a surface layer made of Ge or SiGe.

8. Process according to any one of the previous claims, characterised in that the high temperature heat treatment is RTA annealing.

9. Process according to any one of the previous claims, characterised in that the high temperature heat treatment is a smoothing annealing.

10. Process according to any one of the previous claims, characterised in that the process includes a second treatment in association with the preparation step designed to prevent the appearance of defect lines during the high temperature heat treatment.

11. Process according to the previous claim, characterised in that the said second treatment includes a second heat treatment.

12. Process according to the previous claim, characterised in that the said second heat treatment is done before the preparation step.

13. Process according to one of the two previous claims, characterised in that the said second heat treatment is carried out with a thermal budget lower than a limiting thermal budget beyond which defects will appear during the high temperature heat treatment.

14. Process according to the previous claim, characterised in that the wafer is an SOQ wafer and the second heat treatment is carried out with a thermal budget

less than or equal to the thermal budget corresponding to two hours of annealing at a temperature of 700°C.

15. Process according to claim 13, characterised in that the wafer is a Germanium on Silicon wafer and the second heat treatment is carried out with a thermal budget less than or equal to the thermal budget corresponding to two hours of annealing at a temperature of 500°C.

16. Process according to one of the six previous claims, characterised in that the said second treatment includes a second chemical treatment.

17. Process according to the previous claim, characterised in that the said second chemical treatment is carried out after the preparation step.

18. Process according to the previous claim, characterised in that the said second chemical treatment uses the RIE type of wet etching or dry etching.

19. Process according to one of the two previous claims, characterised in that the second chemical treatment is associated with an oxide deposition and then selective etching of the oxide so as to define an etching pattern.

20. Process according to either claim 17 or 18, characterised in that the said second chemical treatment uses overlapping back face etching.

21. Process according to any one of the eleven previous claims, characterised in that the said second treatment includes a second mechanical treatment.

22. Process according to the previous claim, characterised in that the said second mechanical treatment is carried out after the preparation step.

23. Process according to one of the two previous claims, characterised in that the second mechanical treatment uses attack by a diamond, laser or ionic bombardment of neutral molecules.

24. Process according to one of the three previous claims, characterised in that the second mechanical treatment uses local polishing at the ring, to make a bevel.

25. Process according to claim 10, characterised in that the second treatment includes the definition of regions to be isolated from any singular points in the surface layer of the wafer.

26. Process according to the previous claim, characterised in that the second treatment uses a photolithography that etches grooves delimiting the said regions in the surface of the said surface layer.

27. Process according to one of the two previous claims, characterised in that the said isolated regions correspond to required locations at which chips will be formed on the wafer.

28. Process according to the one of the three previous claims, characterised in that regions are defined such that their contour does not form a projecting angle, the top of which could form a singular point that could be associated with a defect line.