Description

This invention relates generally to a semiconductor integrated circuit device (IC), and more particularly to a technique suitable for use in gate arrays as one of semi-custom ICs.

A gate array includes, for example, an input-output buffer portion and an internal circuit portion, and a plurality of unit cells (macrocells) are formed inside the internal circuit portion. Each of the unit cells (macrocells) in turn consists of a plurality of gates.

The gate array makes it possible to produce a wide variety of semiconductor integrated circuit devices by applying respective wiring works in accordance with the types of the semiconductor integrated circuit devices to large quantities of master wafers that are produced in advance. The gate array provides other advantages such as the reduction of cost of production due to the mass-production of the master wafers, the automatic design of the wirings, and the reduction of development period by a production process which requires only wiring.

The term "gate" hereby means a minimum unit consistuting a logic circuit (a logical functional block that cannot be divided any more), and the term "unit cell (macrocell)„ means a logical functional block constituted by a plurality of gates, such as a multiplexor, a flip-flop, and the like.

The internal wiring of each gate is made by a manufacturer of the IC, while the wiring between the unit cells is made in accordance with a user's specification. The disposition of each cell and the disposition of wirings in the gate array are made by use of CAD (computer Aided Design) or DA (Design Automation).

Hitachi, Ltd. previously developed a Bi-CMOS gate array of a type in which bipolar elements and CMOSFET (complementary insulated gate field effect transistor) exist inside one chip, and its definite content is described in Japanese Patent Application No. 152886/1984. Another Bi-CMOS gate array, from the same applicant, is known from EP—A—0 125 504. In this document the elements having a high load driving capacity (Bipolar transistor) are disposed at peripheral posistions in the basic cell in a direction substantially vertical to the direction of the basic cell arrays and a second kind of element having a lower driving capacity (insulated gate FET) are disposed at the centre portion of said Basic cell. The present invention pertains primarily to improve the integration density of the Bi-CMOS gate array described above and to a layout technique which can enhance the cell utilization efficiency of the gate array.

In order to improve the integration density of the gate array, the following requirements must be satisfied.

(1) A greater number of basic cells (which will be later described) must be formed inside a limited semiconductor substrate.

(2) All the basic cells must be used efficiently. In the Bi-CMOS composite gate array described above, however, it has been difficult to satisfy the requirements (1) and (2) described above because the area of one basic cell tends to be greater than that of a pure CMOS cell, and to secure wiring regions.

It is an object of the present invention to provide a novel semiconductor integrated circuit which has high speed operation, low power consumption and high integration density.

The object is met by the features of the semiconductor integrated circuit device such as claimed in claim 1.

Brief Description of the Drawings

Fig. 1 shows the overall system configuration of a gate array and logic levels of signals in respective blocks;

Fig. 2 is a circuit diagram and shows a further definite circuit construction of a macro-cell level of a gate array shown in Fig. 1;

Fig. 3 is a circuit diagram showing a definite construction of a block 211 shown in Fig. 2; wherein

Fig. 3(a) shows logic symbols;

Fig. 3(b) shows a definite circuit construction;

Fig. 4 shows a definite construction of a block 213 shown in Fig. 2; wherein

Fig. 4(a) is a circuit diagram showing an example of a unit cell (macrocell) by use of logic symbols of an R—S flip-flop;

Fig. 4(b) is a definite circuit diagram of the R—S flip-flop circuit shown in Fig. 4(a);

Fig. 5(a) shows an overall planar layout of a gate array;

Fig. 5(b) shows in more detail the layout of an A region shown in Fig. 5(a);

Fig. 6(a) is a planar layout diagram showing primarily the arrangement of diffusion layers and polysilicon layers in one unit cell;

Fig. 6(b) is a sectional view of the device taken along line X—X of a basic cell shown in Fig. 6(a);

Fig. 6(c) is a symbol diagram of the basic cell shown in Fig. 6(a);

Fig. 7(a) is a circuit diagram showing the construction of a basic cell;

Fig. 7(b) is a diagram showing the construction of the basic cell by logic symbols;

Fig. 8 is a planar layout diagram showing the inside of a basic cell and wiring state between the basic cells and between basic cell arrays in accordance with one embodiment of the present invention;

Figs. 9, 10 and 11 are explanatory views showing the characterizing features of the present invention; wherein

Fig. 9(a) is a plan view showing in a symbolized form a 2-input NAND basic cell;

Fig. 9(b) is a plan view showing in a symbolized form a 3-input NAND basic cell;

Fig. 9(c) shows logic symbols of the 2-input NAND unit cell;

Fig. 9(d) shows logic symbols of the 3-input NAND unit cell;

Fig. 9(e) is a circuit diagram of a D-type flip-flop using the 3-input NAND circuit;

Figs. 10(a) through 10(d) are symbol diagrams useful for explaining the utilization efficiency of the 2-input NAND type cell and the 3-input NAND type cell;

Figs. 10(e) through 10(h) are logic symbol diagrams corresponding to Figs. 10(a) through 10(d), respectively;

Fig. 10(i) is a circuit diagram of a 2-bit decoder constituted by using the 2-input NAND circuit and an inverter;

Figs. 11(a), 11(b) and 11(c) are explanatory views useful for explaining the features and problems when the 3-input NAND type cell is used; wherein

Fig. 11(a) is a logic symbol diagram of a 3-input NAND cell;

Fig. 11(b) is a layout diagram;

Fig. 11(c) is a layout diagram showing the wiring state between basis cell arrays;

Figs. 11(d) through 11(f) show the features when the 2-input NAND type cell is used, and correspond to Figs. 11(a) through 11(c), respectively;

Figs, 11(g) through 11(i) show the feature when a modified 2-input cell of the present invention is used and correspond to Figs. 11(a) through 11(c), respectively;

Fig. 12 is a plan view of a gate array showing the four features (i) through (iv) of the present invention;

Fig. 13 is a layout diagram of a basic cell and is useful for explaining the problem when the present invention is not used; and

Fig. 14 is a planar layout diagram useful for explaining the wiring rule in the gate array in the present invention.

Description of the Preferred Embodiments

a) *Problems examined by the inventors before the present invention*

The following items are important in order to improve the integration density.

(1) To assemble the greatest possible number of basic cells (basic unit on a layout which contains circuit elements sufficient to constitute one gate, such as a diffusion layer, a resistor, or the like) in one semiconductor substrate. To accomplish this object, the occupying area of one basic cell must be minimized. A gate array is an IC in which a large number of (e.g., from several thousands to tens of thousands) of basic cells (which will be sometimes referred to also as "cells") are arranged, and even if the difference of the occupying area of one basic cell is very small, this small difference is built up when a large number of basic cells are integrated so that the integration density will be remarkably different.

(2) The basic cells formed in the substrate must be utilized effectively. Even if a large number of basic cells are formed in the semiconductor substrate, there is no technical significance if such basic cells can not be utilized for forming a practical circuit. The cell utilisation efficiency primarily depends upon where wirings that can be connected to each of a large number of cells can be actually extended in a limited layout space. Therefore, unless the wirings can be extended, the cells cannot be utilized but are left in vain. It is of course possible to improve the utilization ratio of the cells by providing a sufficient space for extending the wirings, but as a result the integration density will drop.

(3) A logic circuit, that can be constituted by use of the elements (diffusion layer, etc) incorporated in one cell, must be selected carefully.

For instance, although a 2-input NAND circuit and a 3-input NAND circuit can be constituted can be formed respectively by use of one basic cell, various differences occur between them when designing a gate array. In other words, since the number of inputs of the 3-input NAND type cell is greater by one than that of the 2-input NAND type cell, and hence the occupying area of the former becomes greater as much. However, if all the circuits requested by users in general can be constituted basically by the 3-input NAND type, the cell utilization efficiency can of course be improved by use of the 3-input NAND type cells. On the contrary, if the circuits requested by the users can be constituted primarily by use of the 2-input type cells, the integration density can be improved by use of the 2-input NAND type cells.

Thus, each type of cells has its merit and demerit. The circuits actually requested by the users are divers; some consist basically of a 3-input NAND circuit while the others consist basically of a 2-input NAND circuit. Therefore, the selection of the cell types must be made carefully by examining the merit and demerit of each type and comparing them with those of the other types and at times, empirically.

b) *Wiring rule in gate array*

A wiring rule will be explained with reference to Fig. 14. As shown in the drawing, basic cell arrays (B.C) 10 are arranged in an X direction to form a basic cell array, and the basic cell arrays are arranged in a Y direction to constitute a basic cell matrix as a whole.

Spaces (W_1, W'_1) between these B.C. arrays are extension regions of external wirings, and the external wirings (1000, 1000') in the X direction and external wirings (1001, 1001', 1001'') in the Y direction are extended in these regions.

Internal wirings l_{IN} inside the B.C. array extend in both X and Y directions inside each B.C. array in order to electrically connect each basic cell.

As shown in the drawing, the internal wiring l_{IN} and external wiring (1000, 1000') in the X direction consist of an aluminum first layer wiring (Al1), and the external wiring (1001, 1001', 1001'') in the Y direction consists of an aluminum second layer wiring (AlR^2).

c) *Features of the present invention*

In order to have the present invention more easily understood, the features of the present invention will be explained with reference to Figs. 9 through 12 before the definite description of the embodiments.

First of all, it will be assumed that a D-type flip-flop circuit such as shown in Fig. 9(e) is constituted by 3-input NAND type cells. If the 3-input NAND type cells shown in Figs. 9(b) and 9(d) are used, the flip-flop circuit described above can be constituted by six basic cells. If 2-input NAND cells such as shown in Figs. 9(a) and 9(c) are used, however, nine basic cells ($1.5 \times 6 = 9$) are necessary to obtain the flip-flop circuit. Therefore, if the 3-input NAND cells are used, the number of cells used is 2/3, and this is more efficient.

Next, it will be assumed that a 2-bit decoder is constituted by use of 2-input NAND cells and inverters as shown in Fig. 10(i). This 2-bit decoder consists of six circuit elements G through L and in this case, one basic cells is used to constitute one circuit element.

The utilization efficiency of the cell when the 2-input NAND cell is used will be explained with reference to Figs. 10(a) and 10(c). It is only the five basic cells ($0.5 \times 2 + 1 \times 4$) that are effectively used for the 2-bit decoder in practice. In contrast, the cell utilization efficiency when the 3-input NAND cells are used will be explained with reference to Figs. 10(b) and 10(d). In this case, 3.3 basic cells ($0.33 \times 2 + 0.66 \times 4 = 3.3$) are utilized effectively. In other words, the utilization efficiency is 5/6 for the 2-input NAND cell, whereas it is 3.3/6 for the 3-input NAND cell, and the former is higher than the latter. Thus, the merit and demerit of the basic cell vary depending upon the circuit (unit cell) to be fabricated.

One of the characterizing features of the present invention lies in that the cell types to be used can be changed suitably in accordance with the circuit construction of the circuit (unit cell) to be fabricated in consideration of the merit and demerit of each cell type, and can form a desired gate array most efficiently.

This feature of the present invention will be explained with reference to Figs. 10 and 11.

Figs. 11(a) through 11(c) illustrate the feature of the present invention when a 3-input NAND type cells are used, wherein (a) is a logic symbol diagram, (b) is its definite layout diagram and (c) shows the channel number of external wirings extended between the cell arrays. Figs. 11(d) through 11(f) shows the feature of the invention when the 2-input NAND cells are used, and correspond to Figs. 11(a) through 11(c), respectively. Figs. 11(g) through 11(c) show the feature of the invention when modified 2-input cells in accordance with the present invention are used, and correspond to Figs. 11(a) through 11(c), respectively.

First of all, the occupying area of one cell will be compared with reference to Figs. 11(b), (e) and (h). The explanation of the definite construction will be hereby omitted because it will be described elsewhere. In the drawings, the portions represented by oblique lines designate the gate of each MOSFET formed by polysilicon, and each functions as a signal input terminal. As can be seen from Fig. 11(a), the lateral width of the cell is increased by the width of a third signal input terminal Xa in the case of the 3-input NAND cell, and the overall lateral width amounts to $l_1 + l_2$. In order to effectively utilize the three signal input terminals as shown in Fig. 11(c), 21 external wirings are necessary therefor.

In the case of a 2-input NAND cell, on the other hand, the lateral width may be only l_1 as shown in Fig. 11(e). Since the number of the signal input terminals of each cell decreases as can be seen from Fig. 11(g), the total number of the necessary external wirings may be only 16, so that the width between the B.C array is W_1 and this is considerably smaller than W_2 in Fig. 11(c).

The modified 2-input cell is based upon the 2-input NAND cell cell described above, and its occupying area as well as its wiring channel number are the same as those of the latter. The difference lies in that the modified 2-input cell has a built-in third signal input terminal, and the cell can be used as a 3-input NAND cell, whenever necessary, by utilizing this terminal.

This third terminal is never connected to the external wiring but only the internal wiring I_{IN} of the basic cell array can be connected to it.

Another characterizing feature of the present invention lies in the layout of the modified 2-input cell. As shown in Fig. 12(iv), bipolar transistors as high load driving functional elements are disposed on both sides of a cell in one cell, while an MOS element is disposed at the center of the cell. According to this layout, a V_{cc} line and a ground line (GND) extend along both edges of the cell and do not prevent the extension of the internal wiring I_{IN}. If the bipolar elements are disposed at the center of the cell with the MOS elements at both ends of the cell as shown in Fig. 13, the V_{cc} line and the GND line must extend through the center of the cell so that the extension of the internal wiring I_{IN} is prevented.

The features of the invention described above can be summarized as follows with reference to the Fig. 12.

i) The cell normally operates as a 2-input NAND cell.

ii) It can be used as a 3-input NAND cell, whenever necessary.

iii) The external wirings may be the same as those of a 2-input NAND cell, and hence the gap W_1 between the basic cell arrays can be reduced.

iv) The wiring structure can be simplified because the bipolar elements are disposed at the external portions and the MOS element at the inner portion.

d) *Embodiments of the invention*

Hereinafter, the invention will be explained with reference to the drawings.

Fig. 1 shows the overall system configuration of the gate array (IC) of the present invention and signal levels at respective portions of the gate array. As can be seen from the drawing, this IC consists of an input buffer 20, a logic portion 21 consisting principally of CMOS and an output buffer 22. The input buffer 20 has a level converting function (and if necessary, a logic calculation

function). For example, it converts input signals IN_A, IN_B and NN_C of a TTL level received from outside to signals of a CMOS levels, and its output signal is applied to the logic portion 21 consisting principally of CMOS. On the other hand, the output buffer 22 has a level converting function of converting the signals of the CMOS level to signals of the TTL level, for example. (If necessary, a logic calculation function can be further added.) Eventually, it produces the output signals OUT_1 OUT_2, . . . , OUT_m of the TTL level, for exmaple.

Fig. 2 shows in further detail the internal construction of the system shown in Fig. 1. In the drawing, reference numerals 21l—21n in the logic portion 21 represent unit cells (macrocells) and black circles or the tip portions colored in black represent that the circuit of the output stage is constituted by a bipolar circuit. (The rest of the portions are constituted by CMOSs of low power consumption type.) The term "unit cell (macrocell)" means a logic function block constituted by a plurality of logic elements (which are the minimum unit constituting a logic circuit and a logic function block which can not be divided any more), and represents, for example, a multiplexor or a flip-flop. The internal wiring of the unit cell is made by manufacturers of the IC while the wiring between the unit cells is made in accordance with a user's specification. The arrangement of each cell and the arrangement of wirings are made by use of DA (Design Automation).

As described already, the output gate (output buffer) of each of the unit cells 21l—21n, the input buffers 20l—20n and the output buffers 22l—22m is a high load driving type gate consisting of a bipolar circuit. For this reason, a signal delay quantity can be made substantially equal to a small signal delay quantity of an internal gate irrespective of the length of wirings connecting one unit to another or the magnitude of the load, and the freedom of design can be remarkably improved.

The block 211 shown in Fig. 2 has the construction shown in Figs. 3(A) and 3(B), wherein (A) shows logic symbols and (B) represents the particular circuit construction.

In Fig. 2, the block 213 is, for example, an R—S flip-flip circuit constituted such as shown in Figs. 4(a) and 4(b).

Next, the planar layout of the silicon chip 1 of the IC (gate array) shown in Figs. 1 and 2 will be explained with reference to Figs. 5(a) and 5(b). As shown in Fig. 5(a), the arrays of the Bi-CMOS cells (basic cells) 10 are arranged regularly in the chip, and the input-output buffers 20, 22 are arranged around the arrays. Bonding pads are disposed around the outermost periphery.

Fig. 5(b) is a planar layout diagram showing more definitely the layout structure of the portion A encompassed by dotted line in Fig. 5(a). Bonding wires 12 are connected to pads 11, and the pads and input-output buffers (20n, 22n) are connected by first layer Al wirings 12. A power source (V_{cc}) line and a ground (GND) line consisting of a second layer Al wiring are extended on the input-output buffers (20n, 22n), and are connected to the first layer Al wiring through respective through-holes. Thus, the V_{cc} line 13 and the GND line 14 that are common to the input-output buffers and the basic cell arrays are extended.

The above explains the overall construction of IC.

Next, the important features of the present invention will be explained once again.

Fig. 8 shows definitely the planar layout of the region B encompassed by dotted line in Fig. 5(b), and Fig. 6(a) shows the planar layout of the basic cells (sometimes referred to as "B.C") shown in Figs. 5(a) and 5(b) with the diffusion layer in the chip being shown primarily. Fig. 6(b) is a sectional view taken along line X—X' in Fig. 6(a). Fig. 6(c) is a symbol diagram of the basic cell shown in Fig. 6(a). Fig. 7(a) shows the circuit of the basic cell and Fig. 7(b) shows the basic cell as logic symbols.

The term "basic cell" means a basic unit of the layout construction at the logic portion formed by disposing constituent elements necessary for constituting an electronic circuit in a predetermined pattern.

The layout structure of the basic cell 10 will be explained with reference to Fig. 6(a). As shown in the drawing, the basic cell 10 consists of the gates 30, 31, 32, n-well 50 and p-well 51 of MOSFET consisting of polysilicon, a P^+ diffusion layer 35 as the source-drain of a P-MOSFET, an N^+ diffusion layer 36 as the source-drain of an N-MOSFET, diffusion layers 37, 40 (serving as emitter: E) constituting two bipolar NPN transistors Q_1, Q_2, diffusion layers 38, 41 (as base: B), diffusion layers 39, 42 (as collector: C), and two impedance elements, that are, in this case, resistors R_1, R_2. Fig. (6b) is a sectional view of the basic cell 10 shown in Fig. 6(a) taken along line X—X'.

Fig. 7a shows the circuit of the basic cell 10. As can be seen from this circuit diagram, an NAND gate which is apparently of the 2-input type but is substantially of the 3-input type can be constituted by applying predetermined wirings to the elements formed inside the basic cell 10. Fig. 7(b) shows the basic cell 10 in the symbolized form.

Fig. 8 shows the basic cell 10 after wiring.

The wiring rule will be explained once again with reference to Fig. 1. In the drawing, the regions I, I' are those in which the basic cells 10 are arranged regularly in the X direction (horizontal to the sheet of the drawing), and will be hereinafter called the "basic cell array".

The wiring inside the basic cell array is made by a first layer aluminum wiring l_{IN} in both X direction and Y direction (perpendicular to the X direction) as indicated by thick line in the drawing.

The wiring between the basic cell arrays (or macrocell wiring) is made by use of a first layer aluminum wiring 510 in the X direction as shown in Fig. 1 and by use of a second layer aluminum wiring 500 (represented by dotted line in the drawing) in the Y direction. In the drawing, the

region II is a wiring region in which the first layer aluminum wiring (microcell wiring) in the X direction is extended.

The above explains the basic construction of the gate array.

Next, the effect of the present invention and the reason why such an effect can be obtained will be described.

As described already, the basic cell is actually a 2-input NAND gate, but it incorporates therein one more gate and hence functions substantially as a 3-input NAND gate.

The planar layout condition of the basic cell is shown in Fig. 2(a), and when such a modified 2-input construction is employed, the cell occupying area can be reduced for the following reasons.

Referring to Figs. 11(b), (e) and (h), the cell area increases in the case of (b) because the gate is formed in such a manner as to extend rightward of the bipolar element (the portion represented by symbol Xa). Studies made by the present inventor reveal that while $l_1 = 32$ μm in the drawing, $l_1 + l_2$ becomes 40 μm. Therefore, if the modified 2-input cell is used, the cell area can be reduced by 20%.

According to the construction described above, the effective utilization efficiency of the cell can also be improved.

In other words, when one circuit (macrocell) is formed, the wiring freedom can be much improved and the number of gates can be reduced by use of the 3-input NAND type cell than by use of the 2-input NAND type cell because the number of input terminals of the former is greater than that of the latter and the freedom of wiring can be improved as much. From the aspect of the cell utilization efficiency, however, the wiring channel number becomes greater in the case of the 3-input NAND, and when various macrocells are constituted, the extension of the Al wirings becomes a critical problem that the number of waste cells becomes greater and the chip area increases, on the contrary.

The modified 2-input cell described above becomes substantially a 3-input NAND type cell when the second signal input terminal incorporated therein is connected by an internal wiring inside the basic cell array. Therefore, the number of gates of the circuit construction can be reduced, and since the third signal input terminal is never connected to the wiring extended in the extension region, the wiring channel number is the same as when the 2-input NAND type cell is used. As a result, the increase of the chip area due to the increase of the channel number can be prevented.

As described above, one of the characterizing features of the present invention resides in that the reduction of the occupying area of one cell itself and the improvement in the cell utilization efficiency can be accomplished by a simple circuit construction.

The present invention has another feature.

As shown in Fig. 12, the bipolar elements are disposed both outsides of MOSFET, so that the V_{cc} line 13 and the GND line 14 are vertically extended in parallel with the basic cell array. In other words, two NPN transistors Q_1 and Q_2 of a totem pole connection at the output stage in the basic cell are disposed on both sides of MOSFET, and along with this arrangement, the V_{cc} line and the GND line extend above and below the cell. Then, it is possible to freely extend the first layer Al wiring in the same way in the center portion of the basic cell 10 is parallel with the basic cell array, that is, the region interposed between the V_{cc} line 13 and the GND line 14, and the freedom of wiring is not at all limited by the existence of the V_{cc} line 13 and the GND line 14. Suppose that the V_{cc} line 13 and the GND line 14 are extended at the center of the cell 10, then, the wiring in the Y direction among the internal wiring so the basic cell array (I, I' . . .) must step over the V_{cc} line and the GND line, and hence a two-layered wiring must be employed. Therefore, the freedom of wiring drops and the wiring structure becomes extremely complicated.

Even when the bipolar elements Q_1, Q_2 are disposed of both external sides (above and below the cell) of MOSFETs (M_1~M_6) as in the present invention, the gate width W of the MOSFET (M_1~M_6) is reduced by several dozens of μm in comparison with that of a pure CMOS cell, and this means that the bipolar elements Q_1, Q_2 are disposed afresh in this reduced region. Thus, the increase of the occupying area of the basic cell due to the disposition of the bipolar elements Q_1, Q_2 can be minimized.

Furthermore, since the widths W_I, W'_I of the basic cell arrays I, I' must be such that some dozens of aluminum first layer wirings 34 (e.g., 16, that is, 16 channels) in the X direction among the internal wirings of the basic cell arrays I, I' can be extended, the construction which permits to dispose the bipolar elements in the Y direction provides the advantage that sufficient W_I, W_I' can be secure, and it becomes possible to cope with the increase of channels of the internal wirings of the basic array due to the miniaturization of the cell. As described above, the present invention can provide IC which requires less consumed power, operates at a high operating speed and has a high integration density.

The present invention can be applied suitably to ICs which have a plurality of cells and must utilize them efficiently, particularly to gate arrays.

Claims

1. A semiconductor integrated circuit device comprising:

basic cells (10), each including a first kind of elements (Q_1, Q_2) having a high load driving capacity and a second kind of elements (M_1 to M_6) having a driving capacity lower than that of said first kind of elements (Q_1, Q_2);

basic cell arrays, each formed by disposing a plurality of said basic cells (10) in a predetermined first direction (X);

a basic cell matrix formed by disposing a plurality of said basic cell arrays in a second

region II is a wiring region in which the first layer aluminum wiring (microcell wiring) in the X direction is extended.

The above explains the basic construction of the gate array.

Next, the effect of the present invention and the reason why such an effect can be obtained will be described.

As described already, the basic cell is actually a 2-input NAND gate, but it incorporates therein one more gate and hence functions substantially as a 3-input NAND gate.

The planar layout condition of the basic cell is shown in Fig. 2(a), and when such a modified 2-input construction is employed, the cell occupying area can be reduced for the following reasons.

Referring to Figs. 11(b), (e) and (h), the cell area increases in the case of (b) because the gate is formed in such a manner as to extend rightward of the bipolar element (the portion represented by symbol Xa). Studies made by the present inventor reveal that while $l_1 = 32$ µm in the drawing, $l_1 + l_2$ becomes 40 µm. Therefore, if the modified 2-input cell is used, the cell area can be reduced by 20%.

According to the construction described above, the effective utilization efficiency of the cell can also be improved.

In other words, when one circuit (macrocell) is formed, the wiring freedom can be much improved and the number of gates can be reduced by use of the 3-input NAND type cell than by use of the 2-input NAND type cell because the number of input terminals of the former is greater than that of the latter and the freedom of wiring can be improved as much. From the aspect of the cell utilization efficiency, however, the wiring channel number becomes greater in the case of the 3-input NAND, and when various macrocells are constituted, the extension of the Al wirings becomes a critical problem that the number of waste cells becomes greater and the chip area increases, on the contrary.

The modified 2-input cell described above becomes substantially a 3-input NAND type cell when the second signal input terminal incorporated therein is connected by an internal wiring inside the basic cell array. Therefore, the number of gates of the circuit construction can be reduced, and since the third signal input terminal is never connected to the wiring extended in the extension region, the wiring channel number is the same as when the 2-input NAND type cell is used. As a result, the increase of the chip area due to the increase of the channel number can be prevented.

As described above, one of the characterizing features of the present invention resides in that the reduction of the occupying area of one cell itself and the improvement in the cell utilization efficiency can be accomplished by a simple circuit construction.

The present invention has another feature.

As shown in Fig. 12, the bipolar elements are disposed both outsides of MOSFET, so that the V_{cc} line 13 and the GND line 14 are vertically extended in parallel with the basic cell array. In other words, two NPN transistors Q_1 and Q_2 of a totem pole connection at the output stage in the basic cell are disposed on both sides of MOSFET, and along with this arrangement, the V_{cc} line and the GND line extend above and below the cell. Then, it is possible to freely extend the first layer Al wiring in the same way in the center portion of the basic cell 10 is parallel with the basic cell array, that is, the region interposed between the V_{cc} line 13 and the GND line 14, and the freedom of wiring is not at all limited by the existence of the V_{cc} line 13 and the GND line 14. Suppose that the V_{cc} line 13 and the GND line 14 are extended at the center of the cell 10, then, the wiring in the Y direction among the internal wiring so the basic cell array (I, I' . . .) must step over the V_{cc} line and the GND line, and hence a two-layered wiring must be employed. Therefore, the freedom of wiring drops and the wiring structure becomes extremely complicated.

Even when the bipolar elements Q_1, Q_2 are disposed of both external sides (above and below the cell) of MOSFETs ($M_1 \sim M_6$) as in the present invention, the gate width W of the MOSFET ($M_1 \sim M_6$) is reduced by several dozens of µm in comparison with that of a pure CMOS cell, and this means that the bipolar elements Q_1, Q_2 are disposed afresh in this reduced region. Thus, the increase of the occupying area of the basic cell due to the disposition of the bipolar elements Q_1, Q_2 can be minimized.

Furthermore, since the widths W_l, W'_l of the basic cell arrays I, I' must be such that some dozens of aluminum first layer wirings 34 (e.g., 16, that is, 16 channels) in the X direction among the internal wirings of the basic cell arrays I, I' can be extended, the construction which permits to dispose the bipolar elements in the Y direction provides the advantage that sufficient W_l, W_l' can be secure, and it becomes possible to cope with the increase of channels of the internal wirings of the basic array due to the miniaturization of the cell. As described above, the present invention can provide IC which requires less consumed power, operates at a high operating speed and has a high integration density.

The present invention can be applied suitably to ICs which have a plurality of cells and must utilize them efficiently, particularly to gate arrays.

Claims

1. A semiconductor integrated circuit device comprising:

basic cells (10), each including a first kind of elements (Q_1, Q_2) having a high load driving capacity and a second kind of elements (M_1 to M_6) having a driving capacity lower than that of said first kind of elements (Q_1, Q_2);

basic cell arrays, each formed by disposing a plurality of said basic cells (10) in a predetermined first direction (X);

a basic cell matrix formed by disposing a plurality of said basic cell arrays in a second

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direction (Y) substantially vertical to said first direction (X) with predetermined gaps (W_1) between the basic cell arrays;

wherein said first kind of elements (Q_1, Q_2) are disposed at peripheral portions in said basic cells (10) in said second direction (Y), and said second kind of elements (M_1 to M_6) are disposed at the center portions of said basic cells (10);

first operating potential lines (13) and second operating potential lines (14) for applying operating potentials (V_{cc}; GND) to said basic cells (10), wherein said first and second operating potential lines (13, 14) are arranged in said basic cell matrix substantially in said first predetermined direction (X) in parallel with said basic cell arrays, passing both peripheries of each of said basic cells (10) in said second direction (Y) and being connected to said first kind of elements (Q_1, Q_2);

first wirings (I_{IN}) disposed in said basic cell arrays, connecting said first and second kinds of elements (Q_1, Q_2; M_1 to M_6) to form a basic composite circuit and connecting said basic cells (10) constituting each basic cell array; and

second wirings (500, 510) disposed in regions of said predetermined gaps (W_1) between said basic cell arrays and used for transmitting signals between said basic cell arrays and between unit cells constituted by several of said basic composite circuits;

each of said basic cells (10) including *m* first signal input terminals (IN_3) that can be connected only to said first wirings (I_{IN}) disposed inside said basic cell arrays and *n* second signal input terminals (IN_1, IN_2) that can be connected to said second wirings (500, 510).

2. A semiconductor integrated circuit device according to claim 1, wherein said first wirings (I_{IN}) consist of a conductive material of the same layer (Al_1) as first and second operating potential lines (13, 14).

3. A semiconductor integrated circuit device according to claim 1 or 2, wherein said first kind of elements are bipolar transistor (Q_1, Q_2) and said second kind of elements are insulated gate field effect transistors (M_1 to M_6).

4. A semiconductor integrated circuit device according to claim 3, wherein each of said basic cells (10) consists of two bipolar transistors (Q_1, Q_2) and three CMOS, and the emitter-collector paths of said two bipolar transistors (Q_1, Q_2) are interposed in series with each other between said first and second operating potentials (V_{cc}; GND).

5. A semiconductor integrated circuit device according to claim 4, wherein said two bipolar transistors (Q_1, Q_2) are NPN transistors.

6. A semiconductor integrated circuit device according to claim 4 or 5, wherein the gates of a CMOS (M_1 to M_6) are arranged in said second direction (Y), comprising a first gate, a second gate and a third gate having an effective gate length smaller than that of said first gate and said second gate in the second direction (Y).

7. A semiconductor integrated circuit device according to claim 6, wherein the circuit constituted by all of said elements of one basic cell is a 3-input NAND circuit having three input terminals (IN_1, IN_2; IN_3), two of which (IN_1, IN_2) can be connected only to said second wirings (500, 510), while the other one (IN_3) can be connected only to said first wirings (I_{IN})..

8. A semiconductor integrated circuit device according to claim 7, wherein said first signal input terminal (IN_1) is the end portion of said first gate, and said second signal input terminal (IN_2) in the end portion of said second gate.

9. A semiconductor integrated circuit device according to any one of claims 6 to 8, wherein said gates consist of polysilicon.

Patentansprüche

1. Integrierte Halbleiterschaltung, umfassend

Grundzellen (10), deren jede Elemente (Q_1, Q_2) einer ersten Art mit hohem Lasttreibvermögen und Elemente (M_1 bis M_6) einer zweiten Art mit gegenüber den Elementen (Q_1, Q_2) der ersten Art kleinerem Lasttreibvermögen enthält.

Grundzellen-Gruppierungen, deren jede durch Anordnen mehrerer Grundzellen (10) in einer vorgegebenen ersten Richtung (X) gebildet ist,

eine Grundzellen-Matrix, die durch Anordnen mehrerer Grundzellen-Gruppierungen in einer zu der ersten Richtung (X) im wesentlichen senkrechten zweiten Richtung (Y) mit vorgegebenen Abständen (W_1) zwischen den Grundzellen-Gruppierungen gebildet ist,

wobei die Elemente (Q_1, Q_2) der ersten Art in Randbereichen der Grundzellen (10) in der zweiten Richtung (Y) und die Elemente (M_1 to M_6) der zweiten Art in Mittelbereichen der Grundzellen (10) angeordnet sind,

erste Arbeitspotentialleitungen (13) und zweite Arbeitspotentialleitungen (14) zur Zuführung von Arbeitspotentialen (V_{cc}; GND) an die Grundzellen (10), wobei die ersten und die zweiten Arbeitspotentialleitungen (13, 14) in der Grundzellen-Matrix im wesentlichen in der ersten vorgegebenen Richtung (X) parallel zu den Grundzellen-Gruppierungen verlaufen, beide Ränder jeder der Grundzellen (10) in der zweiten Richtung (Y) passieren und mit den Elementen (Q_1, Q_2) der ersten Art verbunden sind,

erste in den Grundzellen-Gruppierungen angeordnete Verdrahtungen (I_{IN}), die die Elemente (Q_1, Q_2; M_1 bis M_6) der ersten und der zweiten Art unter Bildung einer zusammengesetzten Grundschaltung sowie die die einzelnen Grundzellen-Gruppierungen bildenden Grundzellen (10) verbinden, und

in Bereichen der vorgegebenen u in Bereichen der vorgegebenen Abstände (W_1) zwischen den Grundzellen-Gruppierungen angeordnete zweite Verdrahtungen (500, 510), die zur Übertragung von Signalen zwischen den Grundzellen-Gruppierungen und zwischen von mehreren der zusammengesetzten Grundschaltungen gebildeten Einheitszellen dienen,

wobei jede der Grundzellen (10) *m* erste Signaleingangsklemmen (IN_3), die nur mit den innerhalb der Grundzellen-Gruppierungen ange-

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ordneten ersten Verdrauhtungen (I_{IN}) verbindbar sind, und *n* mit den zweiten Verdrahtungen (500, 510) verbindbare zweite Signaleingangsklemmen (IN_1, IN_2) aufweist.

2. Integrierte Halbleiterschaltung nach Anspruch 1, wobei die ersten Verdrahtungen (I_{IN}) aus einem leitfähigen Material der gleichen Schicht Al1) wie die ersten und die zweiten Arbeitspotentialleitungen (13, 14) bestehen.

3. Integrierte Halbleiterschaltung nach Anspruch 1 oder 2, wobei die Elemente der ersten Art Bipolartransistoren (Q_1, Q_2) und die der zweiten Art Isolierschicht-Feldeffekttransistoren (M_1 bis M_6) sind.

4. Integrierte Halbleiterschaltung nach Anspruch 3, wobei jede der Grundzellen (10) aus zwei Bipolartransistoren (Q_1, Q_2) und drei CMOS-Giedern besteht und die Emitter-Kollektor-Strekken der beiden Bipolartransistoren (Q_1, Q_2) in Serie miteinander zwischen das erste und das zweite Arbeitspotential (V_{cc}; GND) eingeschaltet sind.

5. Integrierte Halbleiterschaltung nach Anspruch 4, wobei die beiden Bipolartransistoren (Q_1, Q_2) NPN-Transistoren sind.

6. Integrierte Halbleiterschaltung nach Anspruch 4 oder 5, wobei die Gates eines CMOS-Gliedes (M_1 bis M_6) in der zweiten Richtung (Y) angeordnet sind, mit einem ersten Gate, einem zweiten Gate und einem dritten Gate, das in der zweiten Richtung (Y) eine geringere effektive Gate-Länge aufweist als das erste und das zweite Gate.

7. Integrierte Halbleiterschaltung nach Anspruch 6, wobei die von sämtlichen Elementen einer Grundzelle gebildete Schaltung eine NAND-Stufe mit drei Eingangsklemmen (IN_1, IN_2; IN_3) ist, von denen zwei (IN_1, IN_2) nur mit den zweiten Verdrahtungen (500, 510) und die weitere (IN_3) nur mit den ersten Verdrahtungen (I_{IN}) verbindbar sind.

8. Integrierte Halbleiterschaltung nach Anspruch 7, wobei die erste Signaleingangsklemme (IN_1) der Endabschnitt des ersten Gates und die zweite Signaleingangsklemme (IN_2) der Endabschnitt des zweiten Gates ist.

9. Integrierte Halbleiterschaltung nach einem der Ansprüche 6 bis 8, wobei die Gates aus Polysilicium bestehen.

Revendications

1. Dispositif de circuit intégré à semiconducteurs comportant:

des cellules fondamentales (10) comprenant chacune un premier type d'éléments (Q_1, Q_2) possédant une capacité de commande de charge élevée et un second type d'éléments (M_1 à M_6) possédant une capacité de commande inférieure à celle dudit premier type d'éléments (Q_1, Q_2);

des rangées de cellules fondamentales, formées chacune en disposant une pluralité desdites cellules fondamentales (10) dans une première direction prédéterminée (X);

une matrice de cellules fondamentales formée en disposant une pluralité desdites rangées de cellules fondamentales dans une seconde direction (Y) sensiblement perpendiculaire à ladite première direction (X) avec des intervalles prédéterminés (W_1) entre les rangées de cellules fondamentals;

dans lequel les éléments dudit premier type (Q_1, Q_2) sont disposés en des parties périphériques dans lesdites cellules fondamentales (10) dans ladite seconde direction (Y), et les éléments dudit second type (M_2 à M_6) sont disposés aux parties centrales desdites cellules fondamentales (10);

des premières lignes de potential de fonctionnement (13) et des secondes lignes de potential de functionnement (14) pour appliquer des potentiels de fonctionnement (V_{cc}; GND) auxdites cellules fondamentales (10), dans lequel lesdites premières et secondes lignes de potentiel de fonctionnement (13, 14) sont disposées dans ladite matrice de cellules fondamentales sensiblement selon ladite première direction prédéterminée (X) en parallèle avec lesdites rangées de cellules fondamentales, traversant les deux périphéries de chacune desdites cellules fondamentales (10) dans ladite seconde direction (Y) et étant reliées audit premier type d'éléments (Q_1, Q_2);

des premiers câblages (I_{IN}) disposés dans lesdits réseaux de cellules fondamentales, reliant lesdits premier et second types d'éléments (Q_1, Q_2; M_1 à M_6) pour former un circuit composite fondamental et reliant lesdites cellules fondamentales (10) constituant chaque rangée de cellules fondamentales; et

des seconds câblages (500, 510) disposés dans les zones desdits intervalles prédéterminés (W_1) entre lesdites rangées de cellules fondamentales et utilisés pour transmettre des signaux entre lesdits réseaux de cellules fondamentales et entre des cellules unitaires constituées par plusieurs desdits circuits composites fondamentaux;

chacune desdites cellules fondamentales (10) comprenant *m* premières bornes d'entrée de signal (IN_3) qui pevuent être reliées uniquement auxdits premiers câblages (I_{IN}) disposés à l'intérieure desdites rangées de cellules fondamentales et *n* secondes bornes d'entrée de signal (IN_1, IN_2) qui peuvent être reliées ausdits seconds câblages (500, 510).

2. Dispositif de circuit intégré à semiconducteurs selon la revendication 1, dans lequel lesdits premiers câblages (I_{IN}) consistent en un matériau conducteur de la même couche (Al1) que lesdites premières et secondes lignes de potentiel de fonctionnement (13, 14).

3. Dispositif de circuit intégré à semiconducteurs selon la revendication 1 ou 2, dans lequel lesdits éléments du premier type sont des transistors bipolaires (Q_1, Q_2) et lesdits éléments du second type d'éléments sont des transistors à effet de champ à grille isolée (M_1 à M_6).

4. Dispositif de circuit intégré à semiconducteurs selon la revendication 3, dans lequel chacune desdites cellules fondamentales (10)

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consiste en deux transistors bipolaires (Q_1, Q_2) et trois CMOS, et les trajets émetteur-collecteur desdits deux transistors bioplaires (Q_1, Q_2) sont interposés en série chacun avec l'autre entre lesdits premier et second potentiels de fonctionnement (V_{cc}; GND).

5. Dispositif de circuit intégré à semiconducteurs selon la revendication 4, dans lequel lesdits deux transistors bipolaires (Q_1, Q_2) sont des transistors NPN.

6. Dispositif de circuit intégré à semiconducteurs selon la revendication 4 ou 5, dans lequel les grilles d'un transistor CMOS (M_1 à M_6) sont disposées dans ladite seconde direction (Y), comportant une première grille, une seconde grille et une troisième grille possédant une longueur de grille effective inférieure à celle de ladite première grille et de ladite seconde grille dans la seconde direction (Y).

7. Dispositif de circuit intégré à semiconducteurs selon la revendication 6, dans lequel le circuit constitué par la totalité desdits éléments d'une cellule fondamentale est un circuit NONET à trois entrées possédant trois bornes d'entrée (IN_1, IN_2; IN_3), dont deux (IN_1, IN_2) peuvent être reliées seulement auxdits seconds câblages (500, 510), tandis que l'autre (IN_3) peut être reliée seulement auxdits premiers câblages (I_{IN}).

8. Dispositif de circuit intégré à semiconducteurs selon la revendication 7, dans lequel ladite première borne d'entrée de signal (IN_1) est la partie terminale de ladite première grille, et ladite seconde borne d'entrée de signal (IN_2) est la partie terminale de ladite seconde grille.

9. Dispositif de circuit intégré à semiconducteurs selon l'une quelconque des revendications 6 à 8, dans lequel lesdites grilles sont en silicium polycristallin.

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