Description

This invention relates to a large screen display apparatus made up of a number of light emitting elements which is installed mainly at outdoor stadiums or the like.

In general, in a large screen display apparatus of this type, a display section is made up of a number of single picture element light emitting elements which are CRTs or light bulbs. In a color display apparatus, three kinds of single picture element light emitting elements; i.e., red (R), green (G) and blue (B) single picture elements are arranged regularly, or a number of single picture element light emitting elements including three colors, red, green and blue, are arranged in matrix form. More specifically, the display apparatus comprises a number of units including a plurality of light emitting elements and an electronic circuit for driving them, and is provided with a control device for controlling the display operation and a power source.

Fig. 1 shows one example of such a conventional display apparatus. In Fig. 1, reference numeral 30 designates a screen of the display apparatus; 3, units forming the screen 30; 6, a housing which accommodates a plurality of units 3, thus forming the screen; 13, a power source; and 29, a display control section for controlling the units 3 of the screen 30.

Fig. 2 is a block diagram showing the arrangement of the display control section 29. In Fig. 2, reference numeral 26 designates an analog-to-digital converter for converting an input video signal into a digital signal (hereinafter referred to an "an A/D converter", when applicable); 15, a frame memory for storing video signals digitized; 16, an on-off decision section connected to the frame memory 15; 27, a column selecting circuit connected to the on-off decision section, for selecting a column in the screen 30; 28, a line selecting circuit for selecting a line in the screen 30; 18, an address control section for performing the address control of the line selecting circuit and the frame memory 15; 22, a timing control section for performing the timing control of the A/D converter 26; and 32, single picture element light emitting elements forming the above-described units 3.

The operation of the display apparatus thus constructed will be described. A video signal applied to the display apparatus is converted into a predetermined digital signal by the A/D converter 26, which is stored in the frame memory 15. The data stored in the frame memory 15 are read out according to addresses corresponding to the single picture element light emitting elements so as to be converted into on-off signals successively, which are supplied to the light emitting elements 32 which are specified by the column selecting circuit 27 and the line selecting circuit 28. Each single picture element light emitting element 32 has a function of storage, and the on-off signal supplied to the single picture element light emitting element 32 is held thereby until another signal is supplied thereto. With respect to the contents of the frame memory 15, the data of each field are read out a plurality of times and converted into predetermined on-off signals so as to be displayed, and the accumulation of "on" time in one field is proportional to the amplitude of a video signal to be displayed by the single picture element light emitting elements 32.

A variety of screens 30 different in size can be provided by changing the arrangement of the units 3. The control device 29 can control the variety of screens.

The conventional display apparatus is designed as described above. Therefore, the resolution cannot be increased without increasing the density in arrangement of single picture element light emitting elements which are smaller in size. Accordingly, the number of single picture element light emitting elements used is extremely large, and at the same time the numbers of drive circuits and other peripheral circuits are unavoidably large. The manufacturing cost may be reduced by miniaturizing the single picture element light emitting elements; however, the amount of reduction is considerably small. And in this case, the drive circuits and the peripheral circuits should be miniaturized. Therefore, it is considerably difficult to increase the resolution, and to decrease the manufacturing cost, the weight and the width of the display apparatus at the same time.

Conversion of digital data stored in memory into those having predetermined time widths is one of the most important signal processing operations in the display apparatus. If the signal processing sections, which are heretofore located at a position, are assigned to the modules, respectively, then the manufacturing cost of the display apparatus is increased.

According to the present invention there is provided a large screen display means formed by arranging a plurality of display modules;
each of said modules being formed from a plurality of units arranged in a bidirectional matrix form of p rows x q columns (where p and q are positive integers), a power source and a control circuit, and wherein each of said units is formed from light emitting elements, each light emitting element being formed from a plurality of light emitting parts arranged in a matrix form of k rows x l columns (where k and l are positive integers), said light emitting elements being arranged in a matrix form of m rows x n columns (where m and n are positive

integers) to form said unit; and
a housing means to accommodate the display means; and
a drive circuit to drive the display means.

In this way, the invention is able to provide a large screen display apparatus which is high in resolution, low in manufacturing cost, and small both in thickness and weight.

The invention is also able to provide a large screen display apparatus which is capable of displaying a half-tone image, in which the time width of a digital signal can be controlled with a simple circuit.

The invention and its embodiments are described in the following detailed description with reference to the drawings, in which:

Fig. 1 is an explanatory diagram showing the entire arrangement of a conventional display apparatus.

Fig. 2 is a block diagram showing the arrangement of a display control section of the conventional display apparatus.

Fig. 3 is an explanatory diagram showing the entire arrangement of a display apparatus which is one embodiment of this invention.

Fig. 4 is a sectional view illustrating the structure of a fluorescent display tube which is one example of a light emitting element of the display apparatus according to the present invention.

Fig. 5 is an explanatory diagram showing the arrangement of the control electrodes of the fluorescent display tube.

Fig. 6 is a block diagram showing the arrangement of a module in the display apparatus.

Fig. 7 is a perspective view, with parts cut away, showing the construction of the display apparatus.

Fig. 8 is a block diagram showing a control circuit in the module.

Figs. 9 and 10 are time charts showing the timing of transmission of data with a common signal line.

Fig. 11 is a block diagram showing the arrangement of the modules and a signal supplying means in the display apparatus.

Fig. 12 is a time chart showing signals applied to the light emitting element.

Fig. 13 is a diagram showing a display section to which the technical concept of the invention is applied.

Fig. 14 is a block diagram of a display control section in Fig. 1.

Fig. 15 is a block diagram showing a part of the control circuit for a unit.

Figs. 16, 18 and 19 are time charts for a description of the operation of the display apparatus according to the invention.

Fig. 17 is a diagram showing applications of the invention.

One embodiment of this invention will be described with reference to the accompanying drawings.

Fig. 3 is a block diagram showing the entire arrangement of a display apparatus according to the invention. In Fig. 3, reference numeral 1 designates light emitting elements each comprising light emitting parts 2 arranged in a matrix form of k (vertically) × l (horizontally) {k and l being positive integers (k = 4 and l = 4 in Fig. 3)}. Further in Fig. 3, reference numeral 3 designates units each comprising the light emitting elements 1 arranged in a matrix form of m (vertically) × n (horizontally) {m and n being positive integers (m = 4 and n = 4 in Fig. 4)}. Reference numeral 4 designates a module comprising the units 3 arranged in a matrix form of p (vertically) × q (horizontally) p and q being positive integers (p = 2 and q = 2 in Fig. 3). Reference numeral 5 designates module groups each comprising the modules 4 arranged vertically; 6, a housing; and 30, a screen formed by arranging the module groups 5 horizontally in the housing 6. The light emitting elements 1 are dot matrix type display elements such as liquid crystal elements or fluorescent display tubes. The display is controlled by controlling two kinds of electrodes, namely, first and second electrodes which are crossed by one another.

The display apparatus of the invention will be described with reference to the case where the fluorescent display tubes are employed as the light emitting elements. Fig. 4 is a sectional view illustrating the internal structure of the fluorescent display tube. In Fig. 4, reference numeral 9 designates a cathode for emitting thermions; 8, grids for accelerating the electrons; 7, anodes coated with fluorescent material; 10, conductors for applying voltage to the anodes; 11, a gas discharging outlet; and 12, connecting pins which are to be connected to external circuits. In the fluorescent display tube, the fluorescent material on the anodes 7 emits light when thermions from the cathode strike against the anodes 7. The anodes 7 are controlled by voltages applied through the conductors 10. The anode 7 correspond to the aforementioned first control electrodes, and the grids 8 to the second control electrodes.

Fig. 5 is a diagram for a description of the arrangement of the control electrodes adapted to control a display operation. The grids 8 are connected in four lines Y_1 through Y_4, and the anodes 7 are connected in four columns X_1 through X_4; that is, the grids 8 and the anodes 7 are arranged in matrix form so that the display operations of the light emitting parts at the intersections of the first and second control electrodes are controlled. When

it is required to form a full-color display apparatus, the light emitting elements should be such that three kinds of fluorescent materials, i.e, red, green and blue fluorescent materials are applied, in a regular pattern, to the anodes. If the R, G and B light emitting parts 2 are arranged in the ratio of R : G : B = 1 : 2 : 1 and the arrangement of picture elements as shown in Fig. 3 is employed, then a color display apparatus high in resolution can be obtained.

Each of the units 3 is made up of the light emitting elements 1 such as fluorescent display tubes including a plurality of picture elements, and drive circuits including shift registers and latch circuits on a substrate. The control electrodes of each of the light emitting elements are arranged in matrix form, as was described above. Therefore, the number of electrodes 12 extended out of the light emitting elements 1 and the number of drive circuits can be decreased, and therefore the unit 3 can be simplified.

Each of the modules 4, as shown in Fig. 6, comprises: a plurality of units 3; a control circuit 31 for controlling the units 3; and a power source 13. Referring back to Fig. 1, in the conventional display apparatus, the display control section 29 and the power source 13 are provided outside of the screen 30, and are so designed as to be able to control a variety of screens different in size, and the circuitry is accordingly, intricate. On the other hand, in the display apparatus of the invention, the control circuits 31 are provided for the modules 4, respectively; that is, the control range of each control circuit 31 is limited to its own module, and therefore the control circuits 31 are simplified in circuitry, especially when the number (k × l) of light emitting parts 2 in each light emitting element 1, the number (m × n) of light emitting elements in each unit 3. The number (p × q) of units 3 in each module 4 are so determined as to meet $k = 2^r$, $l = 2^s$, $m = 2^t$, $n = 2^u$, $p = 2^v$, and $q = q^w$ (where r and s are positive integers, and t, u, v and w are integers which are not negative); that is, these numbers are so selected as to be effective in processing digital signals, then control circuits 31 can be efficiently formed.

In Fig. 11, reference numeral 24 designates buffers connected to the signal lines 14, for shaping signals; 25, terminal sections for preventing the deformation of the waveforms of signals on the signal lines 14; A/D (analog-to-digital) converter 26 for converting an input video signal into a digital signal, i.e., predetermined display data and 21, buffer memories provided respectively for the module groups 5. The buffer memories 21 operate to store the output display data of the A/D converter 26 for speed conversion, and to deliver the display data together with address data to the respective module group 5, and to form two kinds of timing signals for receiving the display data and the address data. Further in Fig. 11, reference numeral 22 designates a timing signal generating section connected to the A/D converter 26 and the buffer memories 21; and 20, signal supplying means comprising the A/D converter 26, the buffer memories 21 and the timing signal generating section 22. Fig. 8 is a block diagram showing the arrangement of the control circuit 31. In Fig. 8, reference numeral 15 designates a frame memory corresponding to the picture frame of the module 4; 43, an address selector for the frame memory 15; 16, an on-off decision section connected to the frame memory 15; 19, a unit selecting gate connected to the on-off decision section for selectively activating the units 3; and 18, an address control section connected to the address selector 43, the on-off decision section 16 and the unit selecting gate 19. Further in Fig. 8, reference numeral 17 designates a timing control section connected to the address control section 18, the unit selecting gate 19 and the address selector 43, 33, an address setting switch; 40, an address latch section; 41, a comparator for comparing the address separated by the address latch section 40 with the module address set by the address setting switch; 45, a NAND gate which is operated by the output of the comparator; and 42, and address counter. The address counter 42 is driven by the output signal of the NAND 45 which receives both the output signal of the comparator 41 and the signal obtained by inverting a timing signal provided through a timing signal line (DWT).

As shown in Fig. 7, the control circuits 31 together with the power sources 3 are positioned behind the units forming the modules 4, and are connected vertically with the signal lines 14. The signal supplying means 20 for supplying signal to the signal lines 14, and power distributing means 33 for supplying power to the power sources 13 are accommodated in the frame 6 of the screen 30, which makes the display apparatus compact in construction.

The control circuit 31 is combined with the units 3 so that the data written in the frame memory 15 are divided into parts having predetermined time widths which are applied to the display controlling on-off decision section 16, to control the unit selecting gate 19. With respect to the contents of the frame memory 15, a data reading operation for data display and a data writing operation for display renewal are controlled in a time division manner, and writing addresses and reading address are selected by the address selector 43. The data are supplied through the common signal line 14 (including the data signal line and the timing signal lines DWT and ALE), and stored in pre-

determined addresses in the frame memory 15. The addresses and the data are transmitted, in multiplex form, through the common signal line 14, which reduces the number of signal lines. The address data and the display data are separated with the two kinds of timing signal lines ALE and DWT, so that the display data are written in the predetermined addresses. The reading operation should be described with reference to the arrangement of the display section.

Now, the operation of the display apparatus thus constructed will be described. A video signal sampled at high speed is applied to the signal supplying means 20, in which it is converted into a digital signal by the A/D converter 26, which is stored in the buffer memories 21 provided respectively for the module groups 5. The signals written in the buffer memories 21 at high speed are read out, as display data, at low speed, and are delivered to the module groups 5 together with address data for specifying the modules 4 to which the display data should be transmitted, and timing signals for determining the timing of reception of the display data and the address data. In each module group 5, the display data multiplex with the address data in time sharing manner are received by the buffer 24 and transmitted through the signal line 14 to the modules 4. In this case, the display data received by the buffer 24 is made low in speed being subjected to speed conversion by the buffer memory 21 as was described above, and therefore a flat cable can be used as the common signal line 14. The common signal line 14 is made up of a data signal line and two kinds of timing signal lines. The upper part of Fig. 9 shows the address data and the display data which are transmitted in a time-division multiplex mode, the middle part shows a timing signal (hereinafter referred to as "an ALE signal", when applicable) for determining the timing of reception of the address data transmitted through one of the timing signal lines, and the lower part shows a timing signal (hereinafter referred to as "a DWT signal", when applicable) for determining the timing of reception of the display data transmitted through the other timing signal line.

In each of the modules 4, the data and the timing signals transmitted through the signal line 14 are received by the control circuit 31. In the control circuit 31, the address latch section 40 separates the address data according to the ALE signal, and the address data thus separated is supplied to the comparator 41. In the comparator 41, the address data is compared with the address set for the modulate 4 by the address setting switch 33. only when the address data coincides with the address set by the switch 33, is the gate 45 opened. When the gate 45 is opened, the DWT signal is supplied through the gate 45 to the frame memory 15, so that a series of display data following the address data are written in the frame memory 15. In the address counter 42, the content there of is increased by the DWT signal, so that the display data writing address in the frame memory 15 is renewed and applied to the address selector 43.

The display data thus received and written in the frame memory 15 are read out a required number of times within a predetermined period of time and converted into on-off signals under the control of the address control section 18. The on-off signals thus formed are supplied through the unit selecting gate 19 to the units 3. In each unit 3, the display control is carried out in such a manner that the display data are arranged for the picture elements with the aid of shift registers. Thus, in each light emitting element, the light emitting parts 2 emit light beams with predetermined luminances.

In the above-described embodiment, first address data is transmitted, then a series of display data. However, the display apparatus may be so modified that, as shown in Fig. 10, address data and display data are transmitted alternately, and they are separated with the ALE signal and the DWT signal. In this modification the address counter in the control circuit 31 of Fig. 8 can be eliminated.

Fig. 12 is a time chart showing signals applied to the light emitting element 1, which is the fluorescent display tube in this case. Scanning signals different in timing are applied to four grids 8 as indicated by Y_1 through Y_4 in Fig. 12, and predetermined video signals are applied to the anodes 7 in synchronization with the scanning signals as indicated by X_1 through X_4, so that the light emitting parts 2 at the intersections are caused to emit light. In the matrix type light emitting element 1 as described above, it is impossible to control the light emitting parts 2 separately; that is, the light emitting parts 2 are controlled in time division manner separately according to the lines, i.e., separately according to the scanning lines, and therefore the display is made continuous by increasing the scanning speed. Half-tones are displayed by a method in which signals proportional in time width to the amplitudes of the video signals are applied to the anodes 7 thereby to vary the luminances of the light emitting parts 2.

Fig. 13 is a diagram showing the arrangement of the display section. In the display section, the picture elements are arranged in a matrix form of 2^a (vertically) $\times$ 2^b (horizontally).

Fig. 14 is a diagram showing essential circuit elements for reading data out of the frame memory 15 in Fig. 1, i.e., Fig. 14 shows components required essentially for display control. In this case, it is assumed that a reading address has been se-

lected for the frame memory 15, and therefore the address selector 43 is not shown in Fig. 14. In the frame memory 15, the addresses are specified by (a + b) signals lines arranged vertically and horizontally in correspondence to the number ($2^a \times 2^b$) of picture elements in the display section. In the embodiment, a = 5, and b = 5, and the address are specified with 10 bits; A_0 through A_9. In addition, the data are inputted with c bits, which means that a half-tone image having 2^c gradations can be displayed. In the embodiment, c = 6 is selected. In Fig. 14, reference numeral 16 designates an on-off decision section adapted to subject 6-bit data to comparison; 17, a timing control section for controlling the generation of clock signals; and 18, an address control section made up of a series of counters for frequency-dividing a clock signal to provide an output of (a + b + c) bits corresponding to the number of picture elements $2^a \times 2^b$ and the number of display gradations 2^c. The output bits of an address counter 42 are represented by x_0 through x_4, y_2 through y_4, y_0, y_1, and c_0 through c_5 beginning with the least significant bit. These bits x_0 through x_4, and y_0 through y_4 represent the addresses in the frame memory 15, and correspond to the arrangement of the picture elements in the display section as shown in Fig. 13. The display section, as shown in Fig. 13, is made up of four units 3 each of which comprises sixteen (16) light emitting elements l. In each unit 3, the light emitting elements 1 are controlled by a drive circuit provided on the same substrate.

Fig. 15 shows a part of the control circuit 31 for the units 3. The circuit shown in Fig. 15 is provided for each of the units 3. In the control circuit 31, it is necessary to send data to the units individually; however, data, a latch signal, and scanning signals are supplied to the units commonly, and clock signals CK_1 through CK_4 for arranging the data are applied to the units, respectively, so that each of the units receives the respective data with the aid of the clock signal applied thereto.

The operation of the control circuit 31 will be described in more detail. The output of the address control section 18 corresponds to an address in the frame memory 15. The data read is compared with the data (c_0 - c_5) of the on-off decision section 16 which is the output of the address control section 18. As a result of the comparison, 1-bit on-off data is provided which is "1" (corresponding to the "on" state of a picture element) when the data of the frame memory 15 is larger and "0" (corresponding to the "off" state) when the data is smaller. The data thus provided is applied to the respective picture element in the respective unit with the aid of the respective clock signal described above. On the other hand, as the clock signal is counted, the address control section 18 renews the address so that data are read out of the frame memory 15 successively. This operation is carried out repeatedly. In the circuit of Fig. 14, the data of the lines Y_1 are converted into on-off data, which are applied to the shift registers. The on-off data thus applied are simultaneously latched and held for a predetermined period of time thereby to drive the corresponding X electrodes (second control electrodes). At the same time, the scanning electrodes (control electrodes) Y_1 are driven for light emission (the Y electrodes being hereinafter referred to as "first control electrodes", when applicable). As the clock signals are further counted, the address control section 18 carries out the same operation for the line Y_2, Y_3 and Y_4 repeatedly so that display of an on-off binary image forming one picture is accomplished. The timing in this operation is as shown in Fig. 12. In the case of Fig. 14, the on-off decision data, 6 bits (c_0 - c_5), are allotted to six high-order bits of the output of the address control section 18. This means that, during one cyclic operation of the address control section, the binary image display is repeated sixty-four times with the output (c_0 - c_5) changing form (0 - 0) over to (1 - 1) as shown in Fig. 16, a time chart. In Fig. 16, reference characters T_1 through T_{64} designate the periods of time in which the output (c_0 - c_5) of the on-off decision section 16 is (0 - 0), (0 - 1), ... and (1 - 1), respectively. More specifically, in the period of time T_1, the data of the frame memory 15 is compared with the comparison data (((c_0 - c_5) - (0 - 0)) of the on-off decision section 16, as a result of which on-off data are provided and displaced as a binary image. In each of the remaining periods of time T_2 through T_{64}, the comparison data is increased by one "1", and with respect to the comparison data thus increased, the content of the frame memory 15 is converted into on-off data which are displayed as a binary image similarly as in the case of the period of time T_1. As was described above, during one cyclical operation of the address control section 18, the data in the frame memory 15 are read sixty-four times and compared with the sixty-four different binary data ranged from (0 - 0) to (1 - 1), so that sixty-four binary images are displayed. Therefore, in the display during one cyclical operation of the address control section 18, the sum of the periods of time in which the picture elements are placed in "on" state is proportional to the contents of the memory, and half-tone images having sixty-four gradations can be displayed. On the other hand, in a television signal according to the NTSC system, one field of picture is switched every 1/60 sec. Accordingly, in displaying a television signal as an image, data corresponding to one field are rewritten in the frame memory every 1/60 sec. Therefore, selecting the clock frequency

so as to allow the address control section 18 to achieve its one cyclical operation in 1/60 sec. permits the display of a television signal with sixty-four gradation. In the PAL system, one field corresponds to 1/50 sec., and therefore the clock frequency is 5/6 of that in the NTSC system.

The embodiment of the invention has been described with reference to the case where the display elements are operated on 1/4 duty dynamic drive for display control. However, the invention, being based on the relationships between the number of picture elements in the display section, the number of gradations of a half-tone image, and the number of outputs of the address control section 18, is effective irrespective of the display element drive system. The output of the address control section 18 may be allotted to the address or comparison data (c_0 - c_5) in various methods. Fig. 17 shows one example of these methods. The part (a) of Fig. 17 is provided for Fig. 14, with the timing as indicated in Fig. 16. As the lines specified by y_0 and y_1 are scanned simultaneously, y_0 and y_1 are allotted to the high-order bits of the output of the counter. The part (b) of Fig. 17 shows the allotment in the case where the display is controlled on 1/8 duty dynamic drive. In this operation, the timing is as indicated in Fig. 18. In this case, half-tone images are obtained by overlapping sixty-four different binary images. In the case of the part (c) of Fig. 17, similarly as in the case of Fig. 14, the display is controlled on 1/4 duty dynamic drive and y_0 and y_1 are allotted to the most significant bits. In this case, the data are read sixty-four times for every scanning-line drive period, and the time width conversion is carried out for every scanning line, so that a display having sixty-four gradations is carried out with one scanning operation with the timing as shown in Fig. 19.

As was described above, the video signal is processed for every module 4, and a complete image is displayed on the screen 30. In this operation, each of the modules 4 displays only a part of the image; that is, its display function is limited. However, each module has the control circuit 31 and the power source 13 which are essential for the display operation; that is, each module can operate as a display unit by itself. Therefore, the screen 30 which is an assembly of these modules 4 can be simplified in construction by modifying the construction of each module 4.

Further, each module 4 includes the control circuit 31 which is an essential signal processing element for a display operation, and the power source. if, under this condition, the signal supplying means 20 including the A/D converter 26 and the buffer memory 21, and the power distributing means 33 which receives electric power and distributes it to the modules are arranged inside the housing 6 of the screen 30, then all the necessary components are provided in the screen housing; that is, the resultant display apparatus is compact in construction. In the display apparatus of the invention, a plurality of light emitting elements each having a plurality of picture elements, in which a plurality of light emitting parts are arranged in matrix form are employed. The light emitting elements are arranged in a matrix form of $m \times n$, to form a unit and a plurality of the units are arranged in a matrix form of $p \times q$ (where m, n, p and q are positive integers) to form a module. A plurality of the modules are arranged to form the screen. Therefore, the functions of the display apparatus can be distributed to the light emitting elements, units and modules effectively. Furthermore, the light emitting elements are much lower in cost than the single picture element light emitting elements, the number of which is equal to that of the light emitting parts thereof. Therefore, according to the invention, a large screen display apparatus high in resolution can be realized without increasing the manufacturing cost, the weight and the thickness thereof.

The modules with the frame memories may be two-dimensionally arranged to form the large screen. In such a display apparatus, the addresses are assigned to the modules, respectively, and the modules are connected with the common signal lines so that the display data and the address data are supplied to the modules through the common signal lines. According to the address data, the display data for the modules are selected and stored in the frame memories, and the display data thus stored are used for display control. That is, each module carries out its own display control. Thus, in the display apparatus of the invention, the display control is performed with high efficiency. Accordingly, the display apparatus of the invention can readily cope with an increase in the quantity of data which may be caused when the screen size is increased or the resolution is increased. Furthermore, in the display apparatus of the invention, the picture elements are arranged in a matrix form of 2^a (vertically) $\times$ 2^b (horizontally) (where a and b are positive integers) in the display section; i.e., the number of picture elements is so limited as to be convenient in processing digital signals. Therefore in the display apparatus, the output of the address control section comprising a series of binary counters can be used as the control signal, and the simple circuit can effectively achieve the half-tone control while the address control section performs its one cyclical operation. If the invention is practiced as module control circuit, then the module control circuit itself is simplified, and 1-bit data arrangement may be employed for the units. In

addition, the units can be simplified in construction. Therefore, the large screen display apparatus can be reduced greatly in manufacturing cost and made compact in construction according to the invention.

Claims

1. A large screen display apparatus comprising:
   a display means formed by arranging a plurality of display modules (4);
   each of said modules (4) being formed from a plurality of units (3) arranged in a bidirectional matrix form of p rows x q columns (where p and q are positive integers), a power source (13) and a control circuit (31), and wherein each of said units (3) is formed from light emitting elements (1), each light emitting element being formed from a plurality of light emitting parts (2) arranged in a matrix form of k rows x l columns (where k and l are positive integers), said light emitting elements (1) being arranged in a matrix form of m rows x n columns (where m and n are positive integers) to form said unit (3); and
   a housing means (6) to accommodate the display means; and
   a drive circuit to drive the display means.

2. A large screen display apparatus as claimed in claim 1, wherein the number k of said light emitting parts (2) in each column and the number l of said light emitting parts (2) in each row satisfy the following equations:

   $k = 2^r$, and $l = 2^s$ (where r and s are positive integers),

   the number m of said light emitting elements (1) in each column and the number n of said light emitting elements (1) in each row satisfy the following equations:

   $m = 2^t$, and $n = 2^u$ (where t and u are positive integers), and

   the number p of said units (3) in each column and the number q of said units (3) in each row meet the following equations:

   $p = 2^v$, and $q = q^w$ (where v and w are positive integers).

3. A large screen display apparatus as claimed in claim 1 or 2, wherein control electrodes (7, 8) of said light emitting elements (1) for controlling said light emitting parts (2) comprise first control electrode groups (7) connected together in a first matrix direction and second control electrode groups (8) connected together in a second matrix direction and said light emitting parts (2) are arranged at the intersections of said first and second electrode groups (7, 8).

4. A large screen display apparatus as claimed in claim 1, 2 or 3, wherein said light emitting parts (2) of each light emitting element (1) are three kinds of light emitting parts (2) which are adapted to emit red (R), green (G) and blue (B) light respectively, and in each light emitting element (1) said light emitting parts are provided in a ratio of R : G : B = 1 : 2 : 1.

5. A large screen display apparatus as claimed in any one of the preceding claims wherein said housing (6) incorporates power distributing means (33) for receiving electric power and distributing said electric power to said modules (4).

6. A large screen display apparatus as claimed in any one of the preceding claims wherein said modules (4) are arranged to form a plurality of module groups (5), in each of which groups signal input sections of the modules (4) of the group are connected with a common signal line (14), and
   the module groups (5) are arranged to form a screen (30) of said display means.

7. A large screen display apparatus as claimed in claim 6, wherein said housing (6) incorporates signal supplying means (20) which receives a signal, converts said signal into a predetermined digital signal and supplies said digital signal to said common signal lines (14) of said module groups (5).

8. A large screen display apparatus as claimed in claim 7 wherein said module groups (5) which are assigned by respective addresses, are arranged one-dimensionally and wherein said module groups (5) are connected via the common signal lines (14) to the signal input means (20), said module groups (5) receiving respective display data transmitted through said signal lines (14), according to address data transmitted through said signal lines (14).

9. A large screen display apparatus as claimed in claim 8, wherein each of said common signal lines (14) comprises a data signal line and two kinds of timing signal lines, said display data and said address data being transmitted

addition, the units can be simplified in construction. Therefore, the large screen display apparatus can be reduced greatly in manufacturing cost and made compact in construction according to the invention.

Claims

1. A large screen display apparatus comprising:
   a display means formed by arranging a plurality of display modules (4);
   each of said modules (4) being formed from a plurality of units (3) arranged in a bidirectional matrix form of p rows x q columns (where p and q are positive integers), a power source (13) and a control circuit (31), and wherein each of said units (3) is formed from light emitting elements (1), each light emitting element being formed from a plurality of light emitting parts (2) arranged in a matrix form of k rows x l columns (where k and l are positive integers), said light emitting elements (1) being arranged in a matrix form of m rows x n columns (where m and n are positive integers) to form said unit (3); and
   a housing means (6) to accommodate the display means; and
   a drive circuit to drive the display means.

2. A large screen display apparatus as claimed in claim 1, wherein the number k of said light emitting parts (2) in each column and the number l of said light emitting parts (2) in each row satisfy the following equations:

   $k = 2^r$, and $l = 2^s$ (where r and s are positive integers),

   the number m of said light emitting elements (1) in each column and the number n of said light emitting elements (1) in each row satisfy the following equations:

   $m = 2^t$, and $n = 2^u$ (where t and u are positive integers), and

   the number p of said units (3) in each column and the number q of said units (3) in each row meet the following equations:

   $p = 2^v$, and $q = q^w$ (where v and w are positive integers).

3. A large screen display apparatus as claimed in claim 1 or 2, wherein control electrodes (7, 8) of said light emitting elements (1) for controlling said light emitting parts (2) comprise first control electrode groups (7) connected together in a first matrix direction and second control electrode groups (8) connected together in a second matrix direction and said light emitting parts (2) are arranged at the intersections of said first and second electrode groups (7, 8).

4. A large screen display apparatus as claimed in claim 1, 2 or 3, wherein said light emitting parts (2) of each light emitting element (1) are three kinds of light emitting parts (2) which are adapted to emit red (R), green (G) and blue (B) light respectively, and in each light emitting element (1) said light emitting parts are provided in a ratio of R : G : B = 1 : 2 : 1.

5. A large screen display apparatus as claimed in any one of the preceding claims wherein said housing (6) incorporates power distributing means (33) for receiving electric power and distributing said electric power to said modules (4).

6. A large screen display apparatus as claimed in any one of the preceding claims wherein said modules (4) are arranged to form a plurality of module groups (5), in each of which groups signal input sections of the modules (4) of the group are connected with a common signal line (14), and
   the module groups (5) are arranged to form a screen (30) of said display means.

7. A large screen display apparatus as claimed in claim 6, wherein said housing (6) incorporates signal supplying means (20) which receives a signal, converts said signal into a predetermined digital signal and supplies said digital signal to said common signal lines (14) of said module groups (5).

8. A large screen display apparatus as claimed in claim 7 wherein said module groups (5) which are assigned by respective addresses, are arranged one-dimensionally and wherein said module groups (5) are connected via the common signal lines (14) to the signal input means (20), said module groups (5) receiving respective display data transmitted through said signal lines (14), according to address data transmitted through said signal lines (14).

9. A large screen display apparatus as claimed in claim 8, wherein each of said common signal lines (14) comprises a data signal line and two kinds of timing signal lines, said display data and said address data being transmitted

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through said data signal line in a time-division multiplex mode, a timing signal for timing the receipt of said address data being transmitted through one of said two kinds of timing signal lines and a timing signal for timing the receipt of said display data being transmitted through the other, and

each of said modules (5) separates said display data and said address data from one another, according to said two timing signals.

10. A large screen display apparatus as claimed in any one of the preceding claims wherein said display means comprises a plurality of display modules (4) to display a complete picture.

11. A module for a large screen display apparatus as claimed in any one of the preceding claims in which (2^a x 2^b) light emitting parts are arranged in a bidirectional matrix form, the module comprising:

an address control section (18) for providing an output of (a+b+c) bits corresponding to the number (2^a x 2^b) of light emitting parts in said display means and the number (2^c) of display gradiations and for frequency-dividing a clock signal successively by factors ranged from 1/2 to $(1/2)^{a+b+c}$;

timing control means (17) for supplying the clock signal to the address control section (18);

a frame memory (15) which, being addressed with (a + b) bits, inputs and outputs data of c-bits; and

an on-off decision section (16) for subjecting said data of c-bits output from the frame memory (15) to a comparison with c-bits output from the address control section (18) and for applying 1-bit data representing "on" and "off" states of said light emitting parts to said light emitting parts and holding said data for a predetermined period of time to drive said display means.

Patentansprüche

1. Großbildschirm-Anzeigevorrichtung umfassend:

- ein Anzeigemittel, gebildet durch Anordnung einer Vielzahl von Anzeigemodulen (4);
- wobei jedes der Module (4) gebildet ist aus einer Vielzahl von Einheiten (3), die in Form einer bidirektionalen Matrix mit p Zeilen x q Spalten angeordnet sind (wobei p und q positive, ganze Zahlen sind) , aus einer Energiequelle (13) und einem Steuerschaltkreis (31), und eobei jede der Einheiten (3) aus lichtemittierenden Elementen (1) gebildet ist, wobei jedes lichtemittierende Element aus einer Vielzahl von lichtemittierenden Teilen (2) gebildet ist, die in Form einer Matris mit k Zeilen x l Spalten angeordnet sind (wobei k und l positive, ganze Zahlen sind), wobei die lichtemittierenden Elemente (1) in Form einer Matrix mit m Zeilen x n Spalten (wobei m und n positive, ganze Zahlen sind) angeordnet sind, um die Einheit (3) zu bilden;
- ein Gehäusemittel (6), um die Anzeigemittel aufzunehmen; und
- einen Ansteuerungsschaltkreis zur Ansteuerung des Anzeigemittels.

2. Großbildschirm-Anzeigevorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß die Anzahl k der lichtemittierenden Teile (2) in jeder Spalte und die Anzahl l der lichtemittierenden Teile (2) in jeder Zeile die folgenden Gleichungen erfüllen:

$k = 2^r$, und $l = 2^s$ (wobei r und s positive, ganze Zahlen sind),

die Anzahl m der lichtemittierenden Elemente (1) in jeder Spalte und die Anzahl n der lichtemittierenden Elemente (1) in jeder Zeile die folgenden Gleichungen erfüllen:

$m = 2^t$, und $n = 2^u$ (wobei t und u positive, ganze Zahlen sind), und

die Anzahl p der Einheiten (3) in jeder Spalte und die Anzahl q der Einheiten (3) in jeder Zeile die folgenden Gleichungen erfüllen:

$p = 2^v$, und $q = q^w$ (wobei v und w positive, ganze Zahlen sind).

3. Großbildschirm-Anzeigevorrichtung nach einem der Ansprüche 1 oder 2, dadurch gekennzeichnet, daß Steuerelektroden (7, 8) der lichtemittierenden Elemente (1) zum Steuern der lichtemittierenden Teile (2) erste Steuerelektrodengruppen (7), die in der ersten Matrixrichtung miteinander verbunden sind, und zweite Steuerelektrodengruppen (8) umfassen, die in einer zweiten Matrixrichtung miteinander verbunden sind, und die lichtemittierenden Teile (2) an den Schnittpunkten der ersten und zweiten Elektrodengruppen (7, 8) angeordnet sind.

4. Großbildschirm-Anzeigevorrichtung nach einem der Ansprüche 1, 2 oder 3, dadurch ge-

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kennzeichnet, daß die lichtemittierenden Teile (2) jedes lichtemittierenden Elements (1) drei Arten von lichtemittierenden Teilen (2) sind, die geeignet sind, rotes (R), grünes (G) bzw. blaues (B) Licht zu emittieren, und in jedem lichtemittierenden Element (1) die lichtemittierenden Teile in einem Verhältnis von R : G : B = 1 : 2 : 1 vorgesehen sind.

5. Großbildschirm – Anzeigevorrichtung nach einem der vorigen Ansprüche, dadurch gekennzeichnet daß das Gehäuse (6) Energieverteilungsmittel (33) umfaßt, um elektrische Energie aufzunehmen und sie an die Module (4) zu verteilen.

6. Großbildschirm – Anzeigevorrichtung nach einem der vorigen Ansprüche, dadurch gekennzeichnet, daß die Module (4) so angeordnet sind, um eine Vielzahl von Modulgruppen (5) zu bilden, in jeder dieser Gruppen Signaleingabebaugruppen der Module (4) der Gruppe mit einer gemeinsamen Signalleitung (14) verbunden sind, und die Modulgruppen (5) angeordnet sind, um einen Schirm (30) des Anzeigemittels zu bilden.

7. Großbildschirm – Anzeigevorrichtung nach Anspruch 6, dadurch gekennzeichnet, daß das Gehäuse (6) ein Signalzuführmittel (20) umfaßt, welches ein Signal erhält, das Signal in ein vorbestimmtes Digitalsignal umsetzt und das Digitalsignal an die gemeinsame Signalleitung (14) der Modulgruppen (5) zuführt.

8. Großbildschirm – Anzeigevorrichtung nach Anspruch 7, dadurch gekennzeichnet, daß die Modulgruppen (5) , denen entsprechende Adressen zugewiesen sind, eindimensional angeordnet sind und die Modulgruppen (5) über die gemeinsamne Signalleitungen (14) mit dem Signaleingabemittel (20) verbunden sind, wobei die Modulgruppen (5) die durch die Signalleitungen (14) übertragenen jeweiligen Anzeigedaten entsprechend Adreßdaten erhalten, die durch die Signalleitungen (14) übertragen werden.

9. Großbildschirm – Anzeigevorrichtung nach Anspruch 8, dadurch gekennzeichnet, daß jede der gemeinsamen Signalleitungen (14) eine Datensignalleitung und zwei Arten von Zeitsteuerungssignalleitungen umfaßt, wobei die Anzeigedaten und Adreßdaten durch die Datensignalleitung in einem Zeitmultiplexmodus übertragen werden, ein Zeitsteuerungssignal zur Zeitsteuerung des Adreßdatenempfangs durch eine der beiden Arten von Zeitsteuerungssignalleitungen übertragen wird, und ein Zeitsteuerungssignal zur Zeitsteuerung des Anzeigedatenempfangs durch die andere übertragen wird, und dadurch, daß jedes der Module (5) die Anzeige – und Adreßdaten entsprechend den beiden Zeitsteuerungssignalen voneinander trennt.

10. Großbildschirm – Anzeigevorrichtung nach einem der vorigen Ansprüche, dadurch gekennzeichnet, daß das Anzeigemittel eine Vielzahl von Anzeigemodulen (4) umfaßt, um ein vollständiges Bild anzuzeigen.

11. Modul für eine Großbildschirm – Anzeigevorrichtung nach einem der vorigen Ansprüche, in dem (2^a x 2^b) lichtemittierende Teile in Form einer bidirektionalen Matrix angeordnet sind, wobei das Modul umfaßt:
   - eine Adreßsteuerungsbaugruppe (18) zum Bereitstellen einer Ausgabe von (a + b + c) Bits, entsprechend der Anzahl (2^a x 2^b) der lichtemittierenden Teile in dem Anzeigemittel und der Anzahl (2^c) der Anzeigeabstufungen, und um sukzessive ein Taktsignal um Faktoren von 1/2 bis $(1/2)^{a+b+c}$ frequenzzuteilen:
   - Zeitsteuermittel (17) zum Zuführen des Taktsignals an die Adreßsteuergruppe (18);
   - einen Rahmenspeicher (15), mit (a + b) Bit adreßiert und mit Ein – und Ausgabedaten von c Bit;
   - eine Ein/Aus – Entscheidungsbaugruppe (16) um die c Bit – Ausgabedaten aus dem Rahmenspeicher (15) mit c Bit – Ausgabedaten aus der Adreßsteuergrinppe (18) zu vergleichen und den lichtemittierenden Teilen 1 – Bit – Daten einzuspeisen, die die Zustände "Ein" und "Aus" darstellen, und die Daten einen vorbestimmten Zeitraum zu halten, um das Anzeigemittel anzusteuern.

Revendications

1. Dispositif d'affichage à grand écran, comportant:

un moyen d'affichage obtenu en disposant une pluralité de modules d'affichage (4);

chacun desdits modules (4) étant formé d'une pluralité d'organes (3) disposés sous forme d'une matrice bidirectionnelle de p rangées x q colonnes (où p et q sont des entiers positifs),d'une source d'énergie 13 et d'un circuit de commande (31), et dispositif dans lequel chacun desdits organes (3) est formé d'éléments émetteurs de lumière (1), chaque

élément émetteur de lumière étant formé d'une pluralité de parties (2) émettrices de lumière, disposées sous forme d'une matrice de k rangées x l colonnes (où k et l sont des entiers positifs), lesdits éléments émetteurs de lumière (1) étant disposés soins forme d'une matrice de m rangées x n colonnes (où m et n sont des entiers positifs) pour former ledit organe (3); et

un moyen formant carrosserie (6) pour loger le moyen d'affichage; et

un circuit de pilotage pour piloter le moyen d'affichage.

2. Dispositif d'affichage à grand écran comme revendiqué dans la revendication 1, dans lequel le nombre k desdites parties émettrices de lumière (2) dans chaque colonne et le nombre l desdites parties émettrices de lumière (2) dans chaque rangée satisfont les équations suivantes :

$k = 2^r$, et $l = 2^s$ (où r et s sont des entiers positifs),

le nombre m desdits éléments émetteurs de lumière (1) dans chaque colonne et le nombre n desdits éléments émetteurs de lumière (1) dans chaque rangée satisfont les équations suivantes :

$m = 2^t$ et $n = 2^u$ (où t et u sont des entiers positifs), et

le nombre p desdits organes (3) dans chaque colonne et le nombre q desdits organes (3) dans chaque rangée satisfont les équations suivantes:

$p = 2^v$ et $q = 2^w$ (où v et w sont des entiers positifs).

3. Dispositif d'affichage à grand écran comme revendiqué dans la revendication 1 ou 2, dans lequel les électrodes de commande (7, 8) desdits éléments émetteurs de lumière (1) prévues pour commander lesdites parties émettrices de lumière (2) comportent des premiers groupes (7) d'électrodes de commande connectés ensemble dans une première direction de matrice et des second groupes (8) électrodes de commande connectés ensemble dans une seconde direction de matrice et dans lequel lesdites parties émettrices de lumière (2) sont disposées aux intersections desdits premiers et desdits seconds groupes d'électrodes (7, 8).

4. Dispositif d'affichage à grand écran comme revendiqué dans la revendication 1, 2 ou 3, dans lequel lesdites parties émettrices de lumière (2) de chaque élément émetteur de lumière (1) constituent trois types de parties émettrices de lumière (2) qui sont conçues pour émettre respectivement de la lumière rouge (R), de la lumière verte (G) et de la lumière bleue (B), et dans lequel, dans chaque élément émetteur de lumière (1), lesdites parties émettrices de lumière sont prévues dans le rapport R : G : C = 1 : 2 : 1.

5. Dispositif d'affichage à grand écran comme revendiqué dans l'une quelconque des revendications précédentes, dans lequel ladite carrosserie (6) loge un moyen (33) de distribution de l'énergie pour recevoir l'énergie électrique et distribuer ladite énergie électrique auxdits modules (4).

6. Dispositif d'affichage à grand écran comme revendiqué dans l'une quelconque des revendications précédentes, dans lequel lesdits modules (4) sont disposés pour former une pluralité de groupes de modules (5), groupes dans chacun desquels des sections d'entrée des signaux des modules (4) du groupe sont connectées avec une ligne de signaux commune (14), et

les groupes de modules (5) sont disposés pour former un écran (30) dudit moyen d'affichage.

7. Dispositif d'affichage à grand écran comme revendiqué dans la revendication 6 dans lequel ladite carrosserie (6) loge un moyen (20) d'amenée des signaux qui reçoit un signal, convertit ledit signal en un signal numérique prédéterminé et envoie ledit signal numérique auxdites lignes de signaux communes (14) desdits groupes de modules (5).

8. Appareil d'affichage à grand écran comme revendiqué dans la revendication 7, dans lequel lesdits groupes de modules (5) qui sont identifiés par les adresses respectives sont disposés en monodimensionnel, et dans lequel lesdits groupes de modules (5) sont connectés, par l'intermédiaire des lignes de signaux communes (14), au moyen (20) d'amenée des signaux, lesdits groupes. de modules (5) recevant les données respectives concernant l'affichage transmises par lesdites lignes de signaux (14), en fonction des données, concernant les adresses, transmises par lesdites lignes de signaux (14).

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9. Appareil d'affichage à grand écran comme revendiqué dans la revendication 8, dans lequel chacune desdites lignes de signaux communes (14) conporte une ligne de signaux concernant les données et deux types de lignes de signaux chronométriques, lesdits données concernant l'affichage et lesdites données concernant les adresses étant transmises par ladite ligne de signaux concernant les données en mode multiplexage par répartition dans le temps, un signal chronométrique pour déterminer la distribution chronométrique de la réception desdites données concernant les adresses étant transmis par l'un des deux dits types de lignes de signaux chronométriques et un signal chronométrique pour déterminer la chronométrie de la réception desdites données concernant l'affichage étant transmis par l'autre, et

dispositif dans lequel chacun desdits modules (5) sépare les unes des autres lezdites données concernant l'affichage et lesdites données concernant les adresses, en fonction des deux dits signaux chronométriques.

10. Dispositif d'affichage à grand écran comme revendiqué dans l'une quelconque des revendications précédentes, dans lequel ledit moyen d'affichage comporte une pluralité de modules d'affichage (4) pour afficher une image complète.

11. Module pour un dispositif d'affichage à grand écran comme revendiqué dans l'une quelconque des revendications précédentes, dans lequel (2^a x 2^b) parties émettrices de lumière sont disposées sous forme d'une matrice bidirectionnelle, le module comportant:

une section (18) de commande d'adresse pour fournir un signal de sortie de (a+b+c) bits correspondant au nombre (2^a x 2^b) de parties émettrices de lumière dans lesdits moyens d'affichage et au nombre (2^c) de gradations de l'affichage et pour diviser successivement en fréquence un signal d'horloge par des facteurs allant de 1/2 à $(1/2)^{a+b+c}$

un moyen (17) de commande chronométrique pour fournir le signal d'horloge à la section (18) de commande d'adresse;

une mémoire de trame d'image (15) qui, lorsqu'une adresse y est identifiée par (a + b) bits, reçoit et fournit des données de c bits; et

une section (16) de décision en circuit-hors circuit pour soumettre lesdites données des signaux de c bits fournis par la mémoire de trame d'image (15) à une comparaison avec des signaux de c bits fournis par la section (18) de commande d'adresse et pour appliquer des données de 1 bit, représentant les états "allumé" et "éteint" desdites parties émettrices de lumière auxdites parties émettrices de lumière et pour maintenir lesdites données pendant une période de temps prédéterminée pour piloter ledit moyen d'affichage.