

Description

The invention relates to a circuit arrangement for supplying a drive voltage to an enhancement mode field effect transistor arranged as a current source whose channel is included between a first supply voltage terminal and an output terminal, said circuit arrangement comprising:

a first depletion mode field effect transistor operated in the non-saturated mode whose channel is included between the first supply voltage terminal and a junction point,

a second depletion mode field effect transistor operated in the saturated mode whose channel is included between the said junction point and a second supply voltage terminal, the drive voltage for the current source field effect transistor being supplied from the said junction point to the gate of the current source field effect transistor.

A circuit arrangement of this type is known from United States Patent 4,004,164. In this known circuit arrangement the gate of the first field effect transistor is connected to a reference voltage, for example a voltage at ground level, and the gate of the second field effect transistor is connected to the said junction point. With an appropriate choice of the parameters the field effect transistor arranged as a current source will supply a current which varies inversely with changes in the supply voltage in order to apply a compensated current to an analogous circuit.

It is not an object of the present application to supply a compensated current, but it has for its object to provide a circuit arrangement for supplying a drive voltage to an enhancement mode field effect transistor arranged as a current source, which field effect transistor, with this drive voltage, supplies a current which is independent of temperature variations to a great extent.

To this end a circuit arrangement of the type defined in the opening paragraph is characterized in that the gate of the first field effect transistor is connected to the said junction point, in that the gate of the second field effect transistor is connected to the first supply voltage terminal and in that the channel width/channel length ratios k_1 and k_2 , respectively of the first and second field effect transistors and the threshold voltages V_{TD} thereof are chosen to be such that at the desired current intensity supplied by the current source the temperature-dependent variation of the gate-source voltage of the first transistor, at least within a predetermined temperature range, at least substantially corresponds to the temperature-dependent variation required of the source-gate voltage of the field effect transistor arranged as a current source to ensure that the output current of the latter is maintained substantially constant.

The channel width/channel length ratios k_1 and k_2 , of the first and second transistors respectively, and the threshold voltages V_{TD} thereof, as well as the threshold voltage V_{TE} of the field effect transistor arranged as a current source may be chosen to be such that at a given reference temperature T_0 the following equation is at least substantially satisfied

$$\frac{(k_1 + k_2) - \sqrt{k_1(k_1 + 3k_2)}}{k_2 - k_1} = \frac{V_{TE}(T_0) + \frac{4}{3} \left| \frac{dV_{TE}}{dT} \right| \cdot T_0}{\left| V_{TD}(T_0) \right| - \frac{4}{3} \left| \frac{dV_{TD}}{dT} \right| \cdot T_0}$$

Thus it can be achieved that the derivative with respect to temperature of the current supplied by the current source transistor is equal to zero at the reference temperature T_0 while this at least approximately also applies within a very broad temperature range around T_0 .

Furthermore, the channel width/channel length ratio of the second field effect transistor relative to the channel width/channel length ratio of the first field effect transistor is preferably chosen to be relatively large. It is then achieved that the influence of the spread in width/length ratios of the channels of the transistors caused by the manufacturing process is greatly reduced.

Furthermore it is an object of the invention to provide a circuit arrangement for supplying a drive voltage to an enhancement mode field effect transistor arranged as a current source, which field effect transistor supplies a current which is also independent of supply voltage variations to a great extent.

In a circuit arrangement of the type defined in the opening paragraph this object can be satisfied if the channel of a fourth depletion mode field effect transistor operated in the saturated mode is included between the second supply voltage terminal and the channel of the second transistor, the gate of said fourth field effect transistor being connected to the said junction point.

It is to be noted that United States Patent 4,031,456 describes a current source circuit provided with an enhancement mode field effect transistor operated in the non-saturated mode whose channel is included between a first supply voltage terminal and a junction point, a second depletion mode field effect transistor whose channel is included between the said junction point and the output terminal of the circuit arrangement, while the gate of this second field effect transistor is connected to the first supply voltage terminal, and a depletion mode field effect transistor arranged as a current source whose channel is

included between the first supply voltage terminal and an output terminal.

However, in this known circuit arrangement the first field effect transistor is of the enhancement type and not of the depletion type as in the present Application, and furthermore the current source transistor is of the depletion type and not of the enhancement type as in the present Application. Moreover, the channel of the second field effect transistor is not connected to the first supply voltage terminal but is connected to the output terminal of the circuit arrangement, which implies that there is no question of a separate drive circuit for applying a drive voltage to one or more field effect transistors arranged as a current source, but of a circuit arrangement functioning as a current source in its totality. This publication only states that the second field effect transistor is to operate in region with a positive temperature characteristic or that the first field effect transistor is to operate in a region with a negative temperature characteristic.

The invention will be described in greater detail with reference to the accompanying Figures.

Fig. 1a shows an enhancement mode field effect transistor arranged as a current source and Fig. 1b the associated $I-V_{gs}$ characteristic curve.

Fig. 2 shows the relationship between the output current I and the drive voltage V_{gs} of Fig. 1 for two different temperatures.

Fig. 3 shows first example of a drive circuit according to the invention.

Fig. 4 illustrates the dependence of the drive voltage V_{gs} on the temperature required if the output current is not to vary with temperature.

Fig. 5 shows a graph indicating how a beneficial choice can be made for the width/length ratios of the channels of the various transistors of a drive circuit according to the invention.

Fig. 6 shows a complete circuit arrangement for supplying a constant temperature-independent reference current I_{ref} .

Fig. 7 shows a second example of a drive circuit according to the invention.

Fig. 8 shows a more elaborate known current source circuit with which a current can be supplied which is independent of supply voltage variations to a great extent.

Fig. 9 shows a circuit arrangement for supplying a plurality of constant temperature-independent currents, comprising a plurality of current source circuits which are parallel-driven by a drive circuit according to the invention.

Fig. 1 diagrammatically shows an enhancement mode field effect transistor functioning as a current source, together with its $I-V_{gs}$ characteristic curve. The index E will be used hereinafter for a number of parameters relating to this type of transistor). In this characteristic curve the variation of the current I is plotted as a function of the gate voltage V_{gs} for two temperatures T_0 and T_1 , where $T_1 > T_0$. The transistor operates in the region above the point of intersection S, thus for example is set at the point P. When the temperature is raised from T_0 to T_1 , neither the voltage V_{gs} nor the current I will generally remain constant, but the transistor will be set at a point on the curve for T_1 somewhere between the points Q and R, for example at the point U.

However, a current source which is to supply a constant current is required to maintain the supplied current I also when the temperature varies. For a current I through an enhancement mode transistor operating in the saturated mode there applies that

$$I = k(V_{gs} - V_{TE})^2 \quad (1)$$

with

$$k = \mu_E \frac{C_{ox}}{2} \cdot \frac{W}{L} \quad (2)$$

where

μ_E = the mobility of the charge carriers in the channel;

C_{ox} = the capacitance of the oxide under the gate per unit of surface area;

W = the effective channel width;

L = the effective channel length;

V_{TE} = the threshold voltage of the transistor used.

When it is assumed that:

μ_0 = the mobility of the charge carriers at the temperature $T = T_0$,

the above quoted formula (1) may be written as

$$V_{gs} - V_{TE} = \sqrt{\frac{2I \cdot L}{\mu_0 C_{ox} W}} \cdot \sqrt{\frac{\mu_0}{\mu_E}} \quad (3)$$

If the voltage V_{gs} can be changed as a function of the temperature in such a manner that the current I remains constant, formula (3) can be written as:

$$V_{GS} - V_{TE} = C^x \sqrt{\frac{\mu_0}{\mu_E}} \quad (4)$$

where C^x is a constant.

A generally used expression for the mobility of the charge carriers in the channel is:

$$\mu_E(T) = \mu_0 \left(\frac{T_0}{T} \right)^{3/2} \quad (5)$$

which after substitution in (4) leads to:

$$V_{GS} = V_{TE} + C^x \left(\frac{T}{T_0} \right)^{3/4} \quad (6)$$

In Fig. 2 two values of C^x are chosen for the temperature $T_0 = 323 \text{ K}$ (50°C), namely 1.0 and 1.5 volts. Subsequently the gate voltage V_{GS} is plotted with reference to formula (6) as a function of the temperature for the temperature range $233 \text{ K} < T < 413 \text{ K}$ ($-40^\circ\text{C} < T < 140^\circ\text{C}$). Fig. 2 shows that V_{GS} varies substantially linearly with the temperature over a relatively large temperature range. For the purpose of comparison the straight curve is drawn as a broken line along-side both curves, which line makes it clear that the deviation from the straight curve is only very small. The slope of the two substantially straight lines is given by:

$$\frac{\delta V_{GS}}{\delta T} = \frac{dV_{TE}}{dT} \cdot \frac{3}{4} \cdot \frac{C^x}{T_0^{3/4}} \cdot T^{-1/4} \quad (7)$$

Since V_{TE} decreases linearly when the temperature increases, the derivative with respect to temperature increases, the derivative with respect to temperature of this threshold voltage is a constant. The slope of the curves in Fig. 2 at a temperature $T = T_0$ is thus exclusively determined by the value of C^x .

The invention aims to provide a circuit arrangement whose output voltage satisfies the function given in formula (6) at least with a very good approximation. A first embodiment of this circuit arrangement is shown in Fig. 3. When this circuit arrangement is coupled to the current source transistor of Fig. 1, this transistor will supply a current I which is substantially independent of the temperature.

The circuit arrangement of Fig. 3 is provided with the field effect transistors T_1 and T_2 which are both of the depletion type. (The index D will be used hereinafter for a number of parameters relating to this type of transistor). The channels of the two transistors are series-arranged in the manner shown between the supply voltage terminal $+V_B$ and the ground terminal. The junction point between the two channels is connected to the gate of transistor T_1 and the gate of transistor T_2 is connected to the ground terminal. Transistor T_1 operates in the triode region or non-saturated mode, while transistor T_2 operates in the saturated mode. For the current I through the two transistors there applies at least approximately:

$$I = k_2 (-V_{GS} - V_{TD})^2 = k_1 V_{GS} (V_{GS} - 2 V_{TD}) \quad (8)$$

with

$$k_1 = \mu_D \frac{C_{ox}}{2} \frac{W_1}{L_1} \quad \text{and} \quad k_2 = \mu_D \frac{C_{ox}}{2} \frac{W_2}{L_2}$$

An expression for V_{GS} can be derived from this relation:

$$V_{GS} = \frac{(k_1 + k_2) - \sqrt{k_1(k_1 + 3k_2)}}{k_2 - k_1} \cdot |V_{TD}| = f(k_1, k_2) \cdot |V_{TD}| \quad (9)$$

In formula (9) $f(k_1, k_2)$ is a positive factor which is independent of the temperature T and whose magnitude is determined by the W/L ratios of the two transistors. Fig. 4 diagrammatically shows the

variation of the voltage V_{gs} as a function of the temperature for two values of $f(k_1, k_2)$. The slope of the two substantially linear curves is given by:

$$\frac{\partial V_{gs}}{\partial T} = f(k_1, k_2) \cdot \left| \frac{dV_{TD}}{dT} \right| \quad (10)$$

in which the derivative of the threshold voltage V_{TD} with respect to the temperature is a positive constant, which means that the slope of the curves is determined by the W/L ratios of the two transistors.

It will be evident that by correct choice of the effective channel length L and the effective channel width W of the two transistors T_1 and T_2 the curve for V_{gs} in Fig. 4, at least at a chosen reference temperature T_0 , passes through the same point as the corresponding curve for the current source transistor shown in Fig. 2, whilst the slope of the curve of Fig. 4 can also be chosen to be such that the curves of Figs. 2 and 4 coincide or substantially coincide within a broad temperature range.

Based on the above-quoted formulas it is possible to derive a relation which the W/L ratios must satisfy if the curves of Figs. 2 and 4 are to coincide at least one point.

When formula (9) is substituted in formula (6), we find for C^x :

$$C^x = (V_{gs} - V_{TE})_{T=T_0} = f(k_1, k_2) \cdot |V_{TD}(T_0)| - V_{TE}(T_0) \quad (11)$$

Substituting formula (10) in formula (7) yields at the temperature $T = T_0$:

$$f(k_1, k_2) \cdot \left| \frac{dV_{TD}}{dT} \right| = \frac{dV_{TE}}{dT} + \frac{3}{4} \frac{C^x}{T_0} \quad (12)$$

Combination of these last two formulas (11) and (12) yields the condition which the respective channel lengths and widths of the transistors T_1 and T_2 are to satisfy at a given reference temperature $T = T_0$ if at this temperature the derivative with respect to temperature of the supplied current is to be equal to zero, in other words at least around this temperature the current is to be independent of the temperature. This condition is:

$$f(k_1, k_2) = \frac{V_{TE}(T_0) + \frac{4}{3} \left| \frac{dV_{TE}}{dT} \right| \cdot T_0}{|V_{TD}(T_0)| - \frac{4}{3} \left| \frac{dV_{TD}}{dT} \right| \cdot T_0} \quad (13)$$

Since $f(k_1, k_2)$ as a function of k_1 and k_2 is only dependent on the W/L ratios of the relevant transistors, it is only necessary for achieving the required temperature-dependent drive voltage that the width/length ratios of the channels of each transistor are chosen to be such that the above-mentioned formula is satisfied. With such a choice the derivative with respect to temperature of the current through the current source transistor is zero at $T = T_0$ and at least substantially 0 for a large range around $T = T_0$.

In Fig. 5 $f(k_1, k_2)$ is plotted as a function of $(W/L)_2/(W/L)_1$ (at $T = T_0$). This Figure shows that the variation in $f(k_1, k_2)$ becomes increasingly smaller as the ratio $(W/L)_2/(W/L)_1$ becomes larger. In other words, any spread in the (W/L) ratios will have less and less influence on the variation of the current supplied by the current source transistor as a function of the temperature as the value of $f(k_1, k_2)$ is larger. It is therefore to be preferred to choose the value of $f(k_1, k_2)$ as large as possible within the limitations imposed by possible different design requirements.

The total current source circuit consisting of a combination of the circuits of Figs. 1 and 3 is shown in Fig. 6. The current I_{ref} supplied by this circuit is dependent on the choice of the channel length and channel width of the current source transistor T_3 as is apparent from the above-quoted formulas (1) and (2).

Fig. 2 shows a more extensive drive circuit according to the invention in which a fourth depletion-mode transistor T_4 is incorporated in such a manner that the channel of this transistor is arranged between the supply voltage terminal and the channel of the second transistor, whilst the gate of the fourth transistor is connected to the gate of the first transistor. By addition of this transistor T_4 it is achieved that the drive voltage supplied by the circuit arrangement (and hence the current supplied by the current source transistor) becomes independent of supply voltage variations to a great extent.

The added fourth transistor operates in the saturated mode. The minimum supply voltage required in the circuit of Fig. 7 is given by:

$$V_B > V_{gs} + |V_{TD}| \quad (13)$$

Furthermore the supply voltage is to be chosen sufficiently high (with this limitation that the transistor T_4 is saturated. It is apparent from the foregoing that transistor T_2 must also be saturated. This implies that

$$-V_{gs} + |V_{TD}| < V_{ds2} < |V_{TD}| \quad (14)$$

must apply to transistor T_2 .

The voltage $V_{ds} \geq$ must satisfy the two conditions, on the one hand to keep the transistor T_2 saturated and on the other hand to ensure that transistor T_4 is not pinched off. It follows from a calculation that if all transistors T_1 , T_2 and T_4 have different (W/L) ratios, indicated by k_1 , k_2 and k_4 , respectively, there must apply that

$$f(k_1, k_2) > \frac{2k_1}{k_4 - k_1} \quad (16)$$

however, if the transistors T_2 and T_3 have the same (W/L) ratio we find that

$$k_2 = k_4 > 5k_1 \quad (17)$$

or

$$(W/L)_2 = (W/L)_4 > 5 (W/L)_1 \quad (18)$$

It has been found that the circuit of Fig. 7 supplies a drive voltage V_{gs} which is substantially independent of supply voltage variations. As compared with the circuit of Fig. 3 an improvement by a factor of 10 was achieved in a practical embodiment. A practical value for the derivative of the voltage V_{gs} with respect to the supply voltage is

$$\frac{V_{gs}}{V_B} \cong 1 \text{ mV/V} \quad (19)$$

A further improvement in the independence of the supply voltage variations of the current supplied by the current source transistor may be achieved by connection of a further depletion mode transistor T_5 operating in the saturated mode to the current source transistor.

Fig. 8 shows a current source circuit in which the channel of the transistor T_5 is arranged in series with the channel of the current source transistor T_3 . The gate of transistor T_5 is connected to ground. The electronic circuit to which the current is to be applied and which is generally indicated by Z is present between the supply voltage terminal $+V_B$ and the channel of transistor T_5 .

A current source circuit of this type is known per se from British Patent Application 2,054,996.

Finally Fig. 9 shows a complete circuit arrangement consisting of a drive stage provided with the transistors T_1 , T_2 and T_4 and a number of current source circuits consisting of the transistors T_{31} , $T_{51} \dots T_{3n}$, T_{5n} . The drive stage is identical to the circuit of Fig. 7 and the current source circuits are identical to the circuit of Fig. 8. The currents $I_{ref1} \dots I_{refn}$ which are supplied by the various current source circuits can be set by correct choice of the respective width/length ratios (W/L) of the channels of the respective transistors T_{31} , $\dots$, T_{5n} .

Claims

1. A circuit arrangement for supplying a drive voltage to an enhancement mode field effect transistor arranged as a current source whose channel is included between a first supply voltage terminal and an output terminal, said circuit arrangement comprising:

a first depletion mode field effect transistor operated in the non-saturated mode whose channel is included between the first supply voltage terminal and a junction point,

a second depletion mode field effect transistor operated in the saturated mode whose channel is included between the said junction point and a second supply voltage terminal, the drive voltage for the current source field effect transistor being supplied from the said junction point to the gate of the current source field effect transistor, characterized in that the gate of the first field effect transistor is connected to the said junction point, in that the gate of the second field effect transistor is connected to the first supply voltage terminal, and in that the channel width/channel length ratios k_1 and k_2 of the first and second field effect transistors respectively and the threshold voltages V_{TD} thereof are chosen to be such that at the desired current intensity supplied by the current source the temperature-dependent variation of the gate-source voltage of the first transistor, at least within a predetermined temperature range, at least substantially corresponds to the temperature-dependent variation required of the source-gate voltage of the field effect transistor arranged as a current source to ensure that the output current of the latter is maintained substantially constant.

2. A circuit arrangement as claimed in Claim 1, characterized in that the channel width/channel length

Furthermore the supply voltage is to be chosen sufficiently high (with this limitation that the transistor T_4 is saturated. It is apparent from the foregoing that transistor T_2 must also be saturated. This implies that

$$-V_{gs} + |V_{TD}| < V_{ds2} < |V_{TD}| \quad (14)$$

must apply to transistor T_2 .

The voltage V_{ds2} must satisfy the two conditions, on the one hand to keep the transistor T_2 saturated and on the other hand to ensure that transistor T_4 is not pinched off. It follows from a calculation that if all transistors T_1 , T_2 and T_4 have different (W/L) ratios, indicated by k_1 , k_2 and k_4 , respectively, there must apply that

$$f(k_1, k_2) > \frac{2k_1}{k_4 - k_1} \quad (16)$$

however, if the transistors T_2 and T_3 have the same (W/L) ratio we find that

$$k_2 = k_4 > 5k_1 \quad (17)$$

or

$$(W/L)_2 = (W/L)_4 > 5 (W/L)_1 \quad (18)$$

It has been found that the circuit of Fig. 7 supplies a drive voltage V_{gs} which is substantially independent of supply voltage variations. As compared with the circuit of Fig. 3 an improvement by a factor of 10 was achieved in a practical embodiment. A practical value for the derivative of the voltage V_{gs} with respect to the supply voltage is

$$\frac{V_{gs}}{V_B} \approx 1 \text{ mV/V} \quad (19)$$

A further improvement in the independence of the supply voltage variations of the current supplied by the current source transistor may be achieved by connection of a further depletion mode transistor T_5 operating in the saturated mode to the current source transistor.

Fig. 8 shows a current source circuit in which the channel of the transistor T_5 is arranged in series with the channel of the current source transistor T_3 . The gate of transistor T_5 is connected to ground. The electronic circuit to which the current is to be applied and which is generally indicated by Z is present between the supply voltage terminal $+V_B$ and the channel of transistor T_5 .

A current source circuit of this type is known per se from British Patent Application 2,054,996.

Finally Fig. 9 shows a complete circuit arrangement consisting of a drive stage provided with the transistors T_1 , T_2 and T_4 and a number of current source circuits consisting of the transistors T_{31} , T_{51} . . . T_{3n} , T_{5n} . The drive stage is identical to the circuit of Fig. 7 and the current source circuits are identical to the circuit of Fig. 8. The currents I_{ref1} . . . I_{refn} which are supplied by the various current source circuits can be set by correct choice of the respective width/length ratios (W/L) of the channels of the respective transistors T_{31} . . . T_{3n} .

Claims

1. A circuit arrangement for supplying a drive voltage to an enhancement mode field effect transistor arranged as a current source whose channel is included between a first supply voltage terminal and an output terminal, said circuit arrangement comprising:

a first depletion mode field effect transistor operated in the non-saturated mode whose channel is included between the first supply voltage terminal and a junction point,

a second depletion mode field effect transistor operated in the saturated mode whose channel is included between the said junction point and a second supply voltage terminal, the drive voltage for the current source field effect transistor being supplied from the said junction point to the gate of the current source field effect transistor, characterized in that the gate of the first field effect transistor is connected to the said junction point, in that the gate of the second field effect transistor is connected to the first supply voltage terminal, and in that the channel width/channel length ratios k_1 and k_2 of the first and second field effect transistors respectively and the threshold voltages V_{TD} thereof are chosen to be such that at the desired current intensity supplied by the current source the temperature-dependent variation of the gate-source voltage of the first transistor, at least within a predetermined temperature range, at least substantially corresponds to the temperature-dependent variation required of the source-gate voltage of the field effect transistor arranged as a current source to ensure that the output current of the latter is maintained substantially constant.

2. A circuit arrangement as claimed in Claim 1, characterized in that the channel width/channel length



ratios k_1 and k_2 of the first and second transistors respectively and the threshold voltages V_{TD} thereof as well as the threshold voltage V_{TE} of the field effect transistor arranged as a current source are chosen to be such that at a given reference temperature T_0 the following equation is at least substantially satisfied.

$$\frac{(k_1+k_2) - \sqrt{k_1(k_1+3k_2)}}{k_2 - k_1} = \frac{V_{TE}(T_0) + \frac{4}{3} \left| \frac{dV_{TE}}{dT} \right| \cdot T_0}{\left| V_{TD}(T_0) \right| - \frac{4}{3} \left| \frac{dV_{TD}}{dT} \right| \cdot T_0}$$

3. A circuit arrangement as claimed in Claim 1 or 2, characterized in that the channel width/channel length ratio of the second field effect transistor relative to the channel width/channel length ratio of the first field effect transistor is chosen to be relatively large.

4. A circuit arrangement as claimed in any one of the preceding claims, characterized in that the channel of a fourth depletion mode field effect transistor operated in the saturated mode is included between the second supply voltage terminal and the channel of the second transistor, the gate of said fourth field effect transistor being connected to the said junction point.

5. A circuit for supplying a constant current to a load, comprising an enhancement mode field effect transistor arranged as a current source whose channel is included between a first supply voltage terminal and an output terminal, and a circuit arrangement for supplying a drive voltage to said field effect transistor arranged as a current source, said circuit arrangement comprising:

a first depletion mode field effect transistor operated in the non-saturated mode whose channel is included between the first supply voltage terminal and a junction point,

a second depletion mode field effect transistor operated in the saturated mode whose channel is included between the said junction point and a second supply voltage terminal, the drive voltage for the current source field effect transistor being supplied from the said junction point to the gate of the current source field effect transistor, characterized in that the gate of the first field effect transistor is connected to the said junction point, in that the gate of the second field effect transistor is connected to the first supply voltage terminal, and in that the channel width/channel length ratios k_1 and k_2 and of the first and second field effect transistors respectively and the threshold voltages V_{TD} thereof are chosen to be such that at the desired current intensity supplied by the current source the temperature-dependent variation of the gate-source voltage of the first transistor, at least within a predetermined temperature range, at least substantially corresponds to the temperature-dependent variation required of the source-gate voltage of the field effect transistor arranged as a current source to ensure that the output current of the latter is maintained substantially constant.

6. A circuit arrangement as claimed in Claim 5, characterized in that the channel width/channel length ratios k_1 and k_2 of the first and second transistors, respectively, and the threshold voltages V_{TD} thereof, as well as the threshold voltage V_{TE} of the field effect transistor arranged as a current source are chosen to be such that at a given reference temperature T_0 the following equation is at least substantially satisfied

$$\frac{(k_1+k_2) - \sqrt{k_1(k_1+3k_2)}}{k_2 - k_1} = \frac{V_{TE}(T_0) + \frac{4}{3} \left| \frac{dV_{TE}}{dT} \right| \cdot T_0}{\left| V_{TD}(T_0) \right| - \frac{4}{3} \left| \frac{dV_{TD}}{dT} \right| \cdot T_0}$$

7. A circuit arrangement as claimed in Claim 5 or 6, characterized in that the channel width/channel length ratio of the second field effect transistor to the channel width/channel length ratio of the first field effect transistor is chosen to be relatively large.

8. A circuit arrangement as claimed in Claim 5, 6 or 7, characterized in that the channel of a fourth depletion mode field effect transistor operated in the saturated mode is included between the second supply voltage terminal and the channel of the second transistor, the gate of said fourth field effect transistor being connected to the said junction point.

9. An arrangement for supplying a plurality of constant currents to a corresponding number of loads, comprising a corresponding number of enhancement mode field effect transistors arranged as current sources whose channels are each connected between the first supply voltage terminal and one of a corresponding number of output terminals, said arrangement comprising a single circuit as claimed in any of Claims 1 to 4 for supplying a drive voltage to each field effect transistor arranged as a current source.



Patentansprüche

1. Anordnungskreis zur Lieferung einer Steuerspannung an einen Anreicherungs-Feldeffekttransistor, der als Stromquelle geschaltet ist und dessen Kanal sich zwischen einer ersten Speisespannungsklemme und einer Ausgangsklemme befindet, wobei diese Speiseschaltung folgende Elemente umfaßt:
- einen ersten Verarmungs-Feldeffekttransistor, der ungesättigt betrieben wird und dessen Kanal sich zwischen der ersten Speisespannungsklemme und einem Verbindungspunkt befindet,
 - einen zweiten Verarmungs-Feldeffekttransistor, der gesättigt betrieben wird und dessen Kanal sich zwischen dem Verbindungspunkt und einer zweiten Speisespannungsklemme befindet, wobei die Steuerspannung für den Stromquellen-Feldeffekttransistor aus dem Verbindungspunkt dem Gate des Stromquellen-Feldeffekttransistors zugeleitet wird, dadurch gekennzeichnet, daß das Gate des ersten Feldeffekttransistors mit dem Verbindungspunkt verbunden ist, daß das Gate des zweiten Feldeffekttransistors an die erste Speisespannungsklemme angeschlossen ist, und daß die Verhältnisse Kanalbreite/Kanallänge k_1 und k_2 der ersten bzw. zweiten Feldeffekttransistoren und ihre Schwellenwertspannungen V_{TD} derart gewählt werden, daß bei der erwünschten und von der Stromquelle gelieferten Stromstärke die temperaturabhängige Schwankung in der Gate-Quellenspannung des ersten Transistors wenigstens in einem vorgegebenen Temperaturbereich wenigstens hauptsächlich der erwünschten temperaturabhängigen Schwankung in der Quellen-Gate-Spannung des als Stromquelle geschalteten Feldeffekttransistors entspricht, um den Ausgangsstrom dieser Stromquelle im wesentlichen konstant zu halten.
2. Anordnungskreis nach Anspruch 1, dadurch gekennzeichnet, daß die Verhältnisse Kanalbreite/Kanallänge k_1 und k_2 der ersten bzw. zweiten Feldeffekttransistoren und sowohl ihre Schwellenwertspannungen V_{TD} als auch die Schwellenwertspannung V_{TE} des als Stromquelle geschalteten Feldeffekttransistors derart gewählt werden, daß bei einer gegebenen Bezugstemperatur T_0 nachstehende Gleichung wenigstens hauptsächlich erfüllt wird:

$$\frac{(k_1 + k_2) - \sqrt{k_1(k_1 + 3k_2)}}{k_2 - k_1} = \frac{V_{TE}(T_0) + \frac{4}{3} \left| \frac{dV_{TE}}{dT} \right| \cdot T_0}{\left| V_{TD}(T_0) \right| - \frac{4}{3} \left| \frac{dV_{TD}}{dT} \right| \cdot T_0}$$

3. Anordnungskreis nach Anspruch 2, dadurch gekennzeichnet, daß das Verhältnis Kanalbreite/Kanallänge des zweiten Feldeffekttransistors in bezug auf das Verhältnis Kanalbreite/Kanallänge des ersten Feldeffekttransistors verhältnismäßig groß gewählt wird.
4. Anordnungskreis nach einem der vorangehenden Ansprüche, dadurch gekennzeichnet, daß der Kanal eines vierten Verarmungs-Feldeffekttransistors, der gesättigt betrieben wird, sich zwischen der zweiten Speisespannungsklemme und dem Kanal des zweiten Transistors befindet, wobei das Gate des vierten Feldeffekttransistors mit dem Verbindungspunkt verbunden ist.
5. Schaltung zur Lieferung eines Konstantstroms an eine Belastung, mit einem Anreicherungs-Feldeffekttransistor, der als Stromquelle geschaltet ist und dessen Kanal sich zwischen einer ersten Speisespannungsklemme und einer Ausgangsklemme befindet, und mit einem Anordnungskreis zur Lieferung einer Steuerspannung an den als Stromquelle geschalteten Feldeffekttransistor, wobei dieser Anordnungskreis folgende Elemente umfaßt:
- einen ersten Verarmungs-Feldeffekttransistor, der ungesättigt betrieben wird und dessen Kanal sich zwischen der ersten Speisespannungsklemme und einem Verbindungspunkt befindet,
 - einen zweiten Verarmungs-Feldeffekttransistor, der gesättigt betrieben wird und dessen Kanal sich zwischen dem Verbindungspunkt und einer zweiten Speisespannungsklemme befindet, wobei die Steuerspannung für den Stromquellen-Feldeffekttransistor aus dem Verbindungspunkt dem Gate des Stromquellen-Feldeffekttransistors zugeleitet wird, dadurch gekennzeichnet, daß das Gate des ersten Feldeffekttransistors mit dem Verbindungspunkt verbunden ist, daß das Gate des zweiten Feldeffekttransistors an die erste Speisespannungsklemme angeschlossen ist, und daß die Verhältnisse Kanalbreite/Kanallänge k_1 und k_2 der ersten bzw. zweiten Feldeffekttransistoren und ihre Schwellenwertspannungen V_{TD} derart gewählt werden, daß bei der erwünschten und von der Stromquelle gelieferten Stromstärke die temperaturabhängige Schwankung in der Gate-Quellenspannung des ersten Transistors wenigstens in einem vorgegebenen Temperaturbereich wenigstens hauptsächlich der erwünschten temperaturabhängigen Schwankung in der Quellen-Gate-Spannung des als Stromquelle geschalteten Feldeffekttransistors entspricht, um den Ausgangsstrom dieser Stromquelle im wesentlichen konstant zu halten.
6. Anordnungskreis nach Anspruch 5, dadurch gekennzeichnet, daß die Verhältnisse Kanalbreite/Kanallänge k_1 und k_2 der ersten bzw. zweiten Feldeffekttransistoren und sowohl ihre Schwellenwertspannungen V_{TD} als auch die Schwellenwertspannung V_{TE} des als Stromquelle geschalteten



Feldeffekttransistors derart gewählt werden, daß bei einer gegebenen Bezugstemperatur T_0 nachstehende Gleichung wenigstens hauptsächlich erfüllt wird:

$$\frac{(k_1+k_2) - \sqrt{k_1(k_1+3k_2)}}{k_2 - k_1} = \frac{V_{TE}(T_0) + \frac{4}{3} \left| \frac{dV_{TE}}{dT} \right| \cdot T_0}{\left| V_{TD}(T_0) \right| - \frac{4}{3} \left| \frac{dV_{TD}}{dT} \right| \cdot T_0}$$

7. Anordnungskreis nach Anspruch 5 oder 6, dadurch gekennzeichnet, daß das Verhältnis Kanalbreite/Kanallänge des zweiten Feldeffekttransistors in bezug auf das Verhältnis Kanalbreite/Kanallänge des ersten Feldeffekttransistors verhältnismäßig groß gewählt wird.

8. Anordnungskreis nach Anspruch 5, 6 oder 7, dadurch gekennzeichnet, daß der Kanal eines vierten Verarmungs-Feldeffekttransistors, der gesättigt betrieben wird, sich zwischen der zweiten Speisespannungsklemme und dem Kanal des zweiten Transistors befindet, wobei das Gate des vierten Feldeffekttransistors mit dem Verbindungspunkt verbunden ist.

9. Anordnung zur Lieferung einer Anzahl von Konstantströmen an eine entsprechende Anzahl von Belastungen, mit einer entsprechenden Anzahl von Anreicherungs-Feldeffekttransistoren, die als Stromquelle geschaltet sind und deren Kanäle sich jeweils zwischen einer ersten Speisespannungsklemme und einer entsprechenden Anzahl von Ausgangsklemmen befindet, wobei diese Anordnung eine einzige Speiseschaltung nach einem oder mehreren der Ansprüche 1 bis 4 zur Lieferung einer Steuerspannung an jeden als Stromquelle geschalteten Feldeffekttransistor enthält.

Revendications

1. Dispositif de circuit pour délivrer une tension de commande à un transistor à effet de champ du type à enrichissement monté en source de courant, dont le canal est connecté entre une première borne d'alimentation de tension et une borne de sortie ledit dispositif de circuit comportant:

un premier transistor à effet de champ du type à appauvrissement fonctionnant en mode de non-saturation, dont le canal est connecté entre la première borne de tension d'alimentation et un point de jonction,

un deuxième transistor à effet de champ du type à appauvrissement fonctionnant en mode de saturation dont le canal est connecté entre ledit point de jonction et une deuxième borne de tension d'alimentation, la tension de commande pour le transistor à effet de champ source de courant étant délivrée à partir dudit point de jonction à la porte du transistor à effet de champ source de courant, caractérisé en ce que la porte du premier transistor à effet de champ est connectée audit point de jonction, en ce que la porte du deuxième transistor à effet de champ est connectée à la première borne de tension d'alimentation et en ce que les rapports entre la largeur du canal et la longueur du canal, respectivement k_1 et k_2 , des premier et deuxième transistors et leurs tensions de seuil V_{TD} sont choisis de façon qu'à l'intensité de courant désirée fournie par la source de courant la variation dépendant de la température de la tension porte-source du premier transistor, corresponde, au moins dans une gamme de températures préalablement déterminée, au moins pratiquement à la variation dépendant de la température requise pour la tension source-porte du transistor à effet de champ monté en source de courant afin d'assurer que le courant de sortie de ce dernier soit maintenu pratiquement constant.

2. Dispositif de circuit selon la revendication 1, caractérisé en ce que les rapports largeur de canal/longueur de canal k_1 et k_2 respectivement des premier et deuxième transistors et leurs tensions de seuil V_{TD} , ainsi que la tension de seuil V_{TE} du transistor à effet de champ monté en source de courant peuvent être choisis de façon qu'à une température de référence donnée T_0 l'équation suivante soit au moins pratiquement satisfaite

$$\frac{(k_1+k_2) - \sqrt{k_1(k_1+3k_2)}}{k_2 - k_1} = \frac{V_{TE}(T_0) + \frac{4}{3} \left| \frac{dV_{TE}}{dT} \right| \cdot T_0}{\left| V_{TD}(T_0) \right| - \frac{4}{3} \left| \frac{dV_{TD}}{dT} \right| \cdot T_0}$$

3. Dispositif de circuit selon la revendication 1 ou 2, caractérisé en ce que le rapport largeur de canal/longueur de canal du deuxième transistor à effet de champ par rapport au rapport largeur de canal/longueur de canal du premier transistor à effet de champ est de préférence choisi assez élevé.



4. Dispositif de circuit selon l'une des revendications précédentes, caractérisé en ce que le canal d'un quatrième transistor à effet de champ du type à appauvrissement fonctionnant en mode de saturation est connecté entre la deuxième borne de tension d'alimentation et le canal de deuxième transistor, la porte dudit quatrième transistor à effet de champ étant connectée audit point de jonction.

5. Circuit pour délivrer un courant à une charge, comportant un transistor à effet de champ du type à enrichissement monté en source de courant dont le canal est connecté entre une première borne de tension d'alimentation et une borne de sortie et un dispositif de circuit pour délivrer une tension de commande audit transistor à effet de champ monté en source de courant, ledit dispositif de circuit comportant:

10 un premier transistor à effet de champ du type à appauvrissement fonctionnant en mode de non-saturation, dont le canal est connecté entre la première borne de tension d'alimentation et un point de jonction,

un deuxième transistor à effet de champ du type à appauvrissement fonctionnant en mode de saturation dont le canal est connectée entre ledit point de jonction et une deuxième borne de tension d'alimentation, la tension de commande pour le transistor à effet de champ source de courant étant délivrée pour le transistor à effet de champ source de courant étant délivrée à partir dudit point de jonction à la porte du transistor à effet de champ source de courant, caractérisé en ce que la porte du premier transistor à effet de champ est connectée audit point de jonction, en ce que la porte du deuxième transistor à effet de champ est connectée à la première borne de tension d'alimentation et en ce que les rapports entre la largeur du canal et la longueur du canal, respectivement k_1 et k_2 , des premier et deuxième transistors et leurs tensions de seuil V_{TD} sont choisis de façon qu'à l'intensité de courant désirée fournie par la source de courant la variation dépendant de la température de la tension porte-source du premier transistor, corresponde, au moins dans une gamme de températures préalablement déterminée, au moins pratiquement à la variation dépendant de la température requise pour la tension source-porte du transistor à effet de champ monté en source de courant afin d'assurer que le courant de sortie de ce dernier soit maintenu pratiquement constant.

6. Dispositif de circuit selon la revendication 5, caractérisé en ce que les rapports largeur de canal/longueur de canal k_1 et k_2 respectivement des premier et deuxième transistors et leurs tensions de seuil V_{TD} , ainsi que la tension de seuil V_{TE} du transistor à effet de champ montée en source de courant doivent être choisis de façon qu'à une température de référence donnée T_0 l'équation suivante soit au moins pratiquement satisfaite

$$\frac{(k_1 + k_2) - \sqrt{k_1(k_1 + 3k_2)}}{k_2 - k_1} = \frac{V_{TE}(T_0) + \frac{4}{3} \left| \frac{dV_{TE}}{dT} \right| \cdot T_0}{\left| V_{TD}(T_0) \right| - \frac{4}{3} \left| \frac{dV_{TD}}{dT} \right| \cdot T_0}$$

7. Dispositif de circuit selon la revendication 5 ou 6, caractérisé en ce que le rapport largeur de canal/longueur de canal du deuxième transistor à effet de champ par rapport au rapport largeur de canal/longueur de canal du premier transistor à effet de champ est choisi relativement élevé.

8. Dispositif de circuit selon la revendication 5, 6 ou 7, caractérisé en ce que le canal d'un quatrième transistor à effet de champ du type à appauvrissement fonctionnant en mode de saturation est disposé entre la deuxième borne de tension d'alimentation et le canal du deuxième transistor, la porte dudit quatrième transistor à effet de champ étant connectée audit point de jonction.

9. Dispositif pour délivrer plusieurs courants constants à un nombre correspondant de charges, comportant un nombre correspondant de transistors à effet de champ du type à enrichissement monté en sources de courant dont les canaux sont connectés chacun entre une première borne de tension d'alimentation et l'un d'un nombre correspondant de bornes de sortie, ledit dispositif comportant un circuit simple selon l'une des revendications 1 à 4 pour délivrer une tension de commande à chaque transistor à effet de champ monté en source de courant.

