



- (51) **International Patent Classification:**
H03L 7/07 (2006.01) *H03L 7/16* (2006.01)
- (21) **International Application Number:**
PCT/US2014/061719
- (22) **International Filing Date:**
22 October 2014 (22.10.2014)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
61/894,089 22 October 2013 (22.10.2013) US
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(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

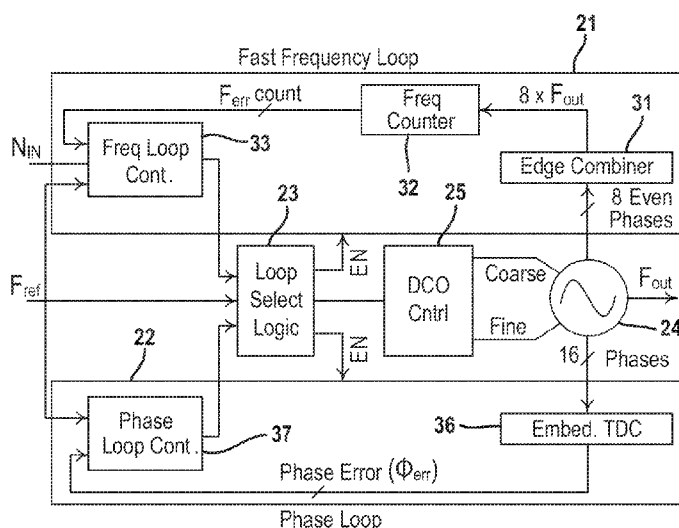
(84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LI, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

[Continued on next page]

(54) **Title:** DUAL-LOOP PROGRAMMABLE AND DIVIDERLESS CLOCK GENERATOR FOR ULTRA LOW POWER APPLICATIONS

**FIG. 2A**

(57) **Abstract:** A programmable clock generator is provided which is particularly suitable for low power applications. The programmable clock generator is comprised of: an oscillator circuit that generates an output signal whose frequency is set by a control signal, two feedback loops for controlling output frequency and a loop select that selects which feedback loop is operational at a given time. In operation, the frequency loop operates to coarsely adjust the frequency of the output signal; whereas, the phase loop operates to finely adjust the frequency of the output signal. The clock generator is preferably implemented by transistors operating in or near the sub-threshold region.



— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*