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DUAL BUS COMMUNICATION SYSTEMBackground of the Invention

5 This invention relates to a communication system.

In communication systems the station, or port, access circuits typically receive information which must be processed by a system resource. In some situations this data must be transferred to a high speed peripheral, such as a disk, and in some cases the information must be transferred to another port access circuit. For voice data, an efficient transfer medium is a time division bus where time slots are assigned for the duration of a call. For bursty, or high speed, data an efficient transfer medium is a packet-switched bus. Thus, an attempt to interface the access circuits with one or the other of the bus types results in a compromise of efficiency with a resultant reduction in system capability.

20 One solution to this problem would be to use a voice interface circuit between voice stations with a time division bus and to use a data interface circuit between data terminals with a packet-switched bus. Such an arrangement solves the basic problem but introduces other undesirable limitations. For example, the typical arrangement for using line circuits is to have the circuits plug into the back plane wiring of a board carrier. Thus, following the above approval, it would be

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necessary to dedicate specific board locations on the carrier to each type of bus and to only use the proper line card for interfacing each bus. This arrangement requires separate inventories of line cards and specific knowledge of which physical spaces each type of line card is adapted to use.

5 In such an arrangement another concern is the pre-engineering that would be required so that there will be enough available physical locations for each board type. Accordingly, systems which are designed primarily for voice would have more available time
10 division positions than packet-switched positions. In such situations if the system migrates toward data terminals it may become necessary to restructure the physical layout to accommodate the necessary interface circuits. This restructuring is costly and inefficient. Accordingly, a need exists for a bus structure which
15 will easily accommodate the various transmission requirements at all positions.

According to the present invention there is provided a communication system comprising a plurality of communication circuits capable of intercommunicating either by a time-division bus
20 or by a packet-switched bus or by both buses, wherein data communicated on the time-division bus is routed by the time slot relationship of the data on the time-division bus, wherein data communicated on the packet-switched bus is routed in accordance with information contained within the data on the packet-switched bus,
25 and wherein the system further comprises connection means for connecting certain of the circuits directly to the time-division bus, certain of the circuits directly to the packet-switched bus, and certain of the circuits directly and concurrently to both of the buses, and wherein certain of said communication circuits includes
30 shared resource means connectable to both of said buses for receiving first data over one of the buses and for delivering second data to the other bus upon receipt of the said first data.

In the preferred embodiment of the invention there is a communication system where each interface circuit has access to both
35 of a time division bus and to a packet-switched bus simply by

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plugging the circuit on a board into any connector. Using this arrangement bus entry points are available for each bus on all connectors so that simply by plugging the board into the connector both time division and packet switching access is available.

5 In this manner it is possible for an access circuit, for example, to communicate with another access circuit during a time slot for the exchange of voice data and to communicate with a peripheral device (a voice storage disk) over the packet bus either concurrently or between time slots.

10 This structure, in addition to solving the physical layout problem, also allows the system to operate in a manner not previously contemplated. For example, in some situations it is necessary to have a protocol

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interchange between communicating stations. This would be possible by using a shared common protocol conversion circuit and allowing any interface circuit to communicate with the common conversion circuit at any time over the packet-switched bus. Thus, signals incoming from the station would pass through the interface circuit and via the packet-switched bus to the common conversion circuit. The converted signals would then be returned to the interface circuit and would then pass to the other station over the time division bus in the assigned time slot. Such an arrangement would work also for many such features where a common circuit may serve a number of interface circuits concurrently.

Circuit boards which do not require access to a certain bus need not be equipped for such access, thereby reducing the cost of those boards, as opposed, for example, to U.S. Patent 4,251,880 which requires all circuit boards to have concurrent access to both buses.

20. Brief Description of the Drawings

The invention

will be more fully understood from a reading of the following description to one embodiment taken in conjunction with the drawing in which:

FIG. 1 shows an overall system block diagram of a parallel running dual bus structure;

FIG. 2 shows details of the TDM bus interface;

FIG. 3 shows details of the packet bus interface;

FIGS. 4 and 5 show examples of shared resource usage over the two system buses; and

FIG. 6 shows details of a dual interface for both continuous and bursty data.

35 Detailed Description

FIG. 1 illustrates a communication system having both a time division (TDM) bus 101 and a packet bus 102, as well as a clock bus 103. TDM bus 101 contains both

circuit-switched time slots and the control channel (for call set-up, etc.). Some of the circuit packs (e.g., TDM bus interface 20) access only the TDM bus. Others (e.g., packet bus interface 30) use the packet bus for communication and use the TDM bus for control information. Still other circuit packs (e.g., TDM and packet interface 60) use both the TDM and packet buses for communication purposes. The structure of each of these buses could be, for example, a set of coaxial cables, with one cable for each path of the bus. Each cable path would then have a termination on the same pin position of each plug-in connection of all the board carriers. Thus, any board type may be plugged into any board position and may have access to either bus.

15 TDM Bus Interface

FIG. 2 gives more detail for TDM bus interface 20. This interface is similar to the one described in Swiss Patent 636,488. Bus buffer 203 and the bus structures are described in U.S. patent application Serial No. 448,835. Network Processing Element 202 provides the time slot interchange functions, as well as gain control and conferencing. They are described in Swiss Patent Nos. 636,488 and 636,487. Port-specific circuit 201 contains the standard circuitry necessary to support various types of telephones or communication devices.

Packet Bus Interface

FIG. 3 shows a more detailed view of packet bus interface 30. This circuit accesses TDM bus 101 only for control information with all data communication being accomplished via packet bus 102. Control interface 310 and microprocessor 309 process the control information exactly the same as on TDM bus interface 20.

The packet bus consists of a parallel data path, a contention bus, and control leads. Any of the standard contention protocols, such as A.S. Tanenbaum, Computer Networks, Prentice-Hall, 1981, Chapt. 7, and W.R. Franta and I. Chlamtac, Local Networks, Lexington

Books, 1981, Chapt. 3, can be used on this bus. The particular implementation could be a variation of a packet-switch bus known as Datakit, as discussed in A.G. Fraser, "Datakit - A Modular Network for Synchronous and Asynchronous Traffic", Proc. ICC, 1979, June 1979, Boston, Mass., pp. 20.1.1-20.1.3. In the transmit direction, the circuit operates as follows. Translation RAM 302 takes data packets from application dependent interface 301 and inserts the proper destination address. CRC generator 303 appends an error-checking checksum to the end of the packet, which is then stored in FIFO 304. When contention control circuit 305 indicates that it has gained control of the data bus, FIFO 304 proceeds to transmit the packet. In one implementation two 9-bit envelopes are transmitted in parallel until the packet is completely transmitted.

In the receive direction, address recognition circuit 306 monitors all packets on the data bus. When circuit 306 detects its own address, a signal is provided to signals FIFO 307 to store the incoming packet, which is then delivered to application interface 301.

In this example, application interface 301 would be a DMA interface to processor 70. In other cases, application interface 301 may interface to a fiber-optic data link, a terminal multiplexor, or to any number of other devices.

As shown in FIG. 1, TDM and packet interface 60 allows, for example, telephone S1 to use circuit-switched TDM bus 101 for continuously generated voice samples while terminal T1 uses packet bus 102 for bursty data transmissions.

FIG. 6 shows a more detailed view of combined TDM and packet interface 60.

The circuit is similar to a combination of TDM bus interface 20 and packet bus interface 30, except that only one set of bus buffers 611, and only one control complex, consisting of microprocessor 609 and control interface 610, are required for connections on both the

TDM and packet buses.

The TDM portion of the interface is similar to the TDM bus interface 20. It contains NPE 608 to control the actual circuit switching. Telephone interface 5 607 is a particular implementation of the port-specific circuitry 201.

The packet interface portion of the circuit is almost identical to packet bus interface 30, except that application interface 301 has been replaced by data 10 terminal interface 601. Data terminal interface 601 does the packet assembly/disassembly (PAD) functions required for accessing a packet-switched system.

Conversion Resources

Numerous examples of conversion resources can 15 be envisioned. Two examples are shown in FIGS. 4 and 5 to illustrate the advantages of simultaneous access to both the TDM and packet buses.

In FIG. 4 conversion resource 40 consists of voice storage processor (VSP) 401. Telephone S2, in 20 conjunction with TDM bus interface 20, generates a continuous 64 Kb/s PCM bit stream which is transmitted in a particular assigned circuit-switched time slot on TDM bus 101. VSP 401 receives this PCM bit stream from bus 101 and encodes it using a more efficient algorithm, 25 such as Linear Prediction Coding or Sub-band Coding (as discussed in L.R. Rabiner and R.W. Schafer, Digital Processor of Speech Signals, Prentice-Hall, 1978) to reduce the bit rate. This encoded speech can be temporarily stored or assembled and then packets of 30 compressed speech can be sent over packet bus 102 to disk control 402 for storage in disk 403.

To play back a recorded message, VSI 401 sends a message over packet bus 102 to disk control 402 to fetch encoded speech packets over the packet bus 35 from disk 403. VSI 401 converts the encoded speech packets back to PCM and places them on TDM bus 101 in a time slot assigned to TDM bus interface 20 which then 38 receives the PCM signal and presents it to telephone S2.

It might appear that disk control 402 could communicate directly with TDM bus interface 20 directly over the TDM bus. However, this is not practical since it is desired, i.e., for economical storage purposes, etc., to connect the PCM signals to a more compact form. Using the system shown, a common conversion resource can be shared among many stations. Also, it might appear that the transfer of information between conversion resource 40 and disk control 402 could occur over the TDM bus. There are several reasons why this, while possible, is not practical. One such reason is because the encoded speech packets, due to the elimination of silent intervals, are not generated at a constant rate. Thus, it would be wasteful of bandwidth to circuit switch these packets over the TDM bus. Another reason is that the transfer between resource 40 and disk control 402 can be delayed for variable time intervals again using up needed bandwidth if a time slot had to remain dedicated to such bursty data transfer.

Also, other devices, such as application processor 70 (FIG. 1), can access disk 402 via the packet bus for high-speed file transfers while the voice storage operation is proceeding.

A second example of a conversion resource is the terminal concentrator 501, illustrated in FIG. 5. Terminal concentrator 501 receives circuit-switch data over the TDM bus from a number of terminals (e.g., terminal T2, terminal S1). Terminal concentrator 501 performs PAD functions on the circuit-switched data and sends the data packets over the packet bus to packet bus interface 30 which transmits the information to application processor 70. Terminal concentrator 501 is thus providing a multiplexed front-end function for application processor 70. This provides for greater throughput from application processor 70 as well as eliminating the need for a data module, such as data module 51, at the application processor end of each connection if communication were to be over the TDM bus.

Also, if communication to and from processor 70 were to be over the TDM bus, then one or more time slots would have to be permanently assigned to the processor.

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The foregoing discussion concerning the use of time division buses for certain types of information and packet-switched buses for other types of information is for illustration only. The particular traffic characteristics at any point in time will dictate which bus is the best one for a particular data transfer. The system described where both buses are connected to all board positions and available simply by plugging the board into the carrier allows the system architect great flexibility in design of the system, both in terms of initial contemplated usage and in terms of future evolutionary changes where different traffic characteristics can be expected.

In addition, the system processor could decide, on a transaction-by-transaction basis, which bus is at that time most appropriate, and tailor the system, on a dynamic basis, for optimum utilization of resources. This can only be achieved if all the boards have continuous access to both buses.

It should be understood that for the purpose of discussion herein, a packet-switched bus is a bus whose bandwidth is allocated on a demand basis, as opposed to a circuit-switched bus, whose bandwidth is allocated for the duration of the connection.

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CLAIMS

1. A communication system comprising a plurality of communication circuits capable of intercommunicating either by a time-division bus or by a packet-switched bus or by both buses, wherein data communicated on the time-division bus is routed by the time slot relationship of the data on the time-division bus, wherein data communicated on the packet-switched bus is routed in accordance with information contained within the data on the packet-switched bus, and wherein the system further comprises connection means for connecting certain of the circuits directly to the time-division bus, certain of the circuits directly to the packet-switched bus, and certain of the circuits directly and concurrently to both of the buses, and wherein certain of said communication circuits includes shared resource means connectable to both of said buses for receiving first data over one of the buses and for delivering second data to the other bus upon receipt of the said first data.

2. A system according to claim 1, wherein the said resource circuits are interconnectable to transmit the said second data concurrent with the transfer of the said first data.

3. A system according to claim 2, wherein certain of said communication circuits are interface circuits for connecting a telephone station to said time-division bus and wherein each shared resource circuit is available for data exchange with any interface circuit.

4. A system according to claim 3, wherein the time slots of the time division bus are assignable for the transfer of information between any of the interface circuits and other interface circuits, and for the transfer of information between any of the interface circuits and the resource circuits.

5. A system according to claim 1, 2, 3 or 4, wherein the communication circuits are contained on circuit boards contained within one or more circuit board housings, each housing having multiple positions therein for the placement of the boards, wherein each board may be placed in any of the positions while still having direct connection to either or both of the buses, and wherein each



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bus includes a multipath cable having a termination for each path at each position of the housing.

6. A system according to claim 3, wherein the interface circuits are contained within a circuit board housing, the latter
5 having multiple prewired positions therein for the semipermanent placement of the interface circuits, and wherein any of the interface circuits may be placed in any of the positions whilst still having access to either or both of the buses without changing the prewiring between the said positions.

10 7. A system according to claim 6, wherein the interface circuits are contained on certain circuit boards and are insertable into the housing at any of the positions thereof, wherein the shared resource circuits are contained on other circuit boards insertable into the housing at any of the positions thereof, wherein the time
15 division or first bus interconnects like paths of each of said positions, the time slots assignable for the transfer of information between any of said housing positions having interface circuits inserted thereat and other housing positions having interface circuits inserted thereat and for the transfer of information
20 between any of said housing positions having interface circuits inserted thereat and housing positions having resource circuits inserted thereat, wherein the packet switched or second bus interconnects like paths of each of said positions, the packet-switched bus serving to transfer information between the
25 interface circuit at selected housing positions while information is concurrently being transferred to or from said selected housing positions over the other bus, and wherein said information transferred over said first bus between a first resource circuit and an interface circuit includes speech signals, and wherein said first
30 resource circuit includes means for modifying speech signals transferred thereto over said first bus and for placing said modified speech signals on said second bus.



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8. A system according to claim 7, wherein at least one of said resource circuits includes means for packaging information transferred from an interface circuit over said first bus for presentation over said second bus to a processor in packet form.

5 9. A communication system substantially as hereinbefore described with reference to the accompanying drawings.

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