WHAT IS CLAIMED IS:

1. A memory system comprising:

a memory module comprising a plurality of memory devices;

a memory controller configured to control a memory operation of the plurality of memory devices; and

a buffer device connected between the memory devices and the memory controller, the buffer device comprises a training block configured to perform training operations for the plurality of memory devices;

wherein the memory controller is configured to control the training block to perform the training operations,

wherein the buffer device and the memory controller are configured to perform the training operations between the buffer device and the memory device in parallel and/or simultaneously with training operations between the buffer device and the memory controller.

2. The memory system of claim 1, wherein the training block includes a signal delay circuit, and the memory controller is configured to compare a pattern data corresponding to training data with a sampling data generated by sampling the training data from a memory device selected as an object for the training operations from among the plurality of memory devices, generates a delay control signal used to control a degree of delay of the signal delay circuit based on a result of the comparison of the pattern data with the sampling data, and transmits the delay control signal to the buffer device.

3. The memory system of claim 2, wherein the sampling data is received from the buffer device, and the training block samples the training data using a data strobe signal for the training operations to generate the sampling data.

4. The memory system of claim 2 or claim 3, wherein, based on the delay control signal, the signal delay circuit delays signals used to perform the training operations on the selected memory device.

5. The memory system of any one of claims 1 to 4, wherein, when performing a memory operation for the plurality of memory devices, the memory controller generates, based

on a result of performing the training operations, a first timing compensation information for reference by the buffer device during a timing compensation operation for signals transmitted/received by the memory devices, the first timing compensation information being transmitted to the buffer device.

6. The memory system of claim 5, wherein the signals transmitted/received by the plurality of memory devices include a first data strobe signal transmitted by the buffer device to the plurality of memory devices and a second data strobe signal received by the buffer device from the plurality of memory devices.

7. The memory system of claim 5 or claim 6, wherein the first timing compensation information includes timing compensation information corresponding to each of the plurality of memory devices.

8. The memory system of any one of claims 5 to 7, wherein the buffer device is connected to the plurality of memory devices via at least two channels, and the first timing compensation information includes timing compensation information corresponding to each of the channels.

9. The memory system of any one of claims 5 to 8, wherein the buffer device compensates for a timing of signals received from the memory controller and signals received from the memory devices, based on the first timing compensation information, and transmits the signals received from the memory controller to the memory devices and the signals received from the memory devices to the memory controller.

10. The memory system of any one of claims 1 to 9, wherein, when performing the training operations for the buffer device and performing the memory operation for the memory devices, the memory controller generates, based on a result of performing the training operations for the buffer device, a second timing compensation information for reference by the memory controller during a timing compensation operation for signals transmitted/received by the buffer device.

11. The memory system of claim 10, wherein, based on the second timing compensation information, the memory controller compensates for a timing of signals to be transmitted to the buffer device and signals received from the buffer device.

12. A memory system comprising:

a memory controller configured to control a memory operation for a plurality of memory devices; and

a memory module including the plurality of memory devices and a buffer device connected between the plurality of memory devices and the memory controller,

wherein the buffer device includes a training block configured to perform training operations for the plurality of memory devices,

wherein the memory controller is configured to control the training block to perform the training operations,

wherein the training block performs the training operations using a first training data and a first data strobe signal each received from a target memory device for the training operations from among the plurality of memory devices, and generates a first timing compensation information for reference by the buffer device during a timing compensation operation for signals relating to a memory operation transmitted/received by the plurality of memory devices, and

wherein the buffer device and the memory controller are configured to perform the training operations between the buffer device and the memory device in parallel and/or simultaneously with training operations between the buffer device and the memory controller.

13. The memory system of claim 12, wherein, when performing read training operations for the target memory device, the training block comprises:

a signal delay circuit configured to delay the first data strobe signal;

a sampling circuit configured to sample the first training data using the delayed first data strobe signal and to generate a first sampling data;

a comparison circuit configured to compare a first pattern data corresponding to the first training data with the first sampling data and to generate a first comparison result; and

a delay adjusting circuit configured to generate, based on the first comparison result, a first delay control signal used to control a degree of delay of the first data strobe signal and to provide the first delay control signal to the signal delay circuit.

14. The memory system of claim 12, wherein, when performing write training operations for the target memory device, the training block comprises:

a sampling circuit configured to sample the first training data corresponding to a second pattern data using the first data strobe signal and to generate a second sampling data;

a comparison circuit configured to compare the second sampling data with the second pattern data and to generate a second comparison result;

a delay adjusting circuit configured to generate, based on the second comparison result, a second delay control signal used to control a degree of delay of the first data strobe signal; and

a signal delay circuit configured to delay the first data strobe signal based on the second delay control signal and to transmit the delayed first data strobe signal to the target memory device of the plurality of memory devices.

15. The memory system of any one of claims 12 to 14, wherein the memory controller is configured to generate, based on a result of performing the training operations for the buffer device, a second timing compensation information for reference during the timing compensation operation for signals relating to a memory operation transmitted/received by the buffer device.

16. The memory system of any one of claims 12 to 15, wherein the training block includes a retiming control unit configured to receive a second pattern data and a second data strobe signal from the memory controller, to re-align the second pattern data based on the second data strobe signal, and to provide the re-aligned second pattern data and the second data strobe signal to the target memory device to perform the training operations for the target memory device.

17. The memory system of any one of claims 12 to 16, wherein, when receiving a fourth data strobe signal from a selected memory device during performing of a memory

operation of a memory device selected from among the plurality of memory devices, the buffer device, based on the first timing compensation information, compensates for timing for the fourth data strobe signal.

18. A memory module comprising:

a plurality of memory devices; and

a plurality of buffer devices configured to route signals to and from the plurality of memory devices,

wherein the plurality of buffer devices comprises:

a first sub-buffer device connected to first memory devices from among the plurality of memory devices;

a second sub-buffer device connected to second memory devices from among the plurality of memory devices; and

a main buffer device connected to the first sub-buffer device and the second sub-buffer device,

wherein the main buffer device is configured to perform first training operations for the first sub-buffer device and second sub-buffer device, and the first sub-buffer device is configured to perform second training operations for the first memory devices, and the second sub-buffer device is configured to perform third training operations for the second memory devices, and wherein the first training operations, second training operations and third training operations comprise generating timing compensation information for one or more of a read training operation, and a write training operation, and

wherein the second training operations and/or the third training operations are performed in parallel and/or simultaneously with the first training operations.

19. The memory module of claim 18, wherein the main buffer device comprises a first register configured to store timing compensation information corresponding to each of the first sub-buffer device and the second sub-buffer device generated as a result of performing the first training operations, and

the first sub-buffer device comprises a second register configured to store timing compensation information corresponding to each of the first memory devices generated as a result of performing the second training operations, and

the second sub-buffer device comprises a third register configured to store timing compensation information corresponding to each of the second memory devices generated as a result of performing the third training operations.