Description

Background of the Invention

1. Field of the Invention

The present invention relates to a technique for forming an electrical contact between a conductor and an underlying region separated by a dielectric layer.

2. Description of the Prior Art

In the production of integrated circuits and other solid state devices, electrical contacts are required between an overlying conductive layer and an underlying region separated therefrom by a layer of a dielectric material. The overlying layer is typically a metal, and the underlying region is typically a doped semiconductor region, or another metal layer. The contact between the overlying and underlying materials is through an opening or window through the intervening dielectric layer. Preferably, to avoid discontinuities in the contact material which extends through the opening, the walls thereof are "smoothed" to have a gently curved rather than an abrupt vertical shape. As described hereinafter, various problems exist with known contacting techniques, and the present invention provides an improvement over such techniques.

JP-A-57 72321 discloses a method of making an electrical contact to a doped region such as a source or drain region of a field effect transistor. The problem which it seeks to solve is that of misalignment between the contact and the region. In the disclosed method the doped region is formed using a primary insulation layer as a mask. A secondary insulation layer is then deposited over the whole wafer surface and anisotropically etched, so that only a sidewall-covering portion remains. The contact is then deposited in the opening formed in the primary insulation layer, which is made slightly smaller, compared with the doped region, by the sidewall-covering layer.

EP-A-0 036 500 discloses a process in which a layer of silicon nitride is laid down over a layer of silicon dioxide. When an opening is made, the sidewalls are not straight, since the oxide etches at a faster rate than the nitride, leaving a recess. Such a recess would give rise to stress and thus cause leakage, so a further oxide layer is deposited to fill the recess prior to depositing the contact material.

Summary of the Invention

With the invention as claimed smoothing of an anisotropically etched aperture is achieved by means of a smoothing layer rather than by "smoothing" in the conventional way.

Brief Description of the Drawings

FIGS. 1-3 illustrate a prior art technique for forming aluminum contacts to semiconductor material.

FIGS. 4-6 illustrate one embodiment of the present invention.

FIGS. 7-9 illustrate an alternate embodiment of the present invention.

Detailed Description

Referring to FIG. 1, in one typical prior art technique, a silicon semiconductor material 10 has formed therein a doped region 11 which may be, for example, the source or drain of a field effect transistor. Formed thereon is a dielectric layer 12, typically of a relatively low softening point (e.g., less than 1100°C in the heating ambient used) glass. This dielectric layer typically has a thickness of less than 1 µm (10000 Ångströms), and presently about 700 nm (7000 Ångströms) in one typical process. There is then formed in layer 12 an opening or window having a width d as indicated. The etching technique, e.g., reactive ion etching, utilized to form the window frequently is anisotropic; that is, it tends to remove material faster in the vertical direction as viewed as compared to the horizontal direction. This process thus forms vertical sidewalls as shown. Since it is desired to deposit a conducting material in this window, the sidewalls typically need to be smoothed. This allows a continuous conducting layer of material to be deposited. In particular, aluminum is notorious for not forming a continuous layer when deposited over vertical sidewalls.

To provide for smoothing the sidewalls, the dielectric material of region 12 is typically a phosphosilicate glass (p-glass), a borosilicate glass, or a glass containing both phosphorous and boron. A heating step, typically 900°C to 1100°C, then causes the sidewalls to flow, forming a smooth transition region 23, as indicated in FIG. 2. Referring to FIG. 3, an aluminum layer 34 is then deposited on the smoothed dielectric material, and makes a continuous contact to the doped region 11 as indicated. Subsequent steps can be used to pattern the conducting region 34 to obtain a desired conductor pattern.

One consequence of this smoothing technique is that it increases the width of the "head" of the contact, i.e., the portion d' of the conductor 34 specifically associated with the contacted region 11. As shown in FIG. 3, this distance d' may be substantially greater than the distance d that initially defined the window. The increase of d' as compared to d limits the density with which adjacent devices can be packed into a given area. Frequently, the distance d is defined by the minimum size that the lithographic technique utilized can achieve. In some cases, it is desirable to form the contact such that this minimum geometry is preserved. One technique that avoids flowing the p-glass layer is by depositing low-resistivity polysilicon into the windows prior to aluminum deposition. The polysilicon then provides electrical conductivity even if the aluminum is discontinuous; see U. S. Patent 4,291,322. However, in some cases even lower electrical contact resistance is desired. In other cases, it is desirable to avoid forming doped (low resistivity) polysilicon, especially as in CMOS circuitry, when

two different dopant types (p-type and n-type) are required. In other instances, it has been found that the aluminum coverage is typically not as good as is desired, even after flowing the p-glass material. That is, small gaps or discontinuities can still exist in aluminum layer 34 deposited on flowed dielectric 12 in FIG. 3. It is desirable to have an alternative technique for making contact to an underlying layer that is separated from a conductive layer by a dielectric region.

Referring to FIG. 4, an embodiment of the invention is now described in which a contact is made to a doped region 41 in a body 40 of semiconductor material. The semiconductor body is typically a silicon substrate, or epitaxial layer formed thereon. Other semiconductor materials, including group III-V materials, are possible. A dielectric material 42 is formed over the region 40. Then an opening is produced in region 42, typically by an anisotropic (i.e., one-directional) etching technique that forms approximately vertical sidewalls as shown. As used herein, the term "vertical" means that the sidewalls are within about ± 20 degrees of being perpendicular to the surface of the substrate; more typically, they are within ± 10 degrees of being perpendicular. The slope may be in either direction, with a negative slope indicating undercut of the dielectric region by the window. The width of the opening (d) is typically about two micrometers for currently made integrated circuits, and is expected to be less than that for future circuits. If desired, the opening as formed can have a width d that is equal to the minimum lithographic dimension.

Next, a material 43, referred to herein as the "smoothing material", is conformally deposited on dielectric region 42. The conformal nature of this deposition implies that the smoothing material has approximately equal thickness over the underlying region 41, the sidewalls of the opening 44, and the surrounding dielectric material 42. The smoothing material 43 preferably does not completely fill in the window, but rather follows the contours of the window. The thickness of the smoothing material as deposited is preferably from 0.4 to 1.5 as much as, and typically somewhat greater than one-half as much as, the thickness of the dielectric material. For example, a thickness of 400 nm for conformal smoothing material 43 is suitable for smoothing a two micrometer opening in a 700 nm thick dielectric region 42.

After thus depositing the smoothing material 43, it is then subjected to an anisotropic etching process, for example, a reactive ion etching process. As used herein with regard to removing the smoothing material, the term "anisotropic" means that the smoothing material is removed at least five times as fast in the vertical direction as in the horizontal direction with respect to the substrate surface. More typically, this ratio exceeds 10 to 1. The result is that the material 43 on the horizontal surfaces as viewed is substantially removed, whereas the smoothing material contacting the vertical sidewall of the window is not substantially removed. Note that the smoothing material is thus removed from the central portion of the underlying region in the opening. In addition, the top portion of the smoothing material contacting the vertical sidewall is etched to some degree. This produces the structure shown in FIG. 5, wherein smoothing region 45 adheres to the sidewall 44 of the opening in dielectric material 42. The smoothing region 45 thus has a nonvertical slope, having an angle typically greater than 20 degrees from the vertical to the substrate. This is as measured by a straight line approximation to the slope, from the upper corner to the lower inside corner of the smoothing region. This smoothing region then serves as a means for obtaining improved conductor coverage. For example, when an aluminum layer 46 is deposited, it typically fills the opening without discontinuities, as indicated in FIG. 6. Note that the size of the contact top is now substantially defined by the distance d, which also defined the window opening. Hence, the contact is said to be "headless".

The smoothing material is typically silicon dioxide. The conformal oxide deposition can be accomplished by decomposing tetraethoxysilane, Si $(OC_2H_5)_4$, at 650° in a low pressure chemical vapor deposition (LPCVD) reaction, according to principles known in the art.

A process suitable for the anisotropic etching of the oxide material is by reactive ion etching with 90% CHF_3 + 10% O_2 at 65 micrometers pressure, at 1500 watts power, or by other methods known in the art. Finally, aluminum can be deposited in the window thus smoothed by sputtering from an aluminum target at 300°C and at 10^{-5} Pa pressure (e.g., in a Varian 3180 sputter system), as is also known in the art. An aluminum thickness in the range of about 0.5 to 1.0 micrometers is typically used in present processes, with a wider range being possible.

While the use of silicon dioxide as a conformally deposited smoothing material has been illustrated above, other materials are possible. For example, silicon nitride can be conformally deposited. Alternately, a conductive material can be deposited as the smoothing material. That is, a metal or metal silicide can be conformally deposited and anisotropically etched to form the smoothing region 45. The use of a conductive material has the advantage of decreasing the contact resistance between the conducting layer 46 and the underlying region 41. This is because the contact area then includes both the areas contacted by smoothing region 45 and conducting layer 46 at the surface of underlying region 41. Note that the conducting layer itself physically contacts the underlying layer only over a diameter d'', as shown in FIG. 5. This diameter has the advantage that it can be less than the minimum lithographic feature size if desired, allowing high-density circuitry to be obtained. However, in some cases the relatively smaller contact area provides a larger than desired contact resistance.

In another embodiment, the conformal

smoothing layer 43 is polysilicon. The polysilicon can be made conductive, either p-type or n-type, corresponding to the conductivity type of underlying region 41, by implanting the appropriate dopant species in the polysilicon material after deposition. This can be followed by a heat treatment to further distribute the dopant evenly throughout the polysilicon, and activate the dopant. Alternatively techniques are known in the art for including a dopant species in polysilicon as it is being deposited. Thus, the smoothing region may be polysilicon doped to an appropriate level for reducing the contact resistance to a doped region 41.

In an alternative embodiment, it is possible to utilize a dielectric smoothing region while also obtaining reduced contact resistance. Referring to FIG. 7, the improved contact resistance is obtained by means of a conductive layer 76 that is deposited or otherwise formed on the underlying region 71 prior to the formation of the smoothing region 74 as discussed previously. The conductive layer 76 then provides a contact area to region 71 that is substantially equal to the area of the opening as formed. The subsequent process steps then can proceed substantially as before. For example, FIG. 8 shows the conductive layer 87, which is typically aluminum, as deposited. In FIG. 9 is shown a view of the contact window, wherein the conducting layer 87 has been patterned so as to remove the aluminum in regions exterior to the window opening. With the aluminum coverage now substantially coextensive with the window opening as formed, it is apparent that the contact is now headless. Note that the aluminum coverage can continue along the direction perpendicular to the plane of FIG. 9 as viewed. The good step coverage provided by the smoothing region 74 allows the aluminum to thus connect several underlying regions 71 together. It is apparent that conducting region 87 can serve as the bit line of a dynamic random access memory, or for numerous other purposes.

The formation of the conductive layer 76 can be facilitated by a technique that provides for selective metal deposition on doped region 71 while avoiding the metal deposition on dielectric 72. Such a technique is known for tungsten; see for example, "Contact Resistance of LPCVD W/AL and PtSi/W/AL Metallization", S. Swirhun et al, IEEE Electron Device Letters, Vol. EDL-5, pp. 209-211 (1984). I recommend depositing the tungsten to a thickness of about 100 nm using a non-oxidizing carrier gas (e.g., nitrogen) to prevent the oxidation of the deposited tungsten. In an alternative method of achieving conductive layer 76, a conductive compound, for example a silicide, can be formed in situ at the surface of doped region 71. The conductive compound thus formed can include silicon derived from doped region 71. It is apparent that still other techniques are possible for selectively forming a conductive layer 76 at the bottom of the window prior to depositing the smoothing material.

One aspect of the present invention is that the dielectric material may be a flowable glass. Then, good step coverage, as over the gate of a field effect transistor, can be obtained by flowing the glass at an elevated temperature before forming the openings for the contacts of the present technique. The contact openings for the gate, source, and drain of a field effect transistor can then be formed and smoothed by the present technique. This can provide for the improved step coverage and small dimensions for contact windows formed by the present technique, while still smoothing and dielectrically isolating other features (e.g., a gate).

An additional layer can be provided between a glass layer and a semiconductor substrate. For example, a 100 nm barrier layer of SiO_2 (not shown) can be grown or deposited on semiconductor layer 40 prior to depositing a glass layer 42. This barrier layer can then serve to prevent the migration of unwanted dopants (e.g., B or P) from the glass into the semiconductor region. Other barrier layer materials (e.g., Si_3N_4) can alternately be used. Hence, the term "overlying" does not imply that the dielectric region necessarily contacts the underlying region, although that may be the case.

While the above description has been in terms of forming a contact to a doped region in silicon, the technique can be applied to doped regions in other semiconductor materials; for example, gallium arsenide and other III-V materials. Furthermore, the technique can be utilized in a "double level metal" technique, wherein it is desired to make contact between an overlying metal layer and an underlying metal layer. The dielectric separating the layers may be a flowable glass, or SiO_2, or other material. The underlying region may be an electro-optic material, for example, lithium niobate, or a conductive pad formed thereon. Then, the conductive overlying layer that contacts the underlying region by the present technique can provide for the application of a control voltage to the electro-optic material.

Claims

1. A method of making a solid state device comprising forming an electrically conductive region (41), forming a first dielectric layer (42) overlying said region, and forming an opening (11) in said dielectric layer, said opening being above a portion of said electrically conductive region (41) and the or each sidewall of said opening being approximately vertical, CHARACTERIZED BY conformally depositing a smoothing material (43) onto said region and said sidewall, said smoothing material having a thickness as deposited of at least 0.4 of the thickness of said first dielectric layer, anisotropically removing said smoothing material from a central portion of said region while maintaining a smoothing portion (45) thereof in contact with said sidewall, and thereafter depositing, by sputtering, conducting material (46) onto said central portion of said region and said smoothing portion.

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2. The method of claim 1 wherein said smoothing material is a dielectric.

3. The method of claim 2 wherein said smoothing material is silicon dioxide.

4. The method of claim 2 wherein said smoothing material is silicon nitride.

5. The method of claim 1 wherein said smoothing material is conductive as deposited.

6. The method of claim 5 wherein said smoothing material is a metal.

7. The method of claim 1 wherein said smoothing material is polysilicon.

8. The method of claim 7 wherein said polysilicon is rendered conductive by the inclusion of a dopant species therein.

9. The method of claim 1 wherein said dielectric material is a glass having a softening point of less than 1100 degrees Celsius.

10. The method of claim 1 wherein said dielectric material is a glass that is flowed at an elevated temperature so as to smooth at least one step of said article prior to said forming said opening.

11. The method of claim 10 wherein said step comprises the gate region of a field effect transistor.

12. The method of claim 1 wherein said smoothing material as deposited has a thickness in the range of from 0.4 to 1.5 of the thickness of said dielectric material.

13. The method of claim 1 further comprising the step of forming a more conductive layer on said underlying region after forming said opening, and prior to depositing said smoothing material.

14. The method of claim 13 wherein said more conductive layer substantially comprises a metal that selectively forms preferentially on said underlying region as compared to said dielectric material.

15. The method of claim 14 wherein said more conductive layer substantially comprises tungsten.

16. The method of claim 1 wherein said underlying region is a doped semiconductor region.

17. The method of claim 1 wherein said conducting material is aluminum.

18. The method of claim 1 wherein said electrically conductive region includes a metal silicide.

19. The method of claim 1 wherein said electrically conductive region is a metal.

Patentansprüche

1. Verfahren zur Herstellung eines Festkörperbauteils, bei dem eine elektrisch leitende Zone (41), eine erste dielektrische Schicht (42) auf der Zone und eine Öffnung (11) in der dielektrischen Schicht gebildet werden, wobei die Öffnung oberhalb eines Teils der elektrisch leitenden Zone (41) angeordnet und die oder jede Seitenwand der Öffnung annähernd vertikal sind,

dadurch gekennzeichnet,

daß sich anpassend ein glättendes Material (43) auf die Zone und die Seitenwand abgelagert wird,

daß das glättende Material im abgelagerten Zustand eine Dicke von wenigstens 0,4 der Dicke der ersten dielektrischen Schicht besitzt,

daß das glättende Material an einem zentralen Teil der Zone anisotrop entfernt wird, wobei ein glättender Teil (45) des Materials in Kontakt mit der Seitenwand erhalten bleibt, und daß danach leitendes Material (46) durch Sputtern auf den zentralen Teil der Zone und den glättenden Teil aufgebracht wird.

2. Verfahren nach Anspruch 1, bei dem das glättende Material ein Dielektrikum sit.

3. Verfahren nach Anspruch 2, bei dem das glättende Material Siliciumdioxid ist.

4. Verfahren nach Anspruch 2, bei dem das glättende Material Siliciumnitrid ist.

5. Verfahren nach Anspruch 1, bei dem das glättende Material im aufgebrachten Zustand leitend ist.

6. Verfahren nach Anspruch 5, bei dem das glättende Material ein Metall ist.

7. Verfahren nach Anspruch 1, bei dem das glättende Material Polysilicium ist.

8. Verfahren nach Anspruch 7, bei dem das Polysilicium durch Einlagerung eines Dotierungsstoffes leitend ist.

9. Verfahren nach Anspruch 1, bei dem das dielektrische Material ein Glas mit einem Erweichungspunkt von weniger als 1100°C ist.

10. Verfahren nach Anspruch 1, bei dem das dielektrische Material ein Glas ist, das bei erhöhter Temperatur zum Fließen gebracht worden ist, um wenigstens eine Stufe des Bauteils vor Bilden der Öffnung zu glätten.

11. Verfahren nach Anspruch 10, bei dem die Stufe die Gate-Zone eines Feldeffekttransistors umfaßt.

12. Verfahren nach Anspruch 1, bei dem das glättende Material im aufgebrachten Zustand eine Dicke im Bereich zwischen 0,4 und 1,5 der Dicke des dielektrischen Materials hat.

13. Verfahren nach Anspruch 1, bei dem ferner der Schritt vorgesehen ist, daß eine besser leitende Schicht auf der unterliegenden Zone nach Bildung der Öffnung und vor Auftragen des glättenden Materials erzeugt wird.

14. Verfahren nach Anspruch 13, bei dem die besser leitende Schicht im wesentlichen ein Metall umfaßt, das selektiv und bevorzugt auf der bezüglich der dielektrischen Schicht unterliegenden Zone gebildet ist.

15. Verfahren nach Anspruch 14, bei dem die besser leitende Schicht im wesentlichen Wolfram enthält.

16. Verfahren nach Anspruch 1, bei dem die unterliegende Zone eine dotierte Halbleiterzone ist.

17. Verfahren nach Anspruch 1, bei dem das leitende Material Aluminium ist.

18. Verfahren nach Anspruch 1, bei dem die elektrisch leitende Zone ein Metallsilicid enthält.

19. Verfahren nach Anspruch 1, bei dem die elektrisch leitende Zone ein Metall ist.

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Revendications

1. Un procédé de fabrication d'un dispositif à l'état solide comprenant la formation d'une région conductrice de l'électricité (41), la formation d'une première couche diélectrique (42) qui recouvre la région précitée, et la formation d'une ouverture (11) dans la couche diélectrique, cette ouverture se trouvant au-dessus d'une partie de la région conductrice de l'électricité (41), et la paroi latérale, où chaque paroi latérale, de l'ouverture étant approximativement verticale, CARACTERISE EN CE QUE on dépose de façon conforme un matériau d'adoucissement (43) sur la région précitée et sur la paroi latérale, ce matériau d'adoucissement ayant une épaisseur, aussitôt après dépôt, d'au moins 0,4 fois l'épaisseur de la première couche diélectrique, on enlève de façon anisotrope le matériau d'adoucissement dans une partie centrale de la région précitée, tout en maintenant une partie d'adoucissement (45) de ce matériau en contact avec la paroi latérale, et on dépose ensuite, par pulvérisation cathodique, un matériau conducteur (46) sur la partie centrale de la région précitée et sur la partie d'adoucissement.

2. Le procédé de la revendication 1, dans lequel le matériau d'adoucissement est un diélectrique.

3. Le procédé de la revendication 2, dans lequel le matériau d'adoucissement est du dioxyde de silicium.

4. Le procédé de la revendication 2, dans lequel le matériau d'adoucissement est du nitrure de silicium.

5. Le procédé de la revendication 1, dans lequel le matériau d'adoucissement est conducteur dans l'état dans lequel il est déposé.

6. Le procédé de la revendication 5, dans lequel le matériau d'adoucissement est un métal.

7. Le procédé de la revendication 1, dans lequel le matériau d'adoucissement est du silicium polycristallin.

8. Le procédé de la revendication 7, dans lequel le silicium polycristallin est rendu conducteur par l'incorporation d'un type de dopant.

9. Le procédé de la revendication 1, dans lequel le matériau diélectrique est un verre ayant un point de ramollissement inférieur à 1100 degrés Celsius.

10. Le procédé de la revendication 1, dans lequel le matériau diélectrique est un verre qu'on fait couler à une température élevée de façon à adoucir au moins une marche du dispositif avant la formation de l'ouverture précitée.

11. Le procédé de la revendication 10, dans lequel la marche constitue la région de grille d'un transistor à effet de champ.

12. Le procédé de la revendication 1, dans lequel le matériau d'adoucissement, aussitôt après avoir été déposé, a une épaisseur dans la plage allant de 0,4 à 1,5 fois l'épaisseur du matériau diélectrique.

13. Le procédé de la revendication 1, comprenant en outre l'opération qui consiste à former une couche plus conductrice sur la région sous-jacente après avoir formé l'ouverture, et avant de déposer le matériau d'adoucissement.

14. Le procédé de la revendication 13, dans lequel la couche plus conductrice consiste pratiquement en un métal qui se forme sélectivement et de façon préférentielle sur la région sous-jacente, en comparaison avec le matériau diélectrique.

15. Le procédé de la revendication 14, dans lequel la couche plus conductrice consiste pratiquement en tungstène.

16. Le procédé de la revendication 1, dans lequel la région sous-jacente est une région de semiconducteur dopé.

17. Le procédé de la revendication 1, dans lequel le matériau conducteur est de l'aluminium.

18. Le procédé de la revendication 1, dans lequel la région conductrice de l'électricité comprend un siliciure de métal.

19. Le procédé de la revendication 1, dans lequel la région conductrice de l'électricité consiste en un métal.