CLAIMS

1. A method of forming a wire in a dielectric layer, comprising:

forming a first opening in a dielectric layer;

depositing a conformal coating of a first layer of a jacket material on said dielectric layer and forming a second opening in said first opening, wherein said jacket material exhibits a first resistivity $\rho 1$;

depositing a core material on said conformal coating, wherein said core material exhibits a second resistivity $\rho 2$ and $\rho 2$ is less than $\rho 1$;

reflowing said core material wherein said core material partially fills said second opening; and

depositing a second layer of said jacket material over said core material and said first layer of said jacket material, filling said second opening and forming a wire, wherein said core material is surrounded by said jacket material.

2. The method of claim 1, wherein said first opening defines a volume and said jacket material is present in the range of 25 % to 75 % of said volume.

3. The method of claim 1, wherein an overburden of said second layer of said jacket material forms over a surface of said dielectric layer and said method further comprises planarizing said second layer of jacket material until said surface of said dielectric layer is exposed.

4. The method of claim 1, wherein said openings are formed in said dielectric layer by photolithography.

5. The method of claim 1, wherein said conformal coating is deposited using chemical vapor deposition.

6. The method of claim 1, wherein said core material is deposited using physical vapor deposition.

7. The method of claim 1, wherein said core material comprises copper and said jacket material excludes copper.

8. The method of claim 1, wherein said dielectric layer exhibits a dielectric constant of lower than 3.9.

9. The method of claim 8, wherein said dielectric layer exhibits a dielectric constant in the range of 1.5 to 3.8.

10. The method of claim 1, wherein said dielectric layer includes one or more materials selected from the group consisting of fluorine-doped silicon dioxide, carbon-doped silicon dioxide, organo silicate glass, silicon oxycarbide, hydrogenated silicon oxycarbide, porous silicon dioxide, and organic polymer dielectrics such as polyimide, polytetrafluoroethylene, polynorbornenes, benzocyclobutene, hydrogen silsequioxane and methylsilsesquioxane.

11. The method of claim 1, wherein said jacket material exhibits a resistivity of 5.0 $\mu\Omega\cdot$cm or greater.

12. The method of claim 1, wherein said core material exhibits a resistivity of 4.0 $\mu\Omega\cdot$cm or less.

13. The method of claim 1, wherein said core material exhibits a first melting temperature and said jacket material exhibits a second melting temperature, wherein said first melting temperature is less than said second melting temperature.

14. A metallization layer, comprising:

an opening defined in a dielectric layer; and

a wire within said opening; wherein said wire includes a core material surrounded by a jacket material, wherein said jacket material exhibits a first resistivity $\rho 1$ and said core material exhibits a second resistivity $\rho 2$ and $\rho 2$ is less than $\rho 1$.

15. The metallization layer of claim 14, wherein said jacket material is present in the range of 25 % to 75 % of the volume of said opening.

16. The metallization layer of claim 14, wherein said dielectric layer exhibits a dielectric constant of lower than 3.9.

17. The metallization layer of claim 14, wherein said dielectric layer exhibits a dielectric constant in the range of 1.5 to 3.8.

18. The metallization layer of claim 14, wherein said dielectric layer includes one or more materials selected from the group consisting of fluorine-doped silicon dioxide, carbon-doped silicon dioxide, organo silicate glass, silicon oxycarbide, hydrogenated silicon oxycarbide, porous silicon dioxide, and organic polymer dielectrics such as polyimide, polytetrafluoroethylene, polynorbornenes, benzocyclobutene, hydrogen silsequioxane and methylsilsesquioxane.

19. The metallization layer of claim 14, wherein said jacket material exhibits a resistivity of 5.0 μΩ·cm or greater.

20. The metallization layer of claim 14, wherein said core material exhibits a resistivity of 4.0 μΩ·cm or less.

21. The metallization layer of claim 14, wherein said core material includes copper and said jacket material excludes copper.

22. The metallization layer of claim 14, wherein said core material exhibits a first melting temperature and said jacket material exhibits a second melting temperature, wherein said first melting temperature is less than said second melting temperature.

23. The metallization layer of claim 14, wherein said core material includes one or more metals selected from the group consisting of copper, aluminum, gold and silver.

24. The metallization layer of claim 14, wherein said jacket material includes one or more metals selected from the group consisting of tungsten, cobalt, ruthenium and molybdenum.

25. An integrated circuit, comprising:

one or more dielectric layers;

a plurality of openings defined in each of said dielectric layers; and

a plurality of wires, wherein each wire is positioned within one of said openings and said

wires include a core material surrounded by a jacket material, wherein said jacket material exhibits a first resistivity ρ1 and said core material exhibits a second resistivity ρ2 and ρ2 is less than ρ1.

CLAIMS

1. A method of forming a wire in a dielectric layer, comprising:

forming a first opening in a dielectric layer;

depositing a conformal coating of a first layer of a jacket material on said dielectric layer and forming a second opening in said first opening, wherein said jacket material exhibits a first resistivity $\rho 1$;

depositing a core material on said conformal coating, wherein said core material exhibits a second resistivity $\rho 2$ and $\rho 2$ is less than $\rho 1$;

reflowing said core material wherein said core material partially fills said second opening; and

depositing a second layer of said jacket material over said core material and said first layer of said jacket material, filling said second opening and forming a wire, wherein said core material is surrounded by said jacket material.

2. The method of claim 1, wherein said first opening defines a volume and said jacket material is present in the range of 25 % to 75 % of said volume.

3. The method of claim 1, wherein an overburden of said second layer of said jacket material forms over a surface of said dielectric layer and said method further comprises planarizing said second layer of jacket material until said surface of said dielectric layer is exposed.

4. The method of claim 1, wherein said openings are formed in said dielectric layer by photolithography.

5. The method of claim 1, wherein said conformal coating is deposited using chemical vapor deposition.

6. The method of claim 1, wherein said core material is deposited using physical vapor deposition.

7. The method of claim 1, wherein said core material includes one or more metals selected from the group consisting of copper, aluminum, gold and silver.

8. The method of claim 1, wherein said jacket material includes one or more metals selected from the group consisting of tungsten, cobalt, ruthenium and molybdenum.

9. The method of claim 1, wherein said core material comprises copper and said jacket material excludes copper.

10. A metallization layer, comprising:

an opening defined in a dielectric layer; and

a wire within said opening; wherein said wire includes a core material surrounded by a jacket material, wherein said jacket material exhibits a first resistivity $\rho 1$ and said core material exhibits a second resistivity $\rho 2$ and $\rho 2$ is less than $\rho 1$.

11. The metallization layer of claim 10, wherein said jacket material is present in the range of 25 % to 75 % of the volume of said opening.

12. The metallization layer of claim 10, wherein said dielectric layer exhibits a dielectric constant of lower than 3.9.

13. The metallization layer of claim 11, wherein said dielectric layer exhibits a dielectric constant in the range of 1.5 to 3.8.

14. The metallization layer of claim 10, wherein said dielectric layer includes one or more materials selected from the group consisting of fluorine-doped silicon dioxide, carbon-doped silicon dioxide, organo silicate glass, silicon oxycarbide, hydrogenated silicon oxycarbide, porous silicon dioxide, and organic polymer dielectrics such as polyimide, polytetrafluoroethylene, polynorbornenes, benzocyclobutene, hydrogen silsequioxane and methylsilsesquioxane.

15. The metallization layer of claim 10, wherein said jacket material exhibits a resistivity of 5.0 $\mu\Omega \cdot cm$ or greater.

16. The metallization layer of claim 10, wherein said core material exhibits a resistivity of 4.0 $\mu\Omega \cdot cm$ or less.

17. The metallization layer of claim 10, wherein said core material includes copper and said jacket material excludes copper.

18. The metallization layer of claim 10, wherein said core material exhibits a first melting temperature and said jacket material exhibits a second melting temperature, wherein said first melting temperature is less than said second melting temperature.

19. The metallization layer of claim 10, wherein the core material includes one or more metals selected from the group consisting of copper, aluminum, gold and silver.

20. The metallization layer of claim 10, wherein said jacket material includes one or more metals selected from the group consisting of tungsten, cobalt, ruthenium and molybdenum.

21. The metallization layer of claim 10, wherein said core material is a reflowed core material.

22. An integrated circuit, comprising:

one or more dielectric layers;

a plurality of openings defined in each of said dielectric layers; and

a plurality of wires connected to one or more components associated with said integrated circuit, wherein each wire is positioned within one of said openings and said wires include a core material surrounded by a jacket material, wherein said jacket material exhibits a first resistivity $\rho 1$ and said core material exhibits a second resistivity $\rho 2$ and $\rho 2$ is less than $\rho 1$.