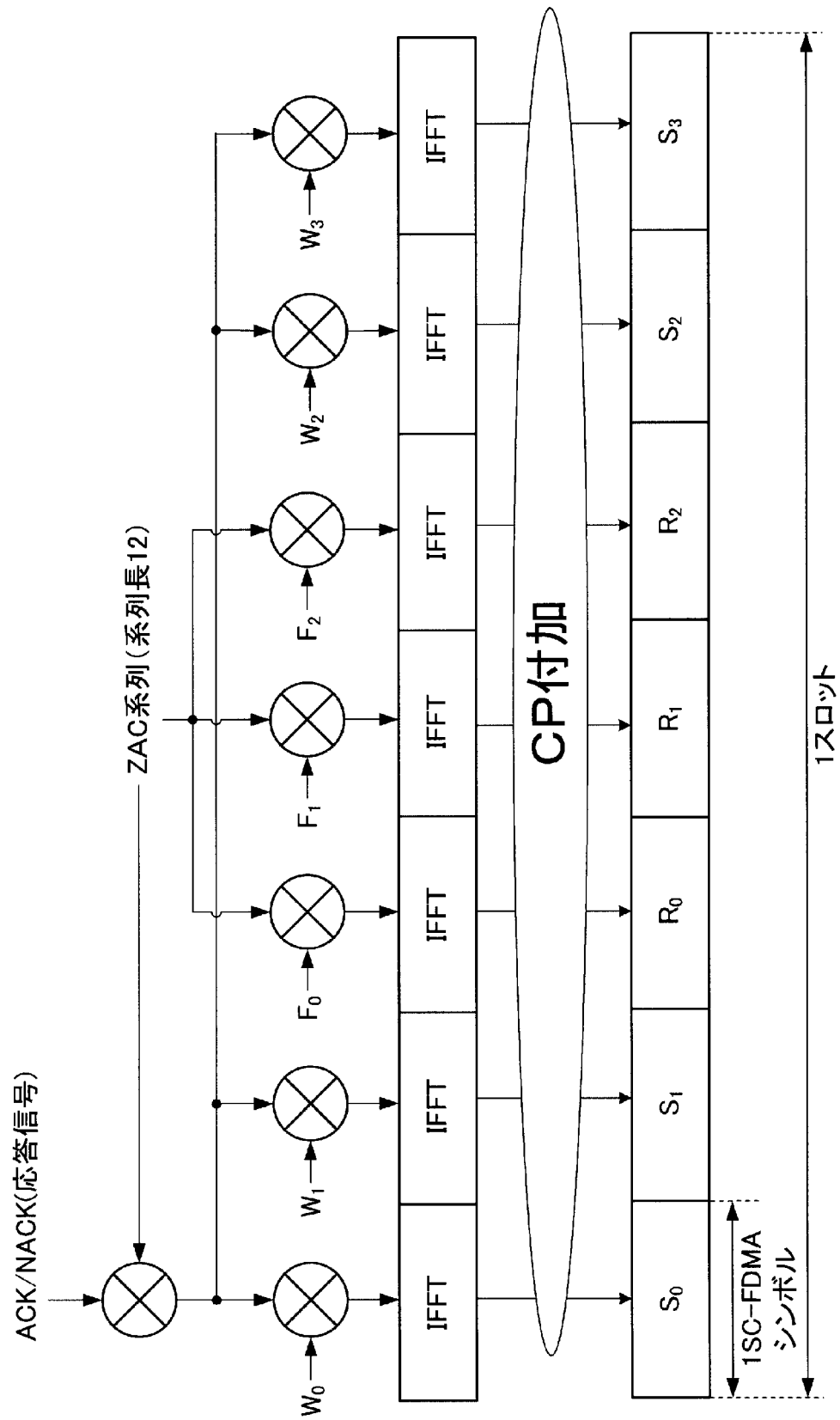
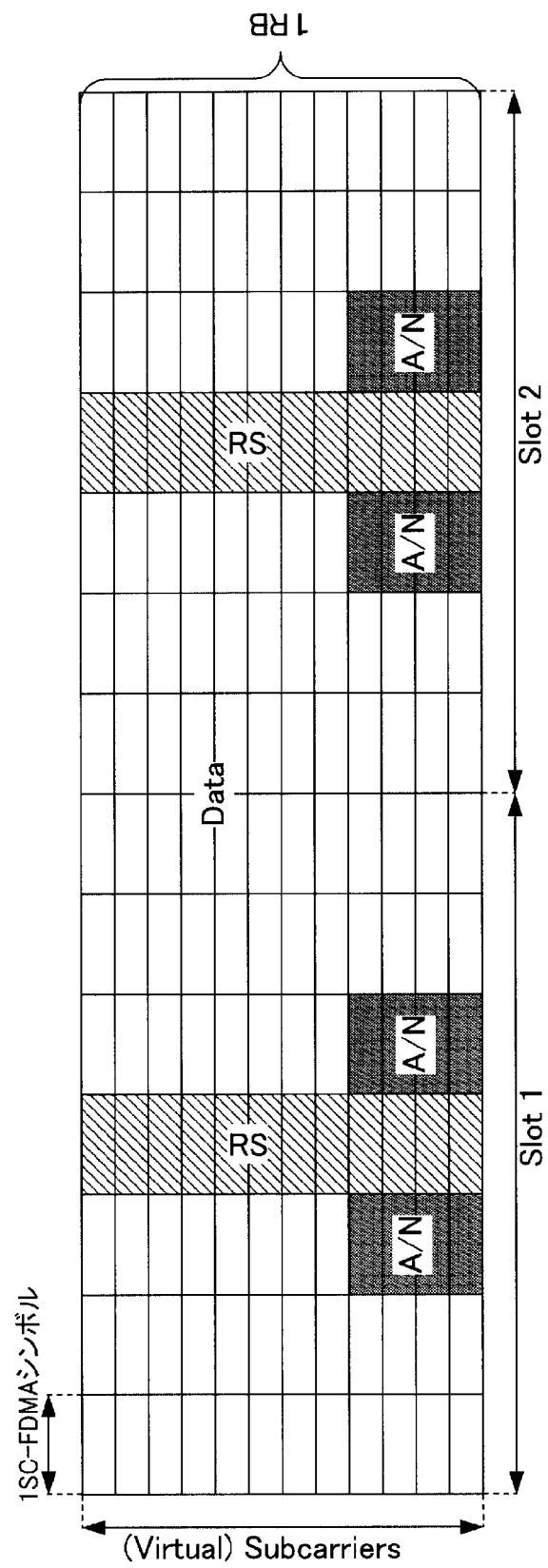


[図1]



[図2]



[図3]

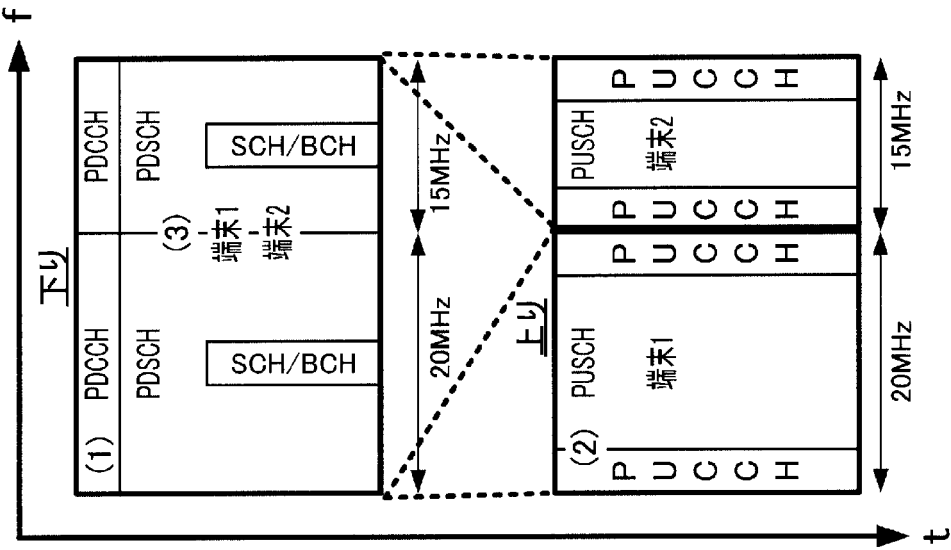


図3B

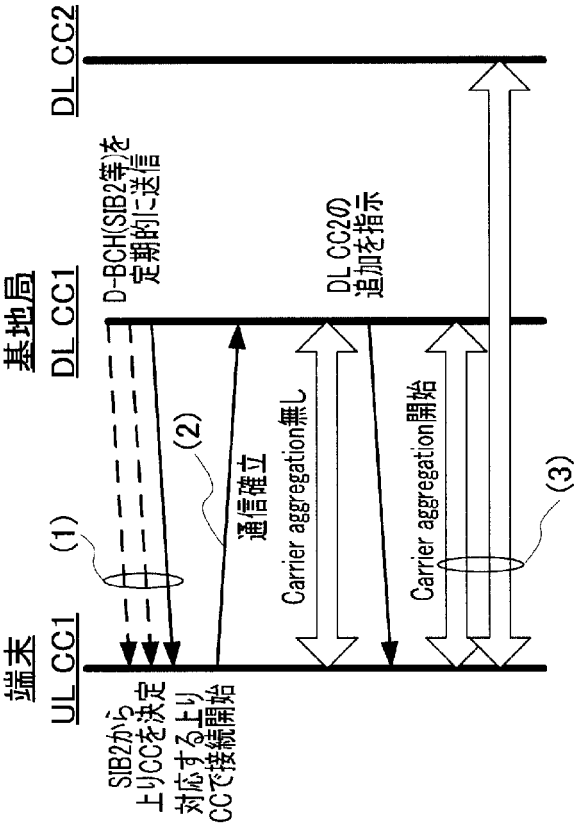
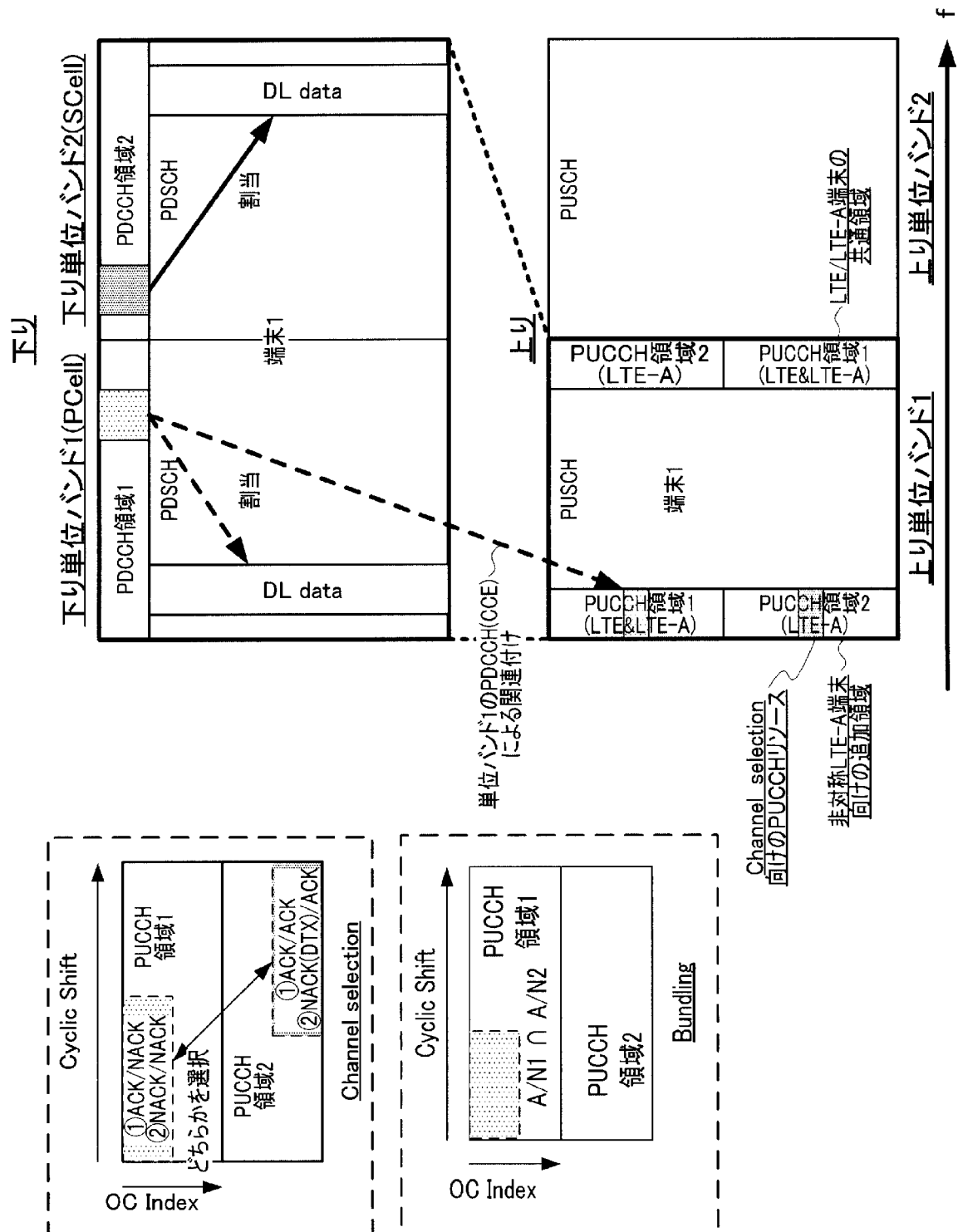
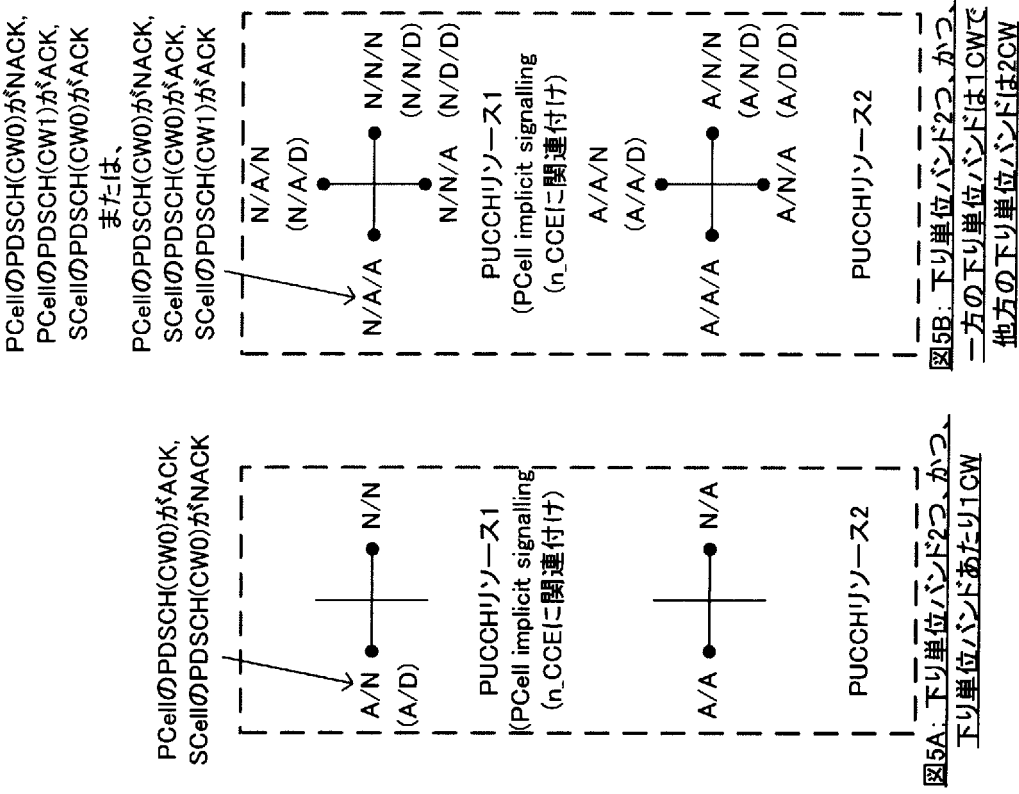


図3A

[図4]



[図5]



[図6]

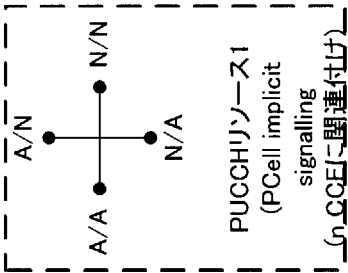


図6B: 下り単位バンド1つ、かつ、2CW

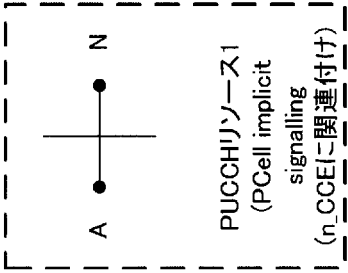


図6A: 下り単位バンド1つ、かつ、1CW

[図7]

Table 5-2: 3 ACK/NAK Bits

	Ch1		Ch2	
	RS	Data	RS	Data
N, N, N	1	1	0	0
N, N, A	1	-j	0	0
N, A, N	1	j	0	0
N, A, A	1	-1	0	0
A, N, N	0	0	1	1
A, N, A	0	0	1	-j
A, A, N	0	0	1	j
A, A, A	0	0	1	-1

Table 5-1: 2 ACK/NAK Bits

	Ch1		Ch2	
	RS	Data	RS	Data
N, N	1	1	0	0
A, N	1	-1	0	0
N, A	0	0	1	1
A, A	0	0	1	-1

- Data applied to SC-FDMA symbols 0, 1, 5, 6
- RS applied to SC-FDMA symbols 2, 3, 4
- Repeated transmission in two slots

[図8]

Table 6: 4 ACK/NAK Bits

	Ch 1		Ch 2		Ch 3		Ch 4	
	RS	Data	RS	Data	RS	Data	RS	Data
N, N, N, N	1	1	0	0	0	0	0	0
N, N, N, A	1	-j	0	0	0	0	0	0
N, N, A, N	1	j	0	0	0	0	0	0
N, N, A, A	1	-1	0	0	0	0	0	0
N, A, N, N	0	0	1	1	0	0	0	0
N, A, N, A	0	0	1	-j	0	0	0	0
N, A, A, N	0	0	1	j	0	0	0	0
N, A, A, A	0	0	1	-1	0	0	0	0
A, N, N, N	0	0	0	0	1	1	0	0
A, N, N, A	0	0	0	0	1	-j	0	0
A, N, A, N	0	0	0	0	1	j	0	0
A, N, A, A	0	0	0	0	1	-1	0	0
A, A, N, N	0	0	0	0	0	0	1	1
A, A, N, A	0	0	0	0	0	0	1	-j
A, A, A, N	0	0	0	0	0	0	1	j
A, A, A, A	0	0	0	0	0	0	1	-1

[図9]

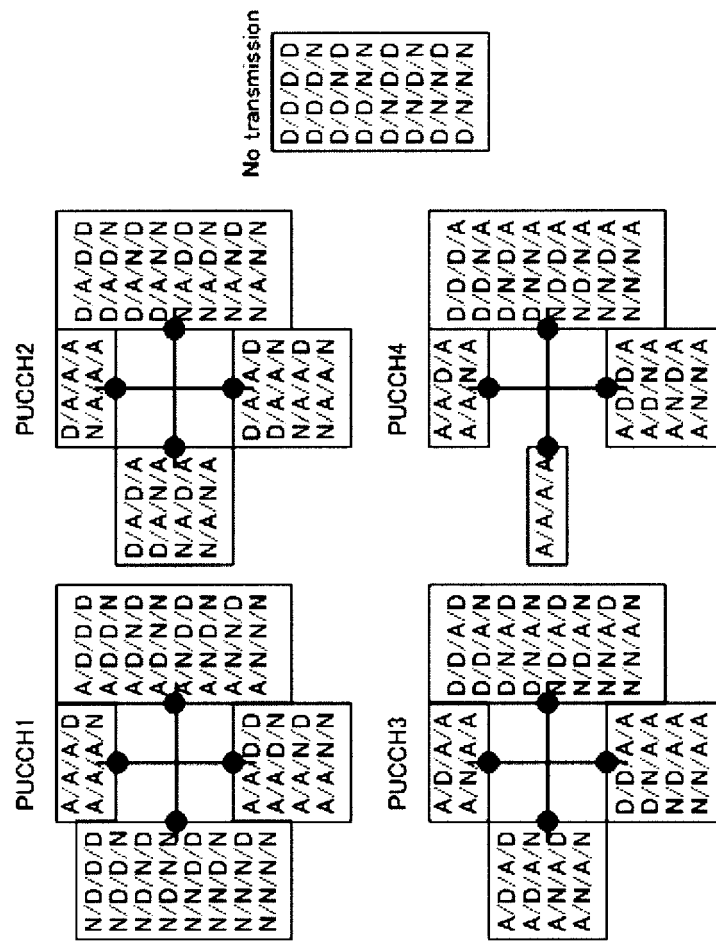
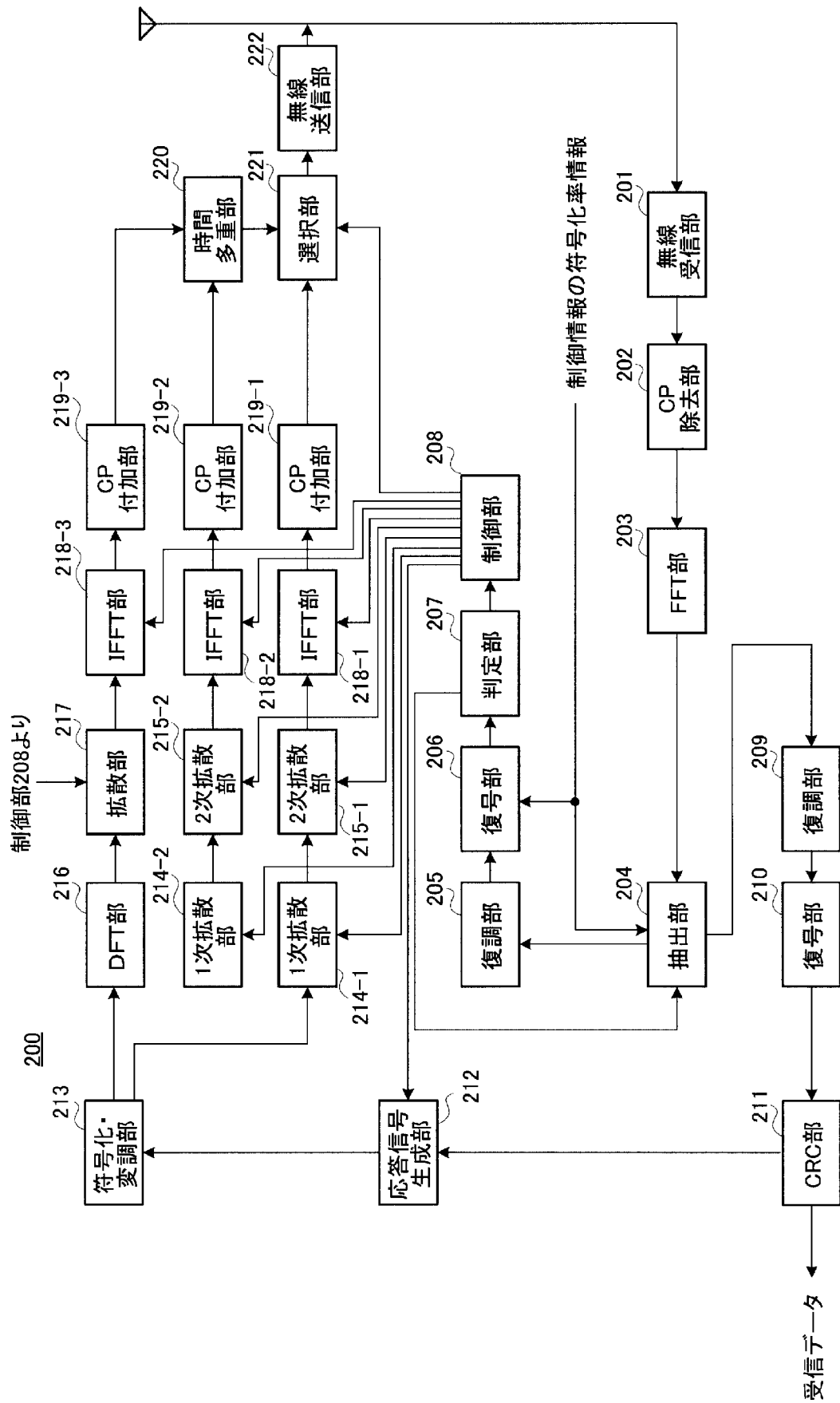
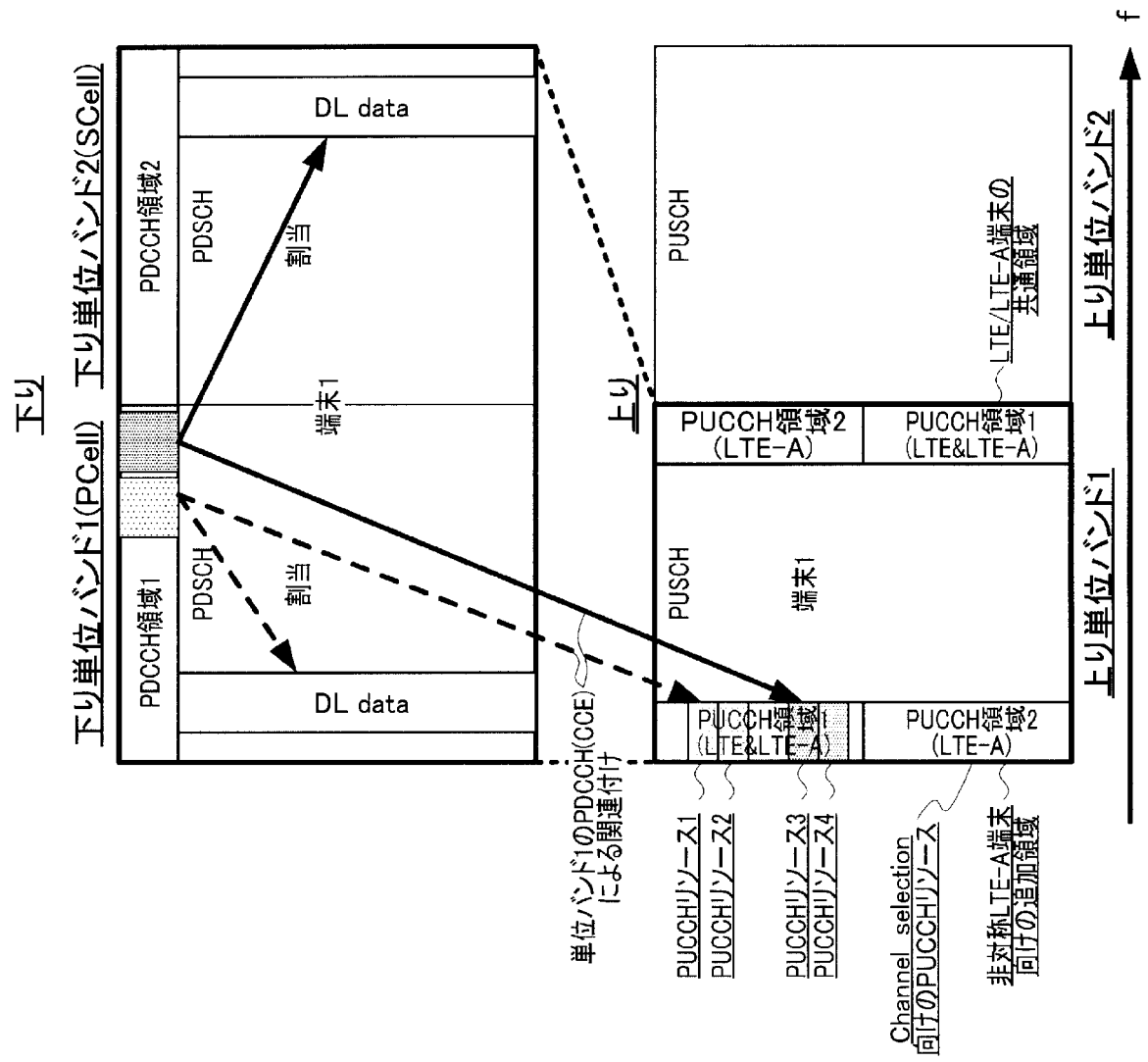


Figure 5 Mapping rules in case that four DL CCs are configured (Alternative 1-2)

[図11]



[図12]



[図15]

PCell	SCell	PUCCHリソース			
		1	2	3	4
A,A	A,A		-1		
A,N	A,A			-j	
N,A	A,A		-j		
N,N	A,A				-1
A,A	A,N		j		
A,N	A,N			1	
N,A	A,N		1		
N,N	A,N				j
A,A	N,A			-1	
A,N	N,A			j	
N,A	N,A				-j
N,N	N,A				1
A,A	N,N	-1			
A,N	N,N	j			
N,A	N,N	-j			
N,N	N,N	1			
A,A	D,D	-1			
A,N	D,D	j			
N,A	D,D	-j			
N,N	D,D	1			
D,D	A,A				-1
D,D	A,N				j
D,D	N,A				1
D,D	N,N	No transmission			
D,D	D,D	No transmission			

[図17]

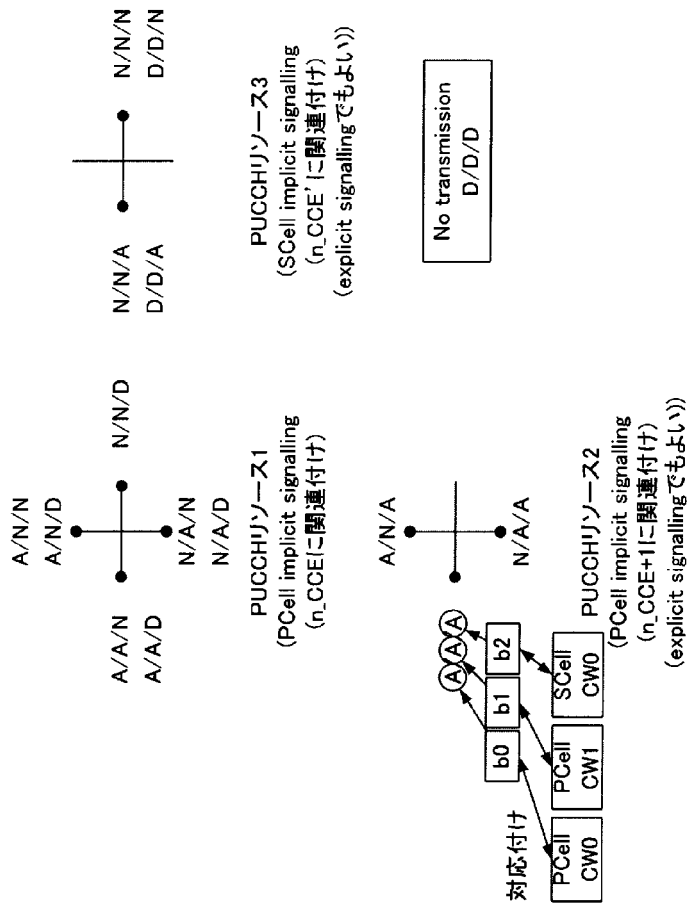


図17A

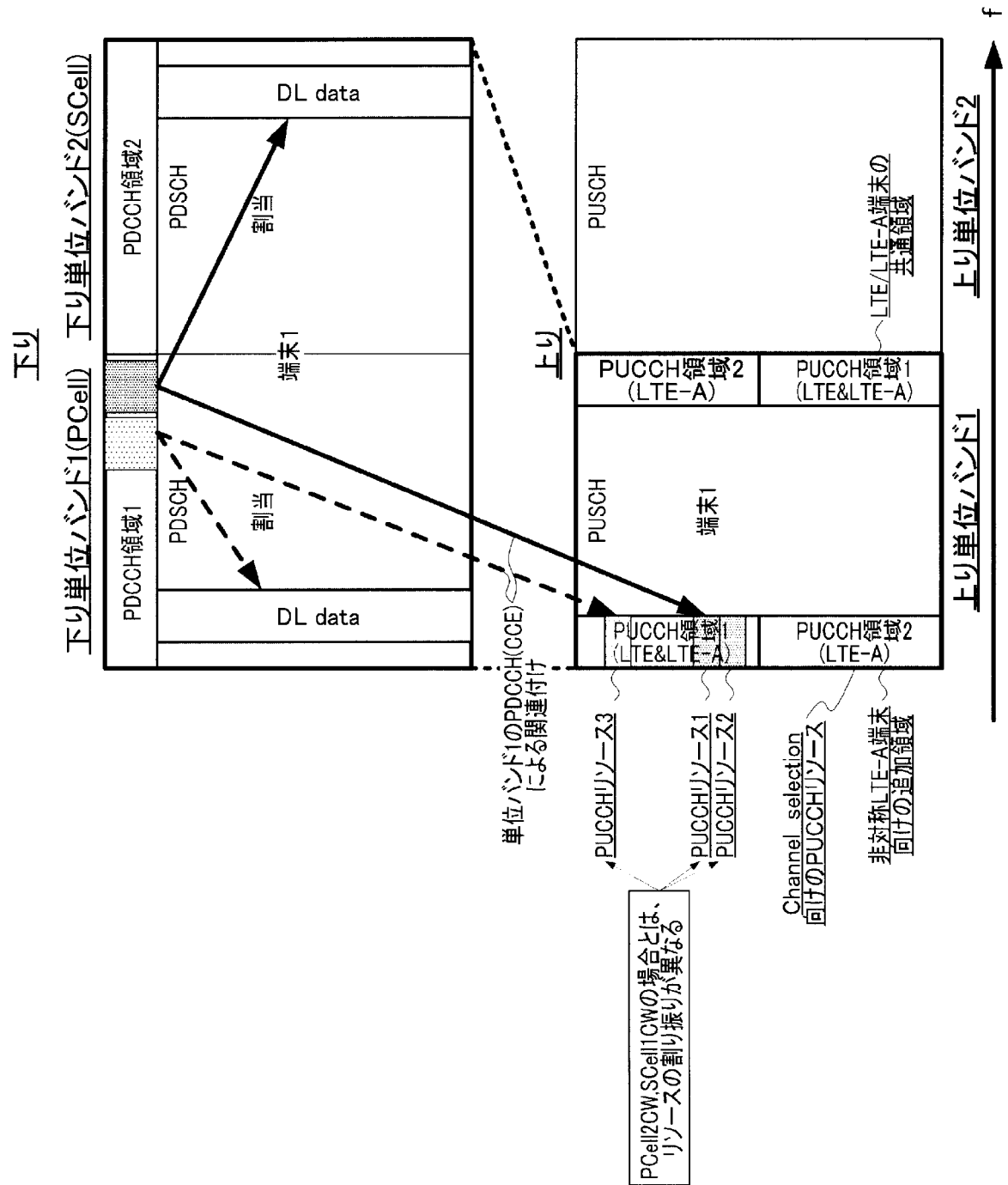
	PUCCHリソース				A:N=1:0or 0:1の個数	A/Nの偏り
	1	2	3			
b0	A	2	2	0	1	3
	N	2	1	2		
b1	A	2	2	0	1	3
	N	2	1	2		
b2	A	0	3	1	2	6
	N	3	0	1		
Rel-8 fallback						format1bへのfallback

図17B

[図18]

SDM Cell	non-SDM Cell	PUCCHリソース		
		1	2	3
A,A	A		-1	
A,N	A		j	
N,A	A		-j	
N,N	A			-1
A,A	N	-1		
A,N	N	j		
N,A	N	-j		
N,N	N			1
A,A	D	-1		
A,N	D	j		
N,A	D	-j		
N,N	D	1		
D,D	A			-1
D,D	N			1
D,D	D	No transmission		

[図19]



[図20]

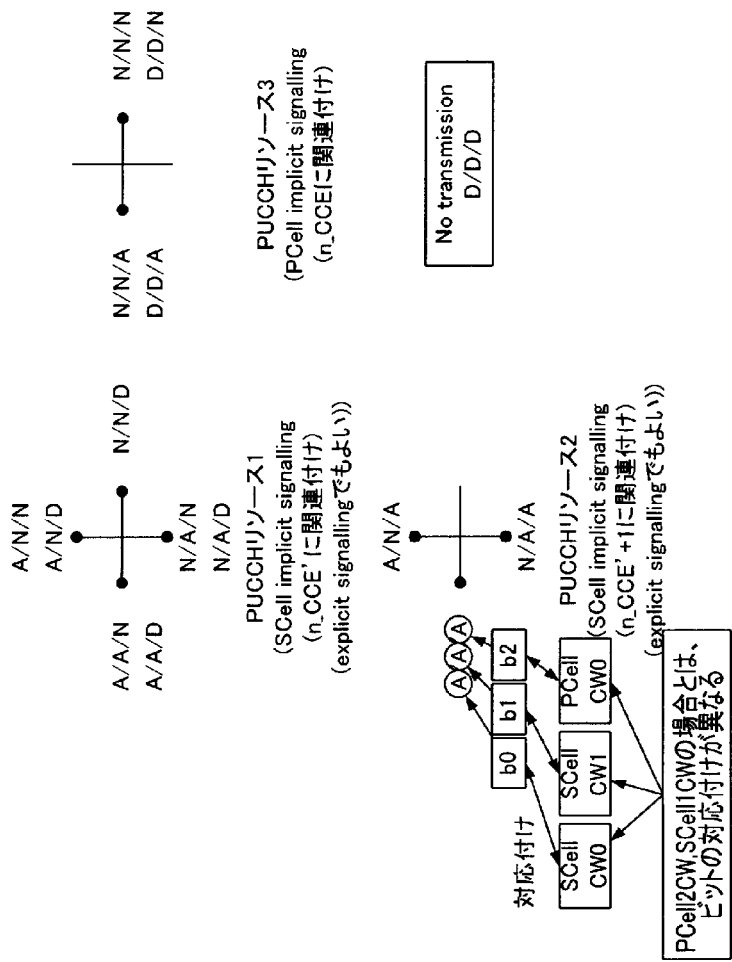


図20A

	PUCCHリソース						A/N=1.0 or 0.1の個数	A/Nの偏り
	1	2	3					
b0	A	2	2	0			1	3
	N	2	1	2				
b1	A	2	2	0			1	3
	N	2	1	2				
b2	A	0	3	1			2	6
	N	3	0	1				
Rel-8 fallback	x	x	0				format1aへのfallback	

PCell2CW, SCell1CWの場合とは、
fallbackするformatが異なる

図20B

[図21]

SDM Cell	non-SDM Cell	PUCCHリソース		
		1	2	3
A,A	A		-1	
A,N	A		j	
N,A	A		-j	
N,N	A			-1
A,A	N	-1		
A,N	N	j		
N,A	N	-j		
N,N	N			1
A,A	D	-1		
A,N	D	j		
N,A	D	-j		
N,N	D	1		
D,D	A			-1
D,D	N			1
D,D	D	No transmission		

[図22]

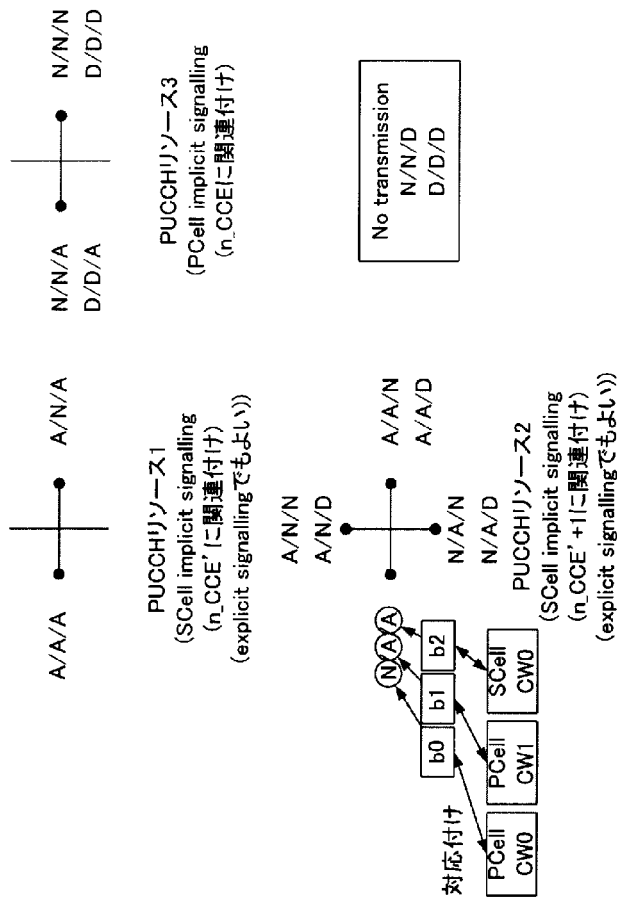


図22A

	PUCCHリソース				A/N=1:0or 0:1の個数	A/Nの偏り
	1	2	3			
b0	A	2	2	0	2	4
	N	0	2	2		
b1	A	1	3	0	1	4
	N	1	1	2		
b2	A	2	1	1	1	4
	N	0	3	1		
Rel-8 fallback	x	x	x		format1bへのfallback	
Rel-8 fallback	x	x		0	format1aへのfallback	

図22B

[図23]

SDM Cell	non-SDM Cell	PUCCHリソース		
		1	2	3
A,A	A	-1		
A,N	A	1		
N,A	A		-1	
N,N	A			-1
A,A	N		1	
A,N	N		j	
N,A	N		-j	
N,N	N			1
A,A	D		1	
A,N	D		j	
N,A	D		-j	
N,N	D	No transmission		
D,D	A			-1
D,D	N			1
D,D	D	No transmission		

[図24]

PCell	SCell	PUCCH resource	
		1	2
A	A		1
A	N	-1	
N	A		-1
N	N	1	
D	A		-1
D	N	No transmission	
A	D	-1	
N	D	1	
D	D	No transmission	

[図25]

SDM Cell	non- SDM	PUCCH resource		
		1	2	3
A,A	A		-1	
A,N	A		j	
N,A	A		-j	
N,N	A			-1
A,A	N	-1		
A,N	N	j		
N,A	N	-j		
N,N	N			1
A,A	D	-1		
A,N	D	j		
N,A	D	-j		
N,N	D			
N,N	D	1 if PCell is SDM configured, No transmission if PCell is non-SDM configured		
D,D	A			-1
D,D	N			1 if PCell is SDM configured No transmission if PCell is non-SDM configured
D,D	D	No transmission		

[図26]

PCell	SCell	PUCCH resource			
		1	2	3	4
A,A	A,A		-1		
A,N	A,A				-j
N,A	A,A		-j		
N,N	A,A			-1	
A,A	A,N		j		
A,N	A,N				1
N,A	A,N		1		
N,N	A,N			j	
A,A	N,A				-1
A,N	N,A				j
N,A	N,A			1	
N,N	N,A			-j	
A,A	N,N	-1			
A,N	N,N	j			
N,A	N,N	-j			
N,N	N,N	1			
A,A	D,D	-1			
A,N	D,D	j			
N,A	D,D	-j			
N,N	D,D	1			
D,D	A,A			-1	
D,D	A,N			j	
D,D	N,A			-j	
D,D	N,N	No transmission			
D,D	D,D	No transmission			

[図28]

図28A: ACK/NACKビット数が2の場合
のマッピングテーブル

ACK/NACK state		ACK/NACK resource	
b0	b1	Ch1	Ch2
A	A		-1
A	N/D	-1	
N/D	A		+1
N	N/D	+1	
D	N/D	No transmission	
PCell		SCell	

図28B: ACK/NACKビット数が3の場合
のマッピングテーブル

ACK/NACK state			ACK/NACK resource		
b0	b1	b2	Ch1	Ch2	Ch3
A	A	A		-1	
A	N/D	A		+j	
N/D	A	A		-j	
N/D	N/D	A			-1
A	A	N/D	-1		
A	N/D	N/D	+j		
N/D	A	N/D	-j		
N/D	N/D	N			+1
N	N/D	D	+1		
D	N	D	+1		
D	D	D	No transmission		

2GW送信までをサ
ポートする送信モー
ドが設定されたCell
(MIMO Cell)

1GW送信のみをサ
ポートする送信モー
ドが設定されたCell
(non-MIMO Cell)

図28C: ACK/NACKビット数が4の場合
のマッピングテーブル

ACK/NACK state				ACK/NACK resource			
b0	b1	b2	b3	Ch1	Ch2	Ch3	Ch4
A	A	A	A		-1		
A	N/D	A	A			-j	
N/D	A	A	A				-1
N/D	N/D	A	A				
A	A	A	N/D		+j		
A	N/D	A	N/D			+1	
N/D	A	A	N/D		+1		
N/D	N/D	A	N/D				+j
A	A	N/D	A			-1	
A	N/D	N/D	A			+j	
N/D	A	N/D	A				j
N/D	N/D	N/D	A				+1
A	A	N/D	N/D	-1			
A	N/D	N/D	N/D	+j			
N/D	A	N/D	N/D	-j			
N	N/D	N/D	N/D	+1			
D	N	N/D	N/D	+1			
D	D	N/D	N/D	+1			
PCell				SCell			
				No transmission			

[図29]

Configured CWs on PCell	Configured CWs on SCell1	Configured CWs on SCell2	Configured CWs on SCell3	Number of ACK/NACK
1	1	-	-	2
1	2	-	-	3
2	1	-	-	3
2	2	-	-	4
1	1	1	-	3
1	1	2	-	4
1	2	1	-	4
2	1	1	-	4
1	1	1	1	4

2CCs

3CCs

4CCs

[図30]

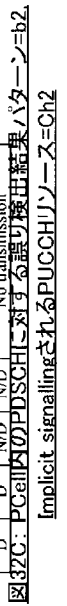
PCell SCell1 SCell2 SCell3

ACK/NACK state				ACK/NACK resource			
b0	b1	b2	b3	Ch1	Ch2	Ch3	Ch4
A	A	A	A		-1		
A	N/D	A	A			-1	
N/D	A	A	A		-j		
N/D	N/D	A	A				-1
A	A	A	N/D		+j		
A	N/D	A	N/D			+1	
N/D	A	A	N/D		+1		
N/D	N/D	A	N/D				+j
A	A	N/D	A			-1	
A	N/D	N/D	A			+j	
N/D	A	N/D	A				-j
N/D	N/D	N/D	A				+1
A	A	N/D	N/D	-1			
A	N/D	N/D	N/D	+j			
N/D	A	N/D	N/D	-j			
N	N/D	N/D	N/D	+1			
D	N	N/D	N/D	+1			
D	D	N/D	N/D	No transmission			

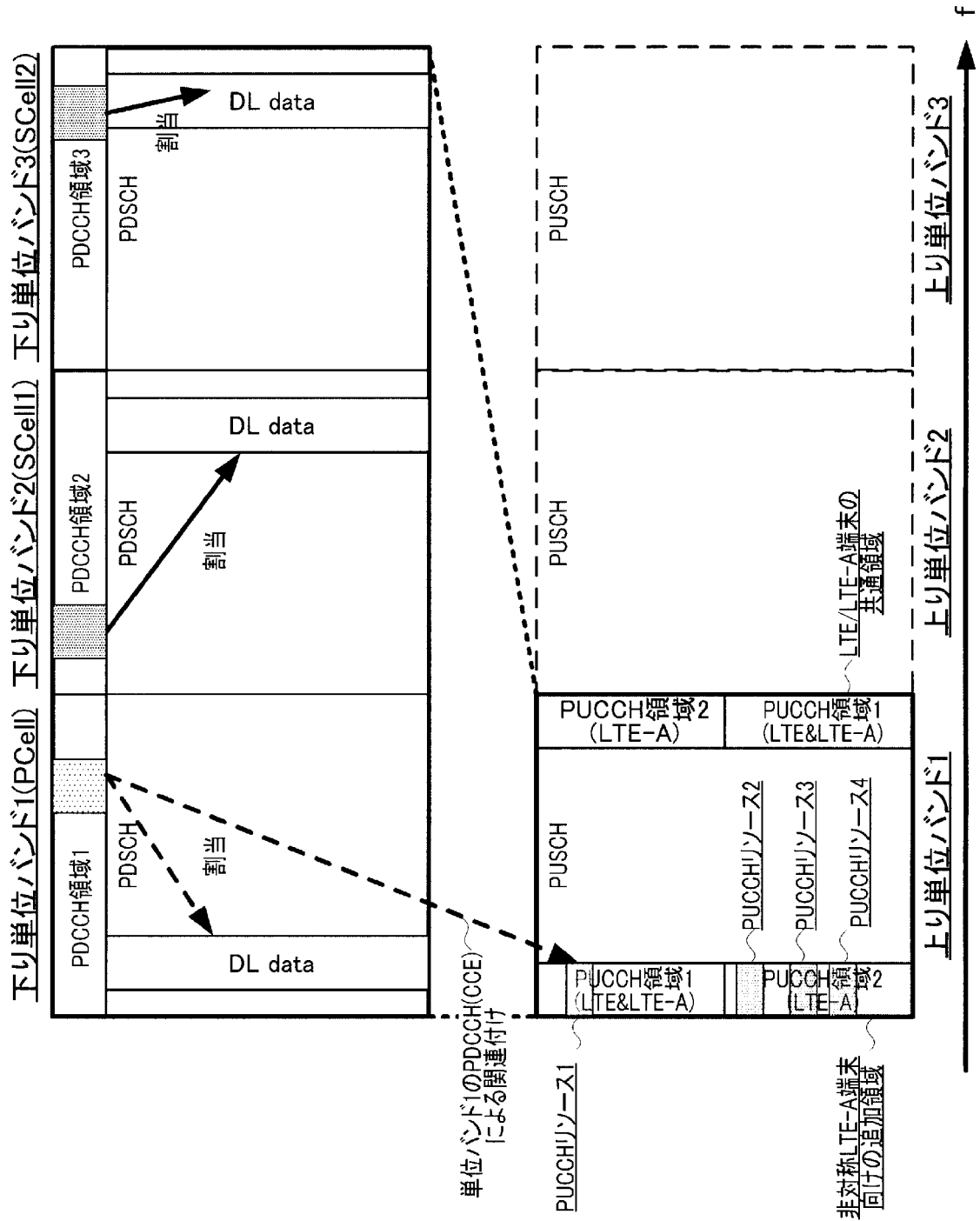
Explicit resources

Implicit resource
を使えない
(Explicit resource)

図32B: PCell内のPDSCHに対する誤り検出結果パターン=bl
Implicit signallingされるPUCCHリソース=Ch2



[図33]



[図34]

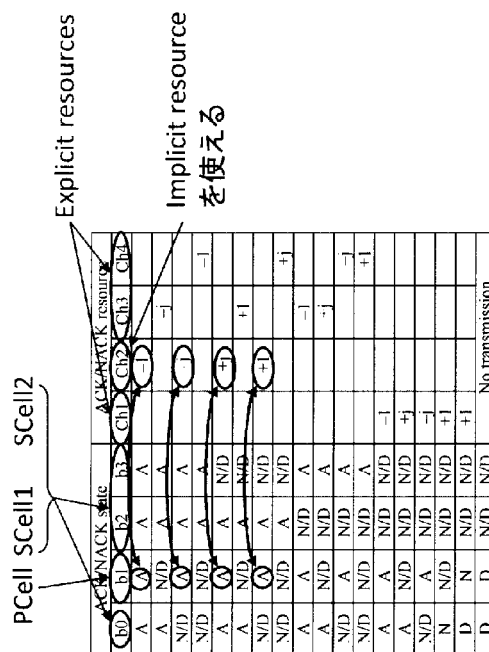


図34B: PCell内のPDSCHに対する誤り検出結果パターン=b0.

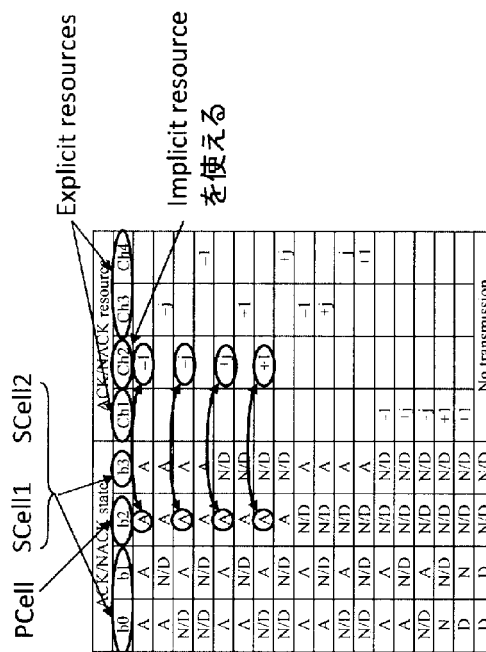


図34C: PCell内のPDSCHに対する誤り検出結果パターン=b2.

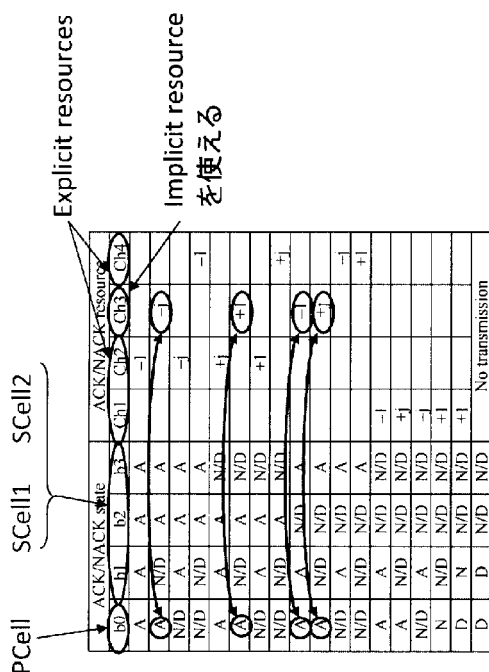
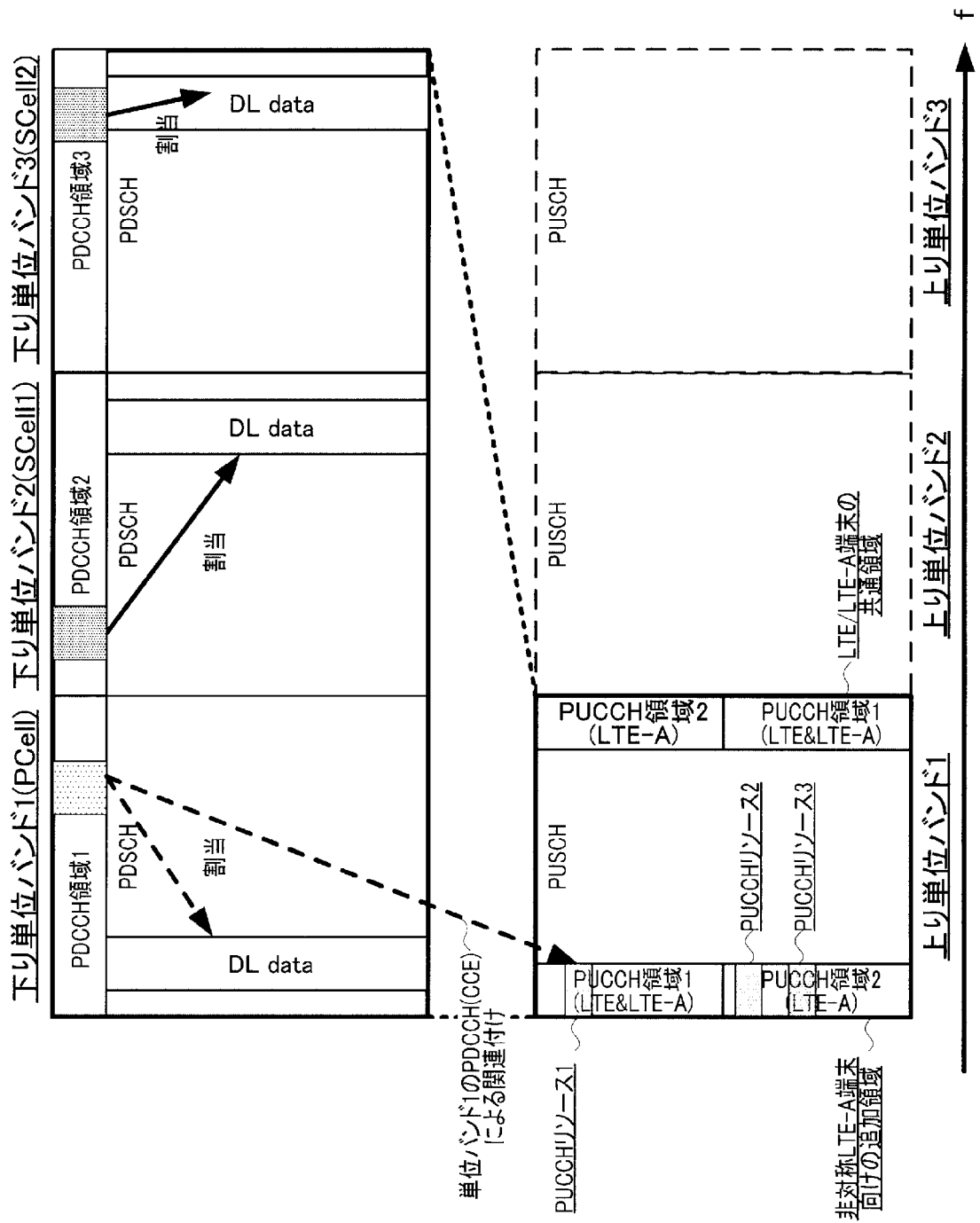


図34A: PCell内のPDSCHに対する誤り検出結果パターン=b0

[図35]



[図36]

