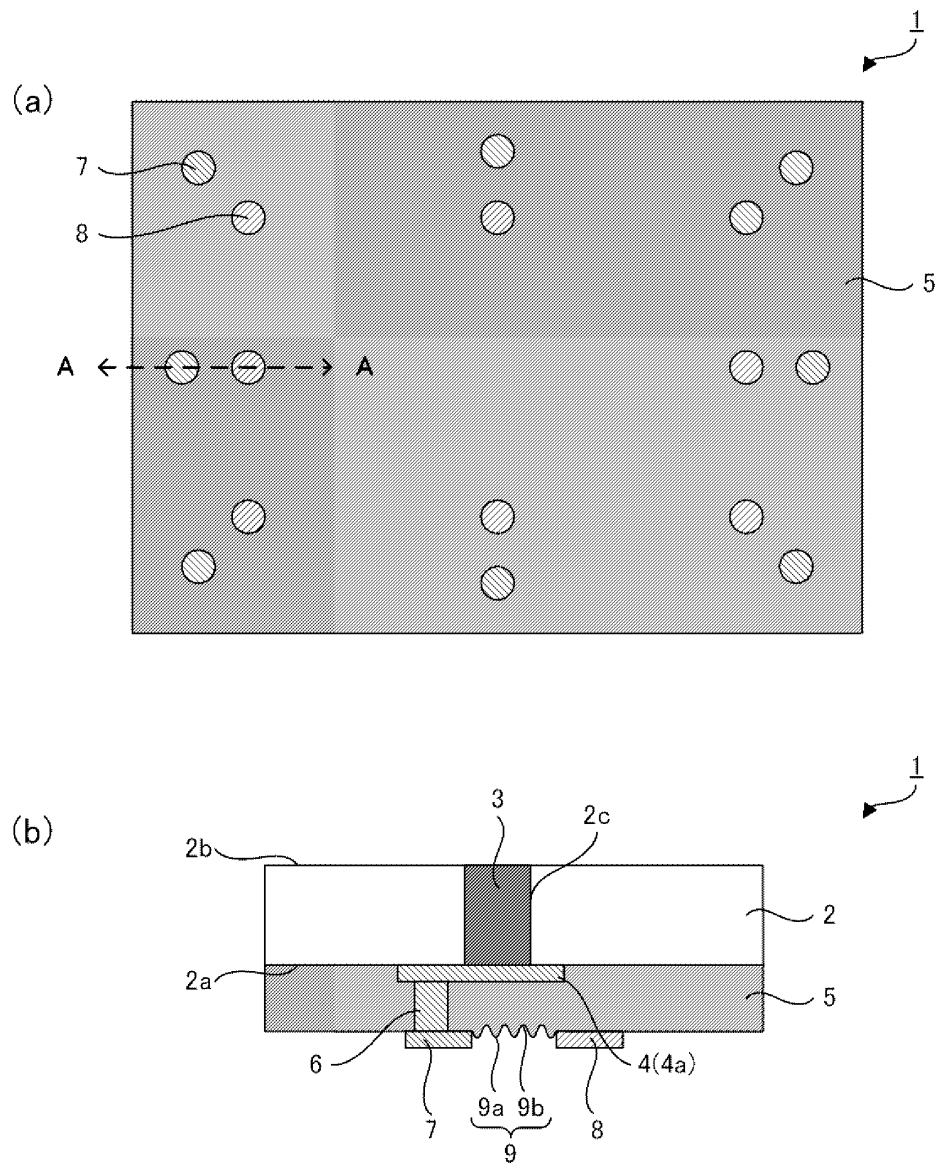


[図1]



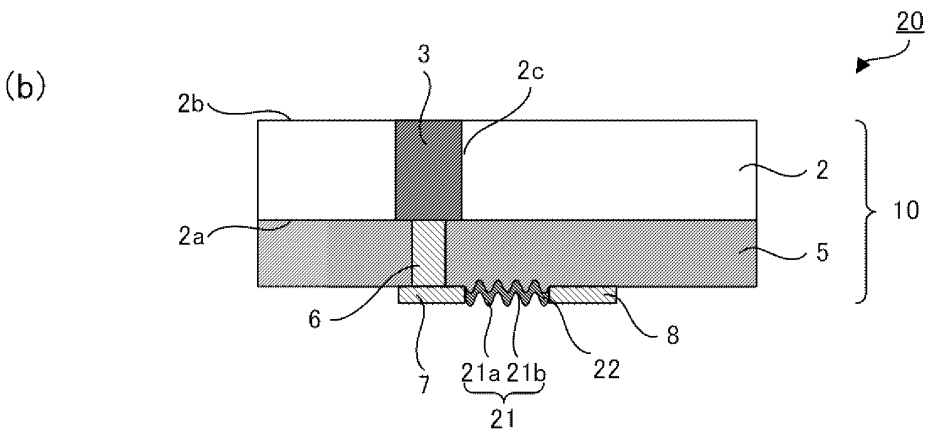
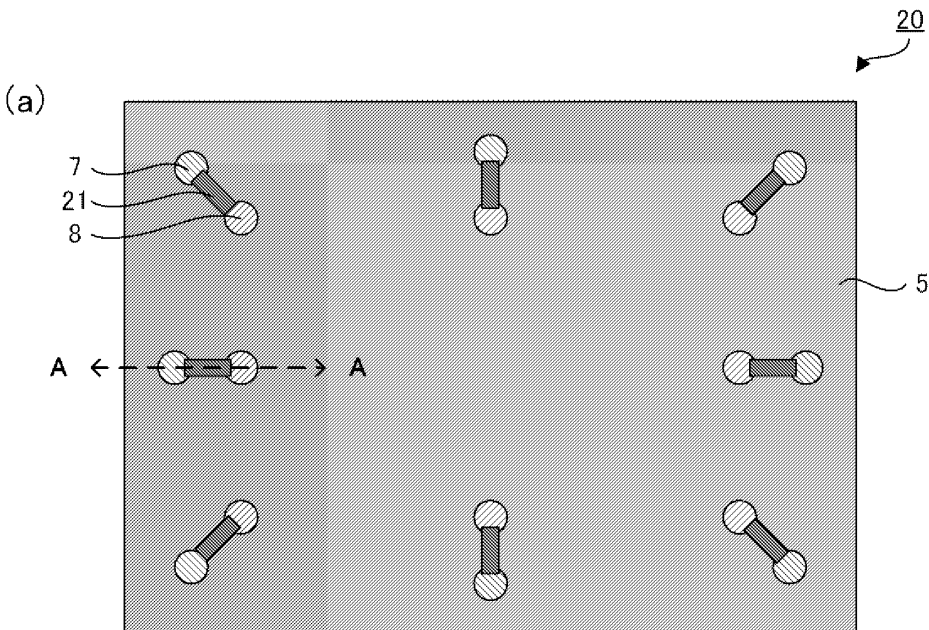


A cross-sectional view of a semiconductor device 40. The device includes a substrate 42. A layer 41 is formed on the substrate 42. A layer 8 is formed on layer 41. A layer 6 is formed on layer 8. A layer 7 is formed on layer 6. A layer 22 is formed on layer 7. A layer 4(4a) is formed on layer 22. A layer 2a is formed on layer 4(4a). A layer 2c is formed on layer 2a. A layer 2b is formed on layer 2c. A layer 3 is formed on layer 2b. A layer 31 is formed on layer 3. A layer 32 is formed on layer 31. A layer 5 is formed on layer 2a. A layer 2 is formed on layer 5. A layer 11 is formed on layer 2. A layer 1 is formed on layer 11. A layer 3 is formed on layer 1. A layer 31 is formed on layer 3. A layer 32 is formed on layer 31. A layer 5 is formed on layer 2a. A layer 2 is formed on layer 5. A layer 11 is formed on layer 2. A layer 1 is formed on layer 11. A layer 3 is formed on layer 1. A layer 31 is formed on layer 3. A layer 32 is formed on layer 31.

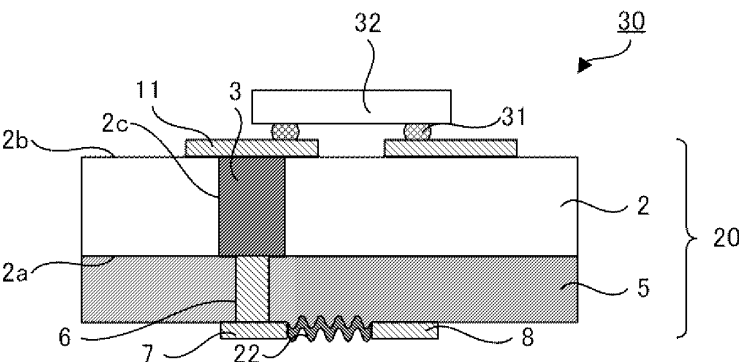
Figure 1(a) is a schematic diagram of a substrate 1. The substrate contains a central region 5. Within this region, there are several circular features, some of which are shaded with diagonal lines. A horizontal line A-A passes through two of these features. Labels 7 and 8 point to specific features on the left side of the central region 5.

[illegible]

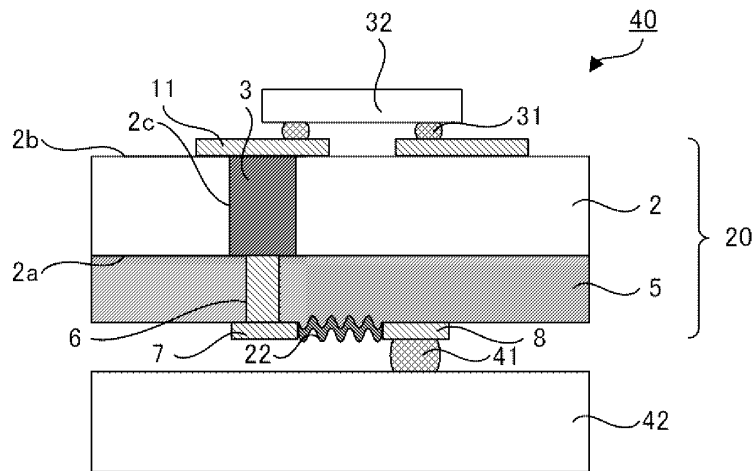
[図6]



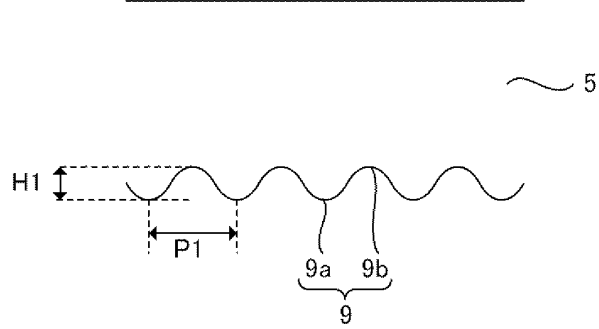
[図7]



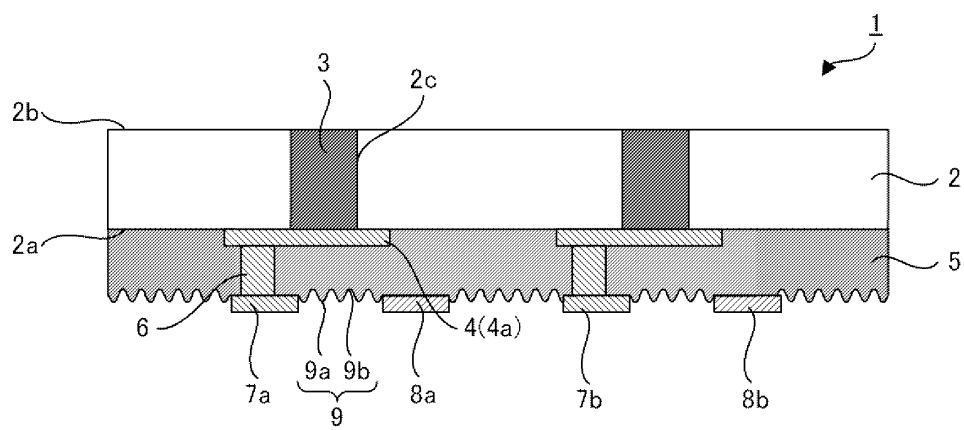
[図8]



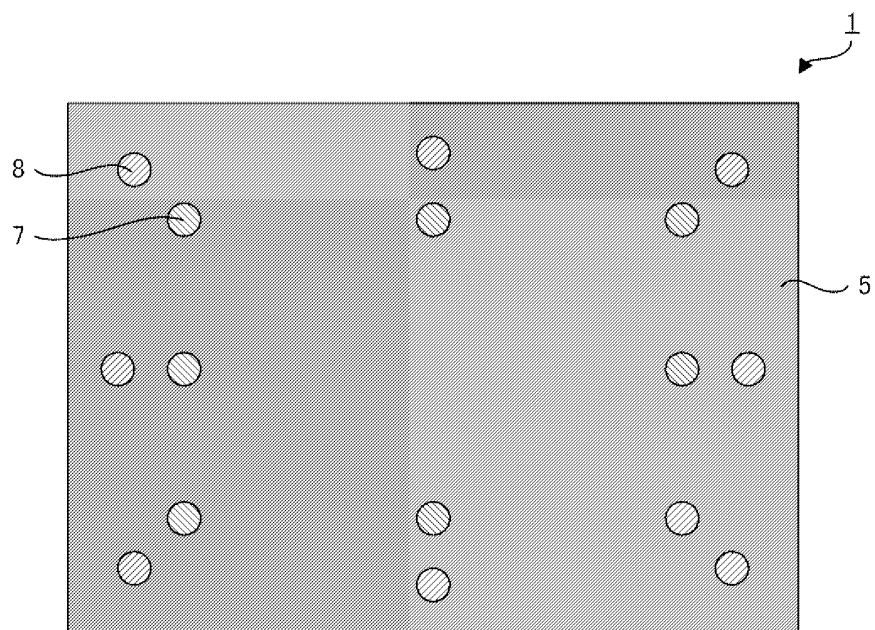
[図9]



[図10]



[図11]



[図12]

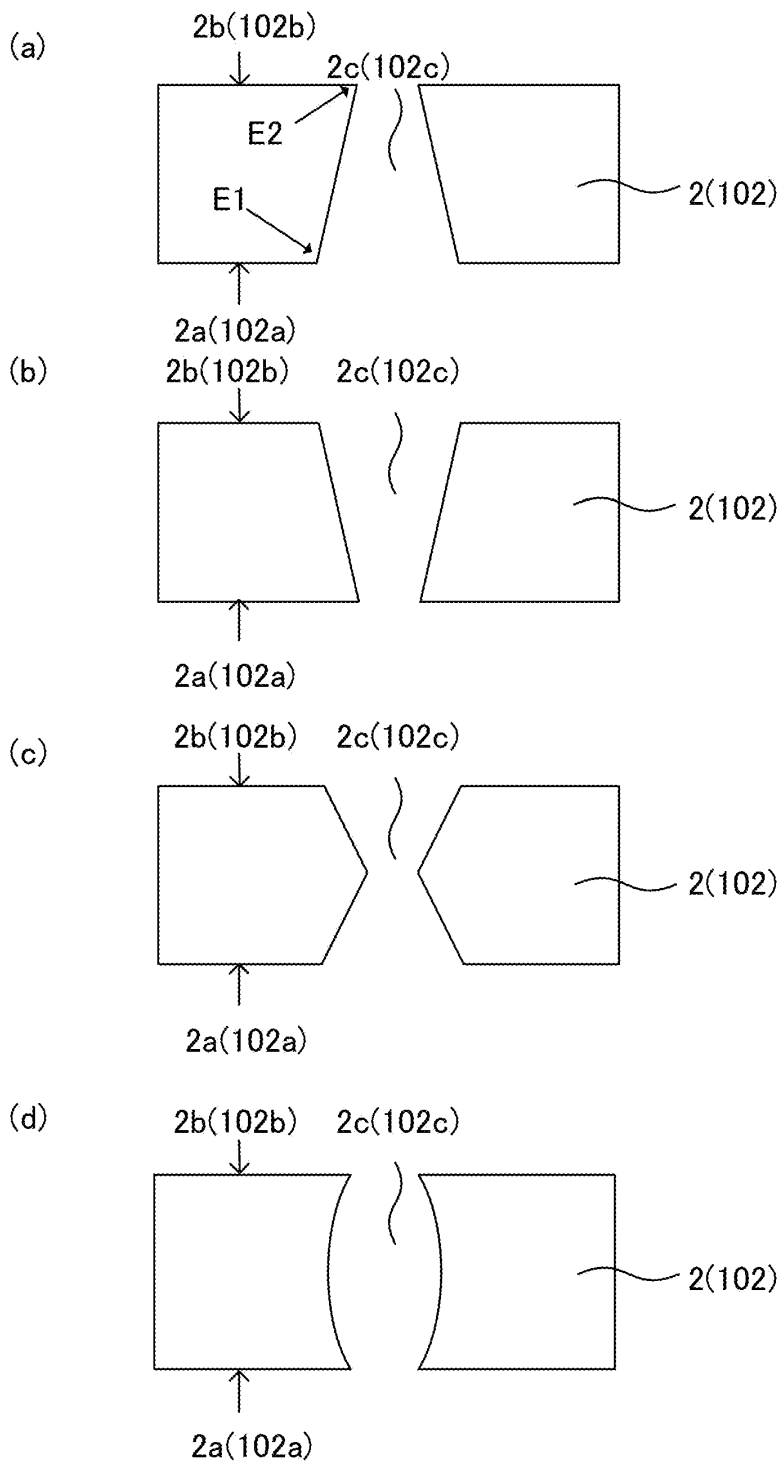
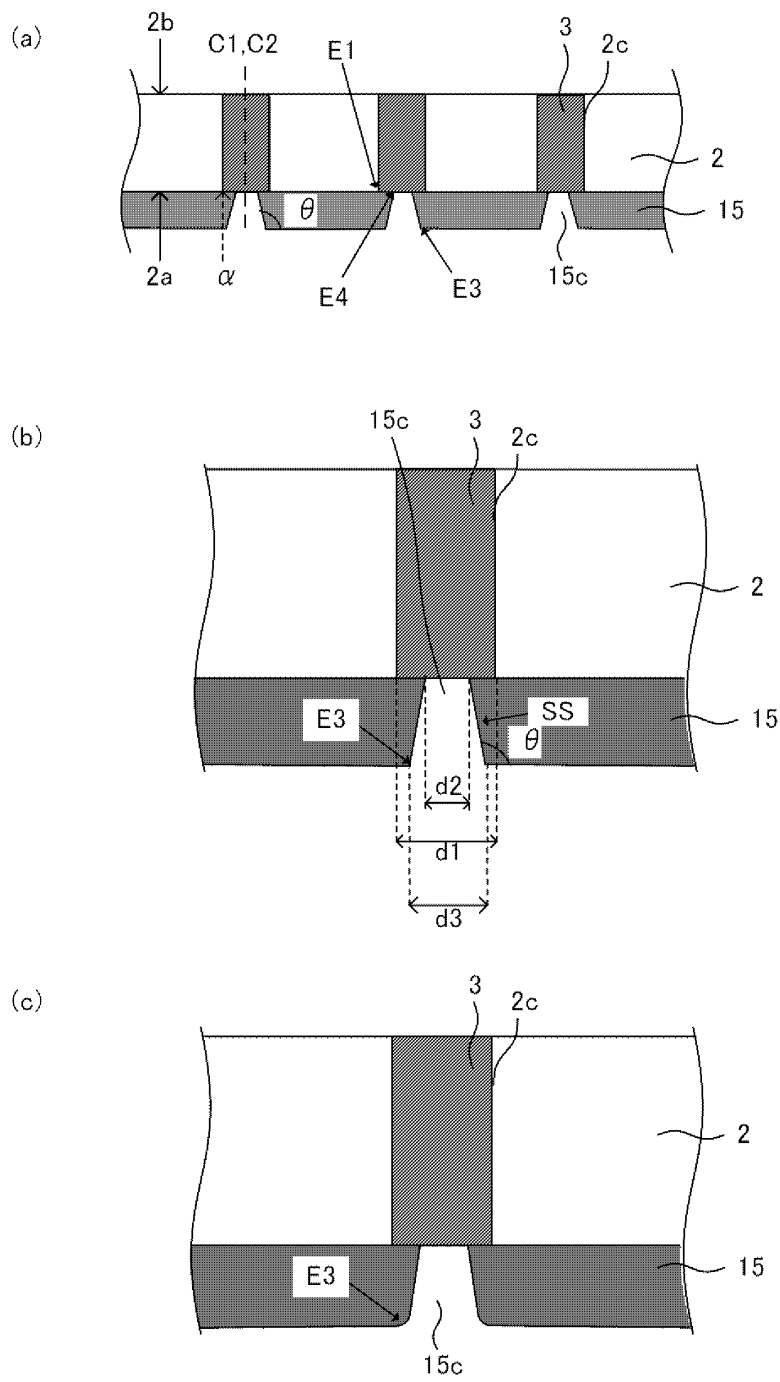


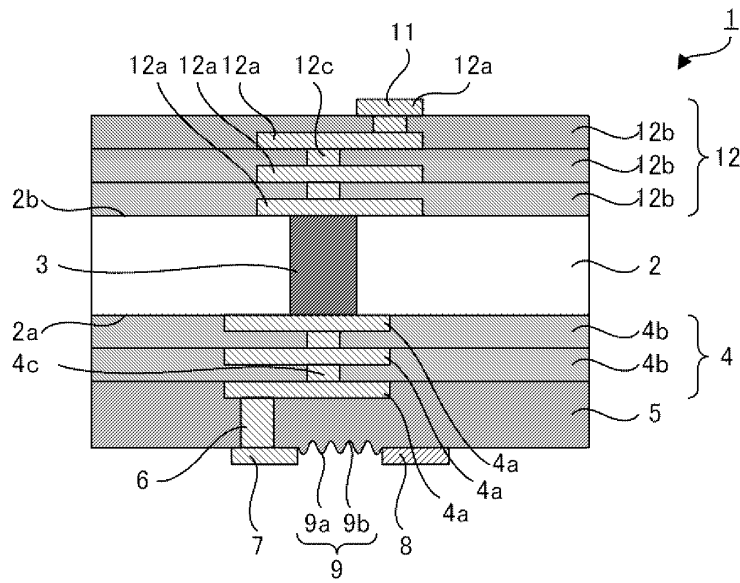
Figure 1 consists of two schematic diagrams, (a) and (b), illustrating a semiconductor device. Diagram (a) shows a cross-section of a substrate 2(102) with two regions 3(103) and two regions 2c(102c). Diagram (b) shows the same structure with additional regions G.

[図15]

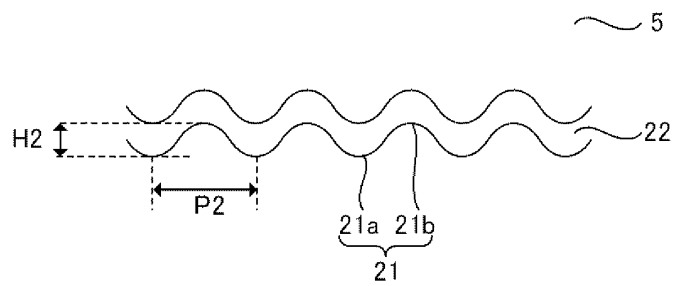




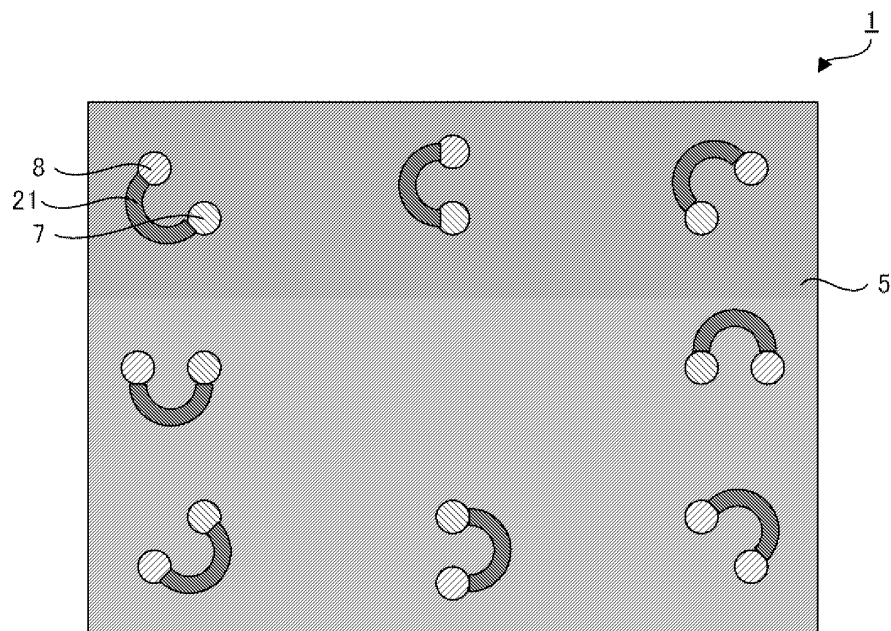
[図18]



[図19]

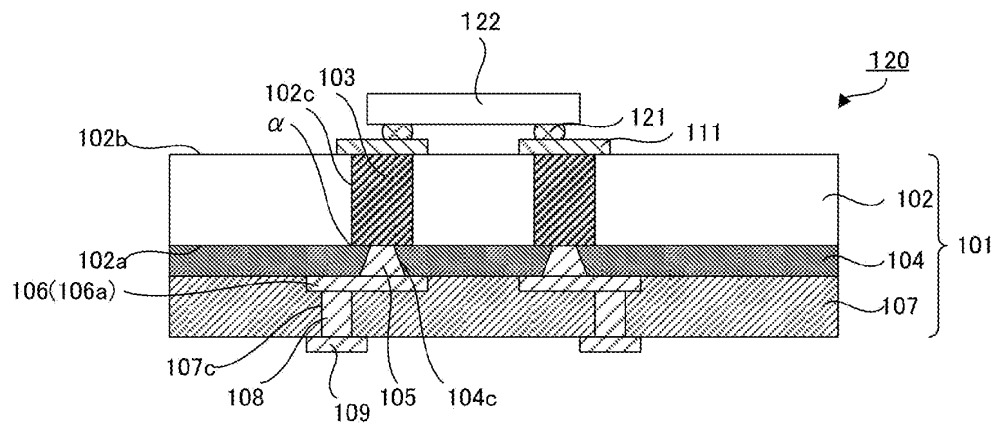


[図20]

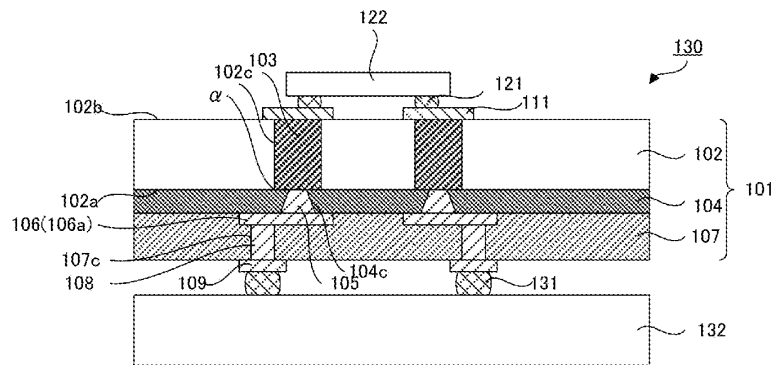




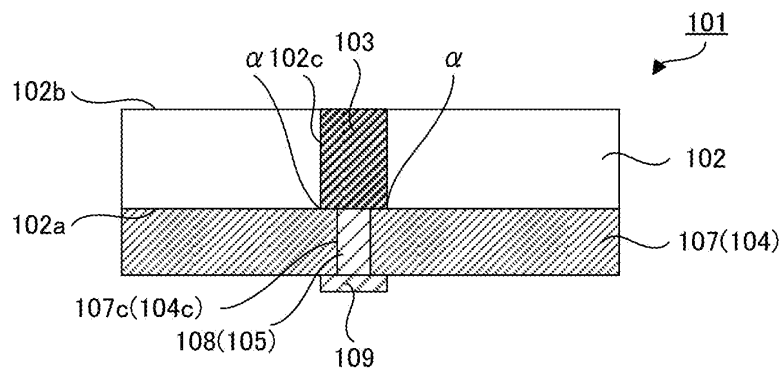
[図24]



[図25]

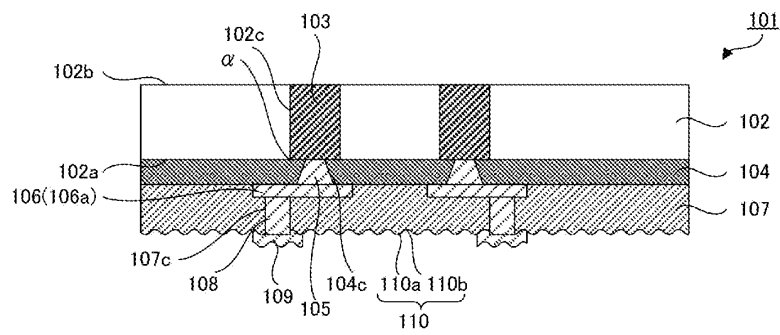


[図26]





[図30]



[図31]

