

ABSTRACT:

"A direct conversion receiver"

In known direct conversion receivers, e.g. for paging, for getting a correct polarity a.f.c. signal, the a.f.c. signal is derived by multiplying demodulated data with an error voltage obtained with a frequency discriminator. Apart from the fact that this requires an elaborate circuit, data filter delay has to be compensated for before multiplying the demodulated data with an output signal of the frequency discriminator. The direct conversion receiver (1) according to the present invention comprises a.f.c. means comprising a digital-to-analog converter (31) for providing a control signal (ct) for a local oscillator (14). The control signal (ct) is determined on a valid data scanning basis, i.e. during scanning intervals, signal quality determining means (32) determine valid data (vdta) while a controller (20) steps through an output range (DAR) of the digital-to-analog converter (31). The control signal (ct) is adjusted within a valid data range (VR), and the scanning is repeated on a regular basis. The present invention provides a simple a.f.c. means, an otherwise necessary loop filter being dispensed with. Signal quality can be based on measured signal frequency or on other criteria such as a valid CRC, a CRC with a unique error syndrome, or the like.

Fig. 1