

ABSTRACT

A semiconductor device includes a substrate including a logic cell region and an ESD cell region, a plurality of active fins on the ESD cell region, disposed alternately in a first direction, including first active fins and second active fins disposed alternately and spaced apart in the first direction, a device isolation layer defining the first and second active fins, a pair of source/drain patterns on each of the plurality of active fins, spaced apart from each other in a second direction intersecting the first direction, a channel pattern between the pair of source/drain patterns, and a gate electrode extending in the first direction on the channel pattern, wherein each of the first and second active fins extending in the second direction, and a length of the first active fin in the second direction is greater than a length of the second active fin in the second direction.

FIG. 2